SONY

Semiconductor IC

Data Book 1987

Audios

SONY®

Semiconductor Integrated Circuit Data Book 1987

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Semiconductor Integrated Circuit Data Book
1987

SONY®

PREFACE

This is the 1987 version of the Sony semiconductor IC databook. This book covers all the semiconductor products manufactured and marketed by Sony.

In preparation of this databook, as much characteristic and application data as possible have been collected and added with a view of making this book a convenient reference for users of Sony products. If, however, you are dissatisfied with this book in any way, please write; we welcome suggestions and comments.

The Sony semiconductor IC databook has been edited to include only accurate and reliable data. However, because of technical improvements and other modifications the contents are subject to change without notice.

The circuit examples used in this book are for illustration of typical applications only; we are not responsible for any problems that may occur in the circuitry and patents of any third party if these examples are put in practice.

Package abbreviations

DIP : Dual Inline Package
MFP : Mini Flat Package (=Flat DIP)
QIP : Quad Inline Package (=Flat QUIP)
PGA : Pin Grid Array
SRK : Shrink Dual Inline Package
SIP : Single Inline Package

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1. List of Model Names

Type	Page	Type	Page	Type	Page
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CX-857	223	CX20090 CX20091	240	CXA1019M/P	308
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CX-7925B/-1	425	CX20111	247	CXA1031M	332
CX-7961A/-1	436	CX20123	210	CXA1032M	342
CX10006	23	CX20172	86	CXA1033P	351
CX10031A	182	CX20177	261	CXA1034P	97
CX10032A	27	CX20187 CXA1097Q	109	CXA1057M	147
CX10033A	39	CX20188 CXA1098Q	125	CXA1058M	156
CX10040 CX10060	191	CX23016 CX23086	377	CXA1111P	362
CX20023	51	CXA1003AM	385	CXD1082M	401
CX20029	234	CXA1015M	281	CXD1083Q	415

2. Index by Usage

1) Tape Recorder

Type	Function	Page
CX10006	Plunger Drive for Car Stereo	23
CX10032A	Stereo Recording/Playback Preamplifier	27
CX10033A	Stereo Microphone/Buffer Amplifier	39
CX20023	Stereo Recording/Playback Preamplifier	51
CX20089A	Low-voltage Power-amplifier	64
CX20107	Preamplifier/Power-amplifier	74
CX20172	Balanced Transformer-less Dual Amplifier for Audio Use	86
CXA1034P	Stereo Headphone Amplifier (P)	97

(P) : Preliminary

2) Dolby System

Type	Function	Page
CX20187 CXA1097Q	□□ Dolby B-C Type Noise Reduction System	109
CX20188 CXA1098Q	□□ Dolby B-C Type Noise Reduction System	125
CXA1057M	□□ Stereo Dolby B Type Noise Reduction	147
CXA1058M	□□ Stereo Dolby B Type Noise Reduction	156

3) Moter Controller

Type	Function	Page
CX-065B	Frequency Servo Controller	171
CX-891	Motor Servo Control	177
CX10031A	2-Phase Brushless Moter Control	182
CX10040 CX10060	2-Phase DC Brushless Moter Control	191
CX20123	OTM Motor Servo Control	210

4) Radio

Type	Function	Page
CX-857	AM Stereo Decoder	223
CX20029	FM/AM Stereo Radio	234
CX20090 CX20091	FM/AM Radio Circuit	240
CX20111	FM/AM Radio	247
CX20177	AM Stereo Radio	261
CXA1015M	AM Radio	281
CXA1017M	AM Stereo Radio	289
CXA1019M/P	FM/AM Radio	308
CXA1030P	FM/AM Tuner	318
CXA1031M	FM/AM Radio	332
CXA1032M	AM Radio	342
CXA1033P	AM Radio	351
CXA1111P	FM/AM Radio (P)	362

(P) : Preliminary

5) Communication System

Type	Function	Page
CX23016 CX23086	Personal Radio MODEM	377
CXA1003AM	Low Power FM IF Amplifier	385
CXD1082M	Filter IC for Cellular Mobile Telephone	401
CXD1083Q	Data and SAT LSI for Cellular Radio Telephone	415

6) Frequency Synthesizer PLL

Type	Function	Page
CX-7925B/-1	Frequency Synthesizer PLL	425
CX-7961A/-1	Frequency Synthesizer PLL	436

3. IC Nomenclature

1) Nomenclature of IC product name

Currently, both the conventional and new nomenclature systems are mixed in naming IC products.

a) Conventional nomenclature system

[Example] CX20011A

- Improvement mark
  - "A" is affixed when specifications are partially improved.
- Product number
  - Identifies individual product.
- Category number
  - Indicates the product category in one or two digits.
    - Bipolar IC: 0, 1, 8, 10, 20, 22
    - MOS IC: 5, 7, 23, 79
- Sony IC mark

(2) New nomenclature

[Example] CXA1001AP

- Package mark
  - P : Plastic DIP
  - D : Ceramic DIP
  - M : Mini Flat Package
  - L : Single Inline Package
  - Q : Quad Inline Package
  - S : Shrink Dual Inline Package
- Improvement mark
  - "A" is affixed when specifications are improved.
- Product number
  - Identifies the individual product.
- Product category mark
  - A : Bipolar IC
  - B : Bipolar digital IC
  - D : MOS logic IC
  - K : Memory
  - P, Q: Microcomputer
  - L : CCD signal processor
- Sony IC mark

2) Nomenclature for CCD image product name

[Example] ICX016AK

- Filter or package mark
- Improvement mark
  - "A" is affixed when specifications are improved.
- Product number
- Sony CCD imager mark

4. Precautions for IC Application

1) Absolute maximum ratings

The maximum ratings for semiconductor devices are normally specified by "absolute maximum ratings". The values shown in the maximum ratings table must never be exceeded even in a moment.

If the maximum rating is ever exceeded, device deterioration or damage will occur immediately. Then, even if the affected device can operate, the life will be considerably short.

Maximum rating must never be reached for two items at the same time.

IC maximum ratings

The following maximum ratings are used for ICs.

(1) Maximum power supply voltage Vcc (V_{DD})

The maximum voltage that can be applied between the power supply terminal and ground terminal.

This power supply voltage rating is directly related to the dielectric voltage of transistors in the internal circuit; the transistors may be destroyed if this voltage is exceeded.

(2) Allowable power dissipation P_D

The maximum power consumption allowed in IC

In the circuit design the absolute maximum ratings must not be exceeded, and it must be designed only after considering the worst situations among the following:

- Fluctuation in source voltage
- Scattering in the electrical characteristics of electrical parts (transistors, resistors, capacitors, etc.)
- Power dissipation in circuit adjustment
- Ambient temperature
- Fluctuation in input signal
- Abnormal pulses

If this allowable power dissipation is exceeded, electrical and thermal damage may result.

This value varies with the amount of IC integration in package types.

(3) Operating ambient temperature Topr

The temperature range within which IC can operate satisfactorily.

Even if this temperature range is exceeded and some deterioration in operating characteristics is noted, the IC is not always damaged.

For some ICs, the electrical characteristics at Ta=25°C are not guaranteed even in this temperature range.

(4) Storage temperature Tstg

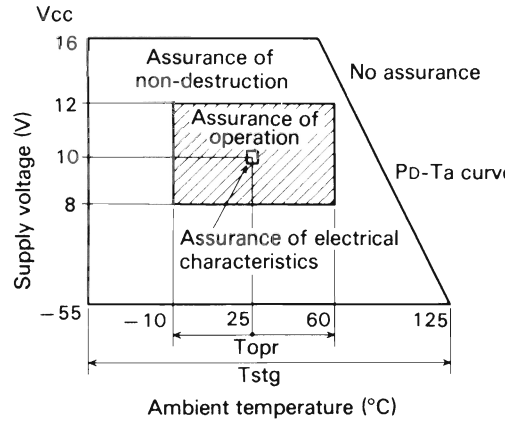
The temperature range for storing the IC which is not operating.

This temperature is restricted by the package material, and the intrinsic properties of the semiconductor.

(5) Other values

The input voltage Vin, output voltage Vout, input current Iin, output current Iout and other values may be specified in some IC's.

The relationship among these maximum ratings for IC is shown below.



2) Protection against electrostatic breakdown

There have been problems of electrostatic destruction of electronic devices since the 2nd World War. Their history is closely related to the advancement in the semiconductor devices; that is, with the development of semiconductor technology, new problems in electrostatic destruction have arisen. This situation, perhaps, can be understood by recalling the case of MOS FET.

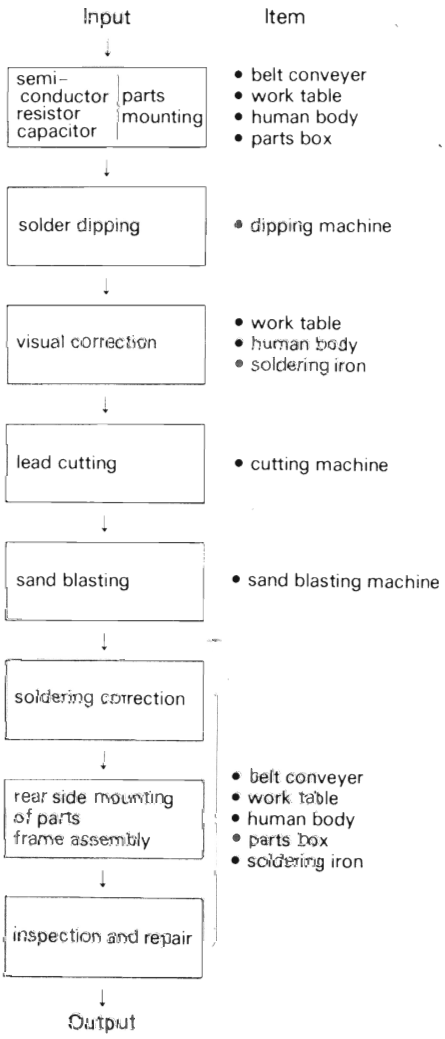
Today, the problem of electrostatic destruction is again drawing people's attention as we are entering the era of LSI and VLSI. Here are our suggestions for preventing electrostatic destruction in the device fabrication process.

Factors causing electrostatic generation in manufacture process

A number of dielectric materials are used in manufacture process. Friction of these materials with the substrate can generate static electricity which may destroy the semiconductor device.

Factors that can cause electrostatic destruction in the manufacture process are shown below:

Causes of electrostatic destruction of semiconductor parts in manufacture process



Handling precautions for preventing electrostatic destruction

Explained below are procedures that must be taken in fabrication for preventing the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

① Equalize potentials of terminals when transporting or storing.

② Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.

③ Prepare an environment that does not generate static electricity.
One method is keeping relative humidity in the work room about 50%.

Operator

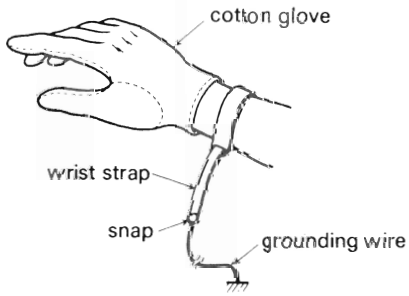
(1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

(2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm. If wrist strap cannot be used, then the operator should touch the grounding point with his hand, before handling any semiconductor device.

example of grounding band

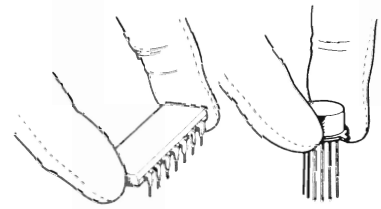


When using a copper wire for grounding, connect a 1MΩ resistance in series near the hand for safety.

(3) Handling of semiconductor device

Do not touch the lead. Touch the body of semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

holding of semiconductor device



DIP type can type

Equipment and tools

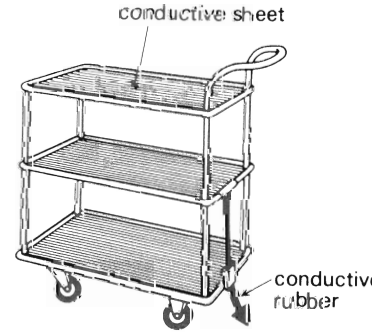
(1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

[Check point]

- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks

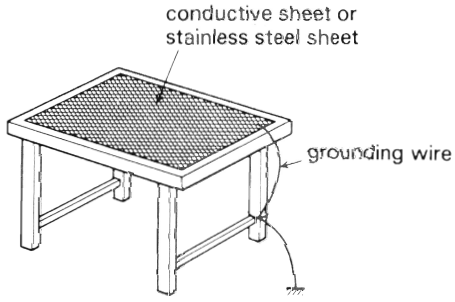
grounding of carrier



(2) Grounding of work table

Ground the work table as illustrated. Do not put anything which can easily generate static electricity, such as foam styrol, on the work table.

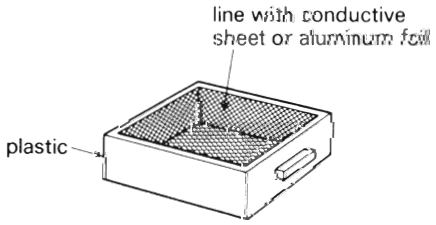
grounding of work table



(3) Semiconductor device case

Use the metal case, or the antistatic plastic case (lined with conductive sheet or aluminum foil).

plastic case for semiconductor devices



(4) Insertion of semiconductor device

Insert the semiconductor device in mounting process or on the belt conveyer. The insertion should be done on a conductive sheet, or a wood or metal carrier.

(5) Operation in energized state

When the substrate is checked while energizing the substrate where the delicate semiconductor device is mounted, be sure to place the substrate on corrugated cardboard, wood, or on a metal carrier.

(6) Other points of caution

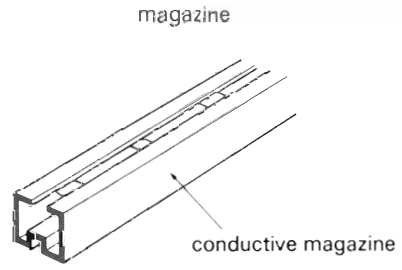
Take note of the kind of the brush material used for removing lead chips. Use metal or antistatic-treated plastic brushes.

Transporting, storing and packaging methods

(1) Magazine

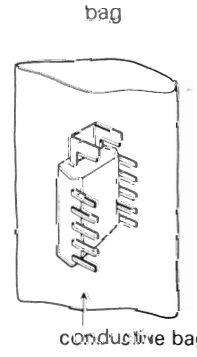
Use the metal, or antistatic-treated plastic IC magazines.

The plastic magazines used for shipping ICs are antistatic-treated, and they can be used for storing ICs.



(2) Bag

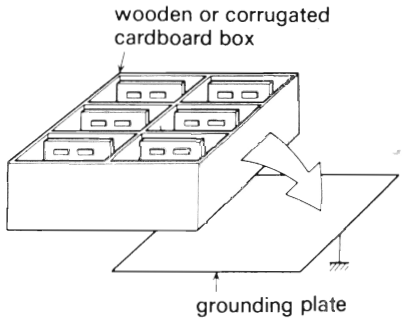
Use a conductive bag for keeping ICs. If use of a vinyl bag is unavoidable, be sure to wrap the IC with aluminum foil.



(3) Handling of delivery box

The delivery box used for carrying substrates must be made of wood or corrugated cardboard. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

handling of delivery box



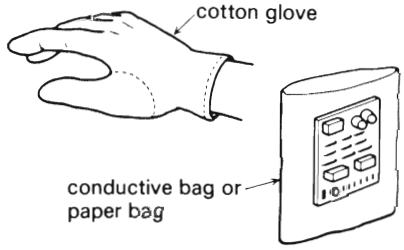
(4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table, or concrete floor for discharging. Do not pull the delivery box for more than 1 meter except on a concrete or a wooden floor.

(5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive or paper bag. Do not use a polyethylene bag.

handling of mounted substrate



Soldering operation

(1) Soldering iron

Use a soldering iron with a grounded metal part or a soldering iron whose insulation resistance after five minutes from energizing is greater than 10 MΩ (DC 500V).

(2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by car.

(3) Correction

When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves. Also, connect the grounding band to the arm, or touch the grounding point before operation.

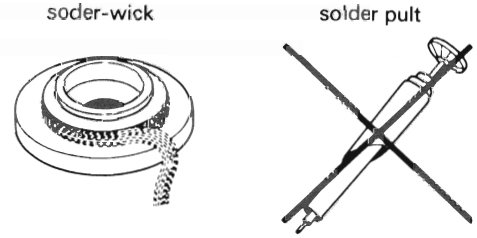
(4) Manual soldering

Solder with wrist strap connected to the hand, or by touching the grounding point from time to time during operation.

(5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Soder-wick or equivalent.

solder remover



(6) Soldering work table

Use a grounded work table, corrugated cardboard, or wooden work table for soldering. Do not solder on foam styrol, vinyl, or decorative board.

3) Mounting method

Soldering and solderability

(1) Solderability guaranteed by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2". An abstract of this standard follows:

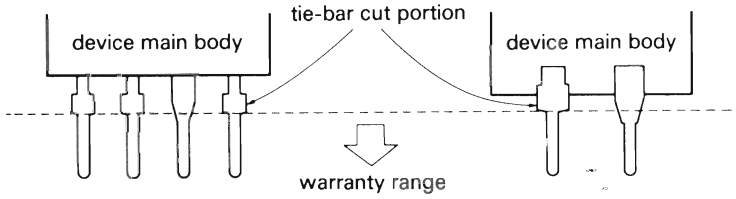
- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which has been heated to 230°C±5°C for 5±1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

(2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.

warranty area for soldering



Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10±1 seconds in a solder bath of 260°C±5°C, or for $3^{+0.5}_{-0}$ seconds in a solder bath of 350°C ±10°C, for a distance of up to 1 to 1.5 mm from the main body.

The temperature of 260°C ±5°C assumes the soldering with solder flow system, and the temperature 350°C ±10°C assumes soldering by soldering iron.

- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited for 10 seconds at 260°C ±5°C. The distance between the device main body and solder bath is assumed as 1.6 mm.

5. Quality Assurance and Reliability

Sony's Policy of Quality Assurance

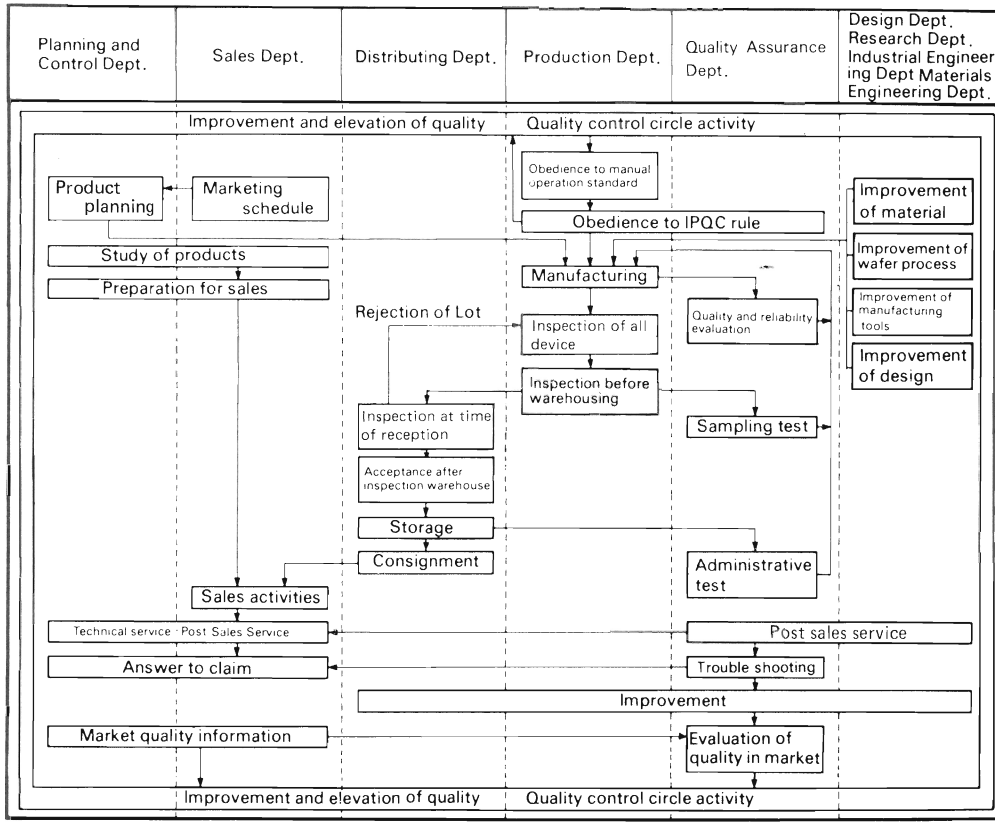
The Sony semiconductor embodies two fundamental ideas: "highest quality" and "lowest cost". There are the two key points for realizing these ideas.

One is the "quality" of men fabricating the semiconductor devices. The reliability of these people is reflected in the Sony products. Accordingly, Sony is making a continuous effort to raise the "quality" of people capable of manufacturing and fabricating Sony semiconductor devices.

The other point is a source management system combined with the concept of thorough quality design. With this system, higher quality products can be steadily manufactured through automation of device design, process design, and the fabrication process.

Sony is making constant efforts to supply the most economical and most useful products of very high quality for users.

Quality assurance system of semiconductor products



Quality assurance criteria and reliability test criteria

1) Quality assurance in shipping

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "total-inspected" at the final fabrication stage, thus ensuring no detective items. This sampling inspection is done in accordance with MIL-STD-105D.

2) Reliability

The reliability test is done, periodically, to confirm reliability level.

Periodical reliability test

Type of Test		Test Hour	LTPD (%)
Electrical characteristic test		In order to know the quality level, some types are selected and tested again.	
LIFE TEST	High temperature operation	Up to 1000 hr	10%
	High temperature storage	Up to 1000 hr	10%
	Low temperature storage	Up to 1000 hr	10%
	High temperature and high humidity storage	Up to 1000 hr	10%
	High humidity bias test	Up to 1000 hr	10%
	High temperature and high humidity with bias	Up to 500 hr	10%
	Pressure cooker	Up to 200 hr	10%
ENVIRONMENT TEST	Soldering heat resistance heat cycle	10 s	15%
	Heat cycle	10 cycle	15%
MECHANICAL TEST	Solderability	Japan Industrial Standard (JIS)	15%
	Lead strength		15%
OTHER TESTS	if necessary test, are selected accordingly to JIS C7021, C7022, EIAJ SD121, IC121.		

• These tests are selected by sampling standard.

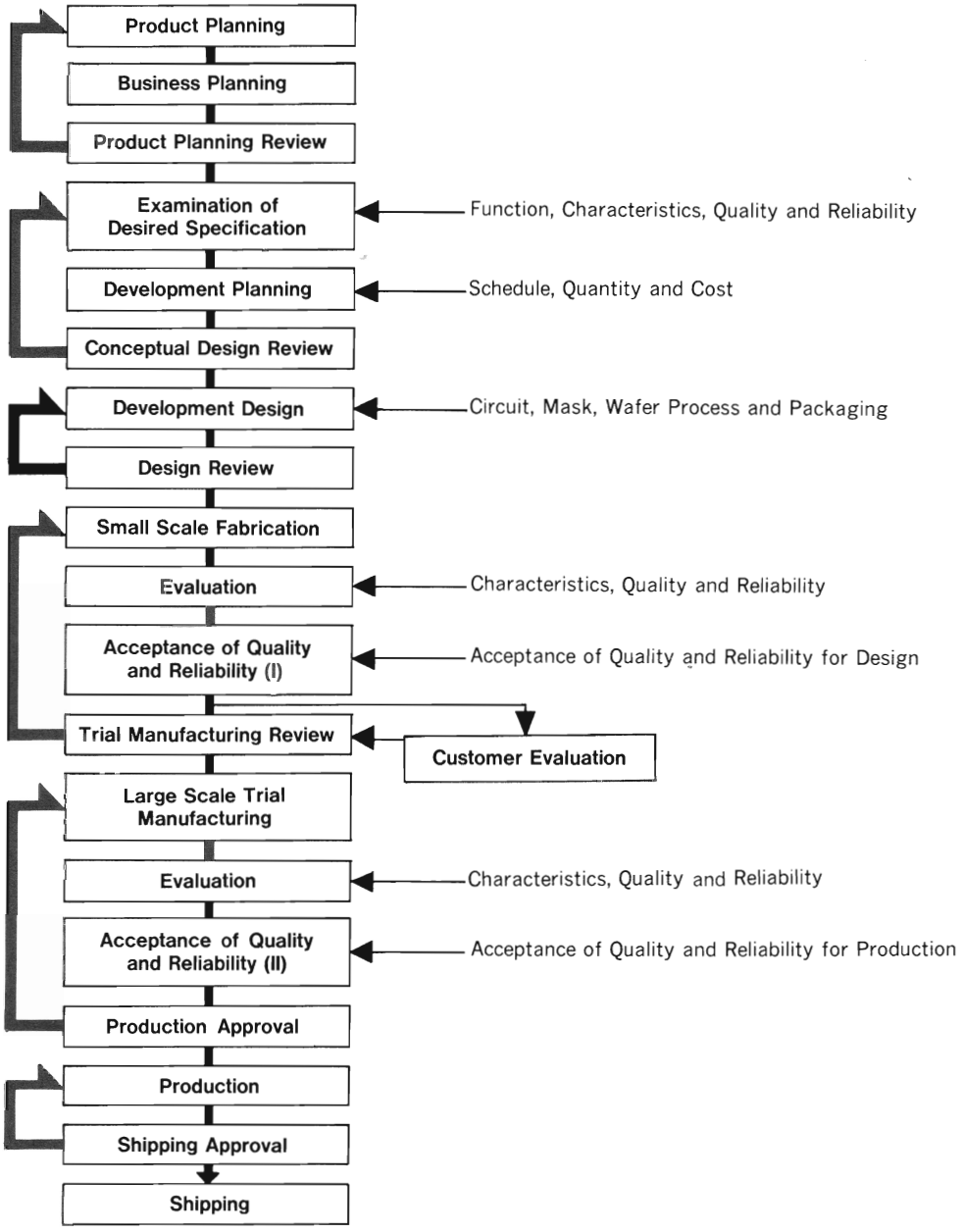
These tests and Inspection data are useful not only to estimate quality in the market place but also as data to improve design and wafer processes.

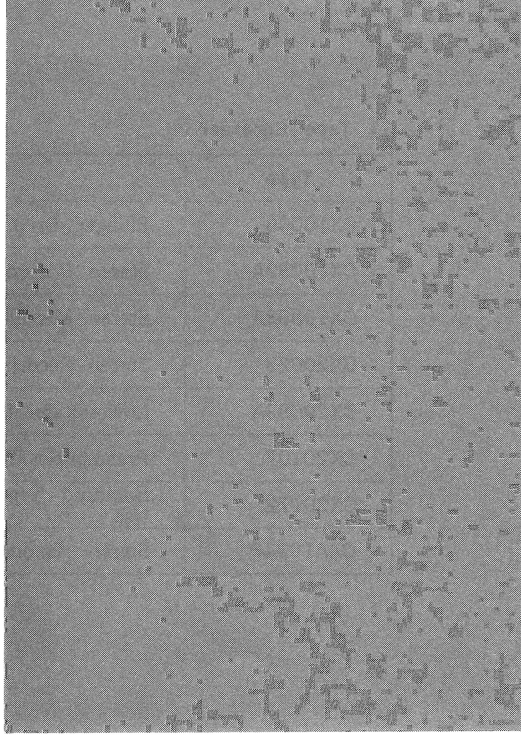
Reliability test standard for acceptance of products

Type of Test	Condition	Supply voltage	Testing time	LTPD(%)
High temperature operation	Ta = 125°C, 150°C	Typ	1000 hr	5%
High temperature with bias	Ta = 125°C, 150°C	Typ	1000 hr	5%
High temperature storage	Ta = 150°C		1000 hr	5%
Low temperature storage	Ta = −65°C		1000 hr	5%
High temperature and humidity storage	Ta = 85°C, 85%RH		1000 hr	5%
High temperature and High humidity with bias	Ta = 85°C, 85%RH	Typ (1 hr on/3 hr off)	1000 hr	5%
Pressure cooker	Ta = 121°C, 100%RH, 30 pounds per square inch		1000 hr	5%
Temperature cycle	Ta = −65°C to +150°C		100 C	10%
Heat shock	Ta = 0°C to +100°C		5 C	10%
Soldering heat resistance	Tsolder = 260°C		10 S	105
Solderability	Tsolder = 230°C (Rosin type flux)		5 S	10%
Mechanical shock	X, Y, Z 1500G 0.5 ms half sine wave		3 times for each direction	10%
Vibration	X, Y, Z 20G 10 to 2000 to 10 Hz (4 min) sine wave vibration		16 minutes for each direction	10%
Constant acceleration	X, Y, Z 20,000 G centrifugal acceleration		1 minute for each direction	10%
Fall by gravity	Falling from the height of 75cm to maple plate by gravity		3 times	10%
Lead strength (Bend) (Pull)	Japan Industrial Standard (JIS)			10%
Electrostatics strength	Device must be designed again, when electrostatic strength is below standard supplying surge voltage To each pin under the conditions of C = 200PF and Rs = 0 Ω.			

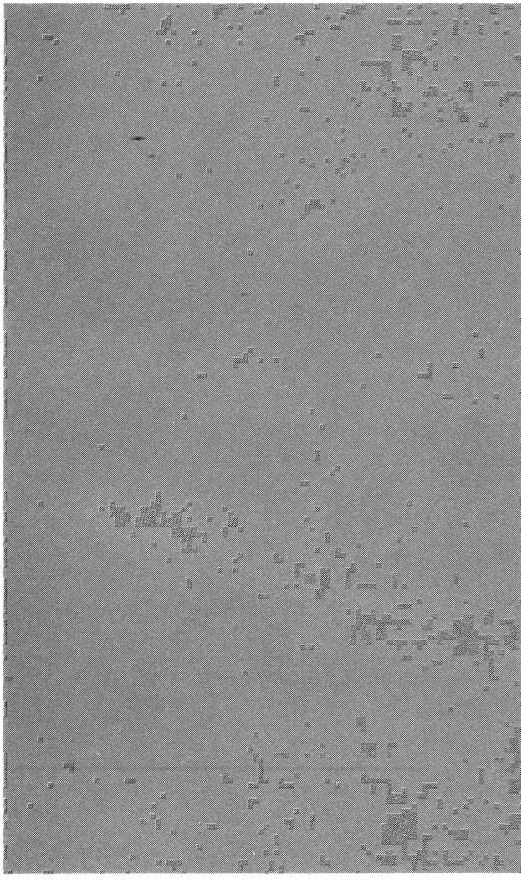
Flow Chart from Development to Manufacturing

Sony attains high quality and high reliability of semiconductor products by designing devices with quality and reliability from the initial steps of development and evaluating them sufficiently in each step of the development.





Tape Recorder



1) Tape Recorder

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CX20089A	Low-voltage Power-amplifier	64
CX20107	Preamplifier/Power-amplifier	74
CX20172	Balanced Transformer-less Dual Amplifier for Audio Use	86
CXA1034P	Stereo Headphone Amplifier (P)	97

(P) : Preliminary

Plunger Drive for Car Stereo

Description

The CX10006 is a bipolar IC designed to drive the plunger by detecting the stop signal of rotary detector signal, when combined with detecting device, this IC forms a compact car stereo with high sensitivity, automatic reverse system and automatic eject system.

Features

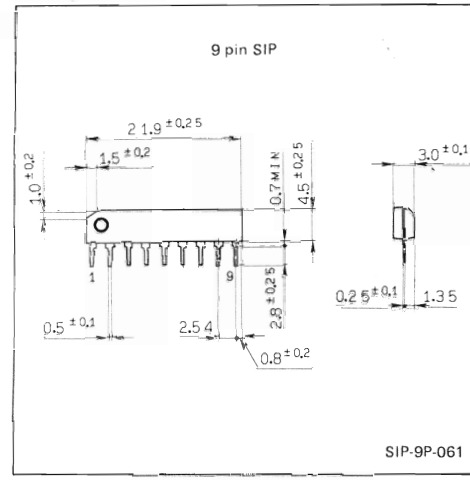
- Stabilized power supply for magnetoresistance device.
- Muting output amplifier incorporated.
- Signal output pin for detecting rotator enables application to other use.

Structure

Bipolar Silicon Monolithic IC.

Package Outline

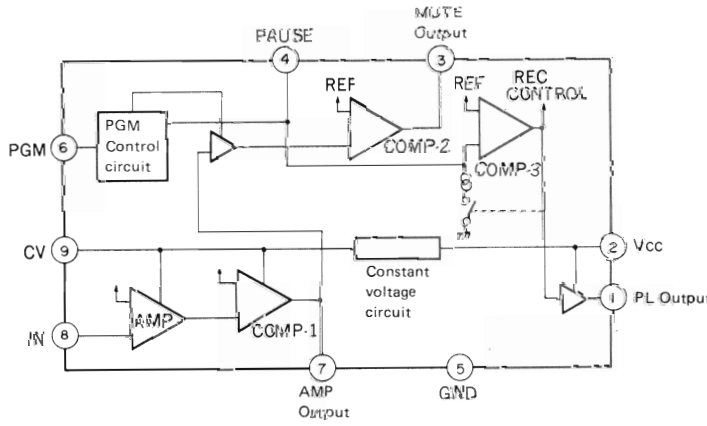
Unit: mm



Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	18	V
• Serge power supply voltage	$V_{CCSURGE}$	40	V
• Load current	I_{OUT}	0.1	A
• Operating temperature	T_{OPR}	−20 to +75	°C
• Storage temperature	T_{STG}	−55 to +125	°C
• Allowable power dissipation	P_D	350	mW

Block Diagram



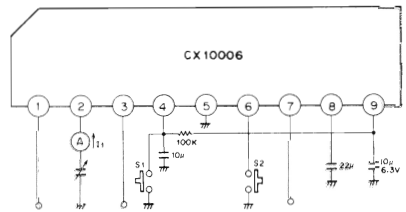
Electrical Characteristics

(Ta=25°C, Vcc=13.2V)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input Sensitivity	Vin		3		30	mVp-p
Plunger Response Time	tr	R=100kΩ C=10μF	1.0	1.3	1.6	sec
Plunger Drive Time	tp	R=100kΩ C=10μF	0.1	0.14	0.2	
Operating Voltage	VCCop		8	13.2	18	V
Current Consumption	ICCoff	Unload Vcc=18V		8	13	mA
Mute Signal Delay Time	tm	R=100kΩ C=10μF		0.05	0.1	sec
PL Output Saturation Voltage	Vsat	IL=100mA		1.2	2.0	V
CV Terminal Voltage	Vq	Unload	5	5.5	6	
Program Response Time	tPGM			50		ms

Test Method

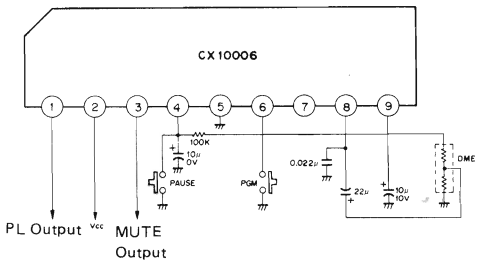
Electrical Characteristics Test Circuit



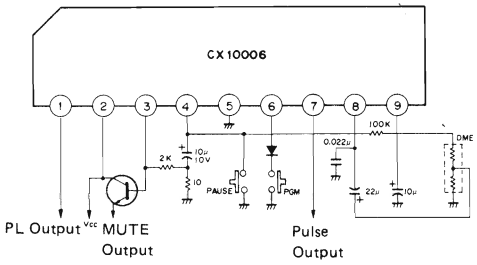
1. Input Sensitivity
   Apply 100 Hz signal to pin 8. Then monitor pin 7 with oscilloscope, increase the input signal from 0 and check the input level when output is generated (3 to 30 mVp-p)
2. Plunger Response Time
   Cut pin 8 input. Measure the time from the moment when S1 was turned OFF to the moment when output was generated from pin 1 (1.0 to 1.5 sec)
3. Plunger Drive Time
   Cut pin 8 input. Then measure the period of time when pin 1 stayed at level H. (0.1 to 0.2 sec)
4. Current Consumption
   Feed signal over 30 mVp-p to pin 8. Measure I1. (13 mA at maximum)
5. Mute Signal Delay Time
   Cut pin 8 input. Monitor pin 1 and pin 3 by dual trace. Measure time from the moment when pin 3 reached H level to the moment when pin 1 reached H level (0.1 sec at maximum) Suitable load should be connected to pin 3 (★10kΩ)
6. Program Response Time
   Feed signal over 30 mVp-p to pin 8. Measure the time from the moment S2 was turned ON to the moment when output is generated from pin 3 Mute output. (50 ms typ.)

Application Circuit

1) Repeat operation of PGM, without rotating pulse.



2) One-shot operation of PGM, with rotating pulse.

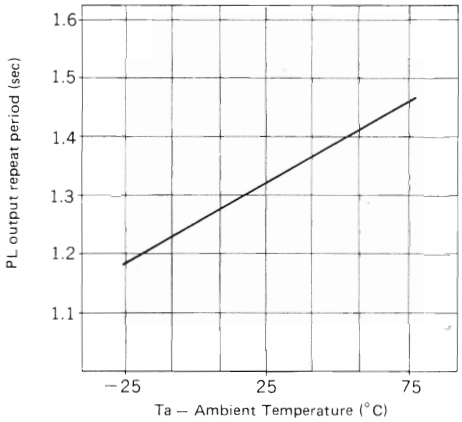


Notes on Application

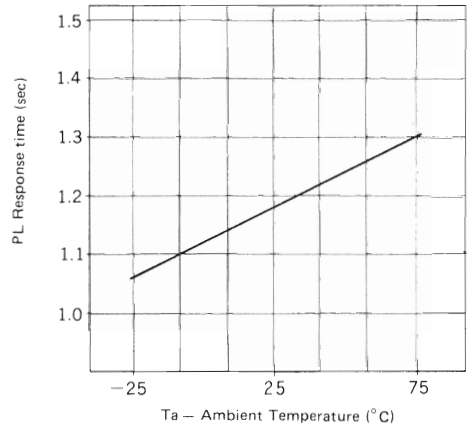
1. PL output generates output level about Vcc−1(V). Select a suitable control resistance value so that PL output current stays below 100 mA.
2. When programming in one-shot operation, use a capacitor with small internal resistance for determining time constant.
3. MUTE output generates output of about CV−1(V) (4.5V). Select the control resistance value for MUTE load so that current is 3 mA at maximum.

Temperature Characteristics

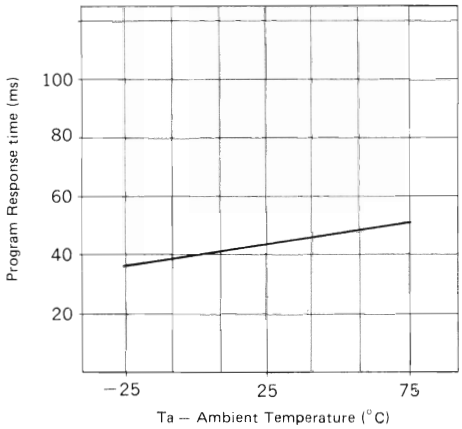
PL Output Repeat Period



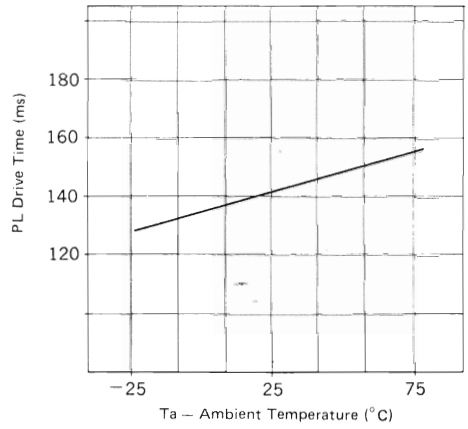
PL Response Time



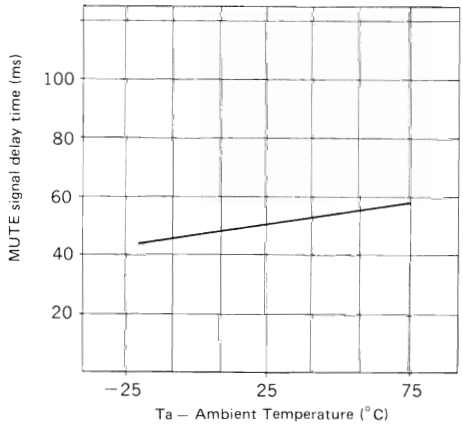
Program Response Time



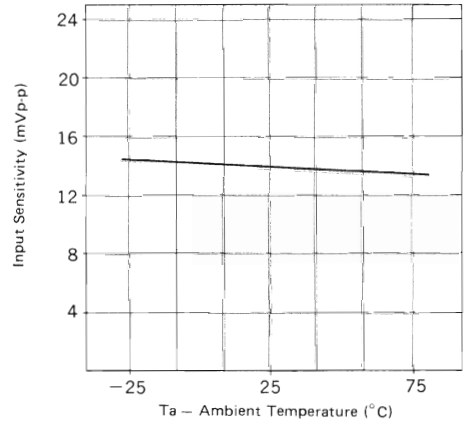
PL Drive Time



MUTE Signal Delay Time



Input Sensitivity



Stereo Recording/Playback Preamplifier

Description

The CX10032A is an IC designed to be used for cassette tape deck. It incorporates playback equalizer amplifier and recording equalizer amplifier 2 channels each into a single chip.

Features

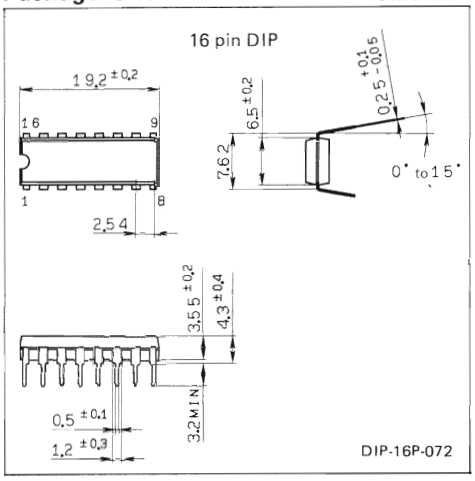
- Split power supply (±7V)
- Playback equalizer characteristic is low-noise design matched with the head.
- Recording equalizer output is constant current source to drive the head.

Structure

Bipolar silicon monolithic IC.

Package Outline

Unit: mm



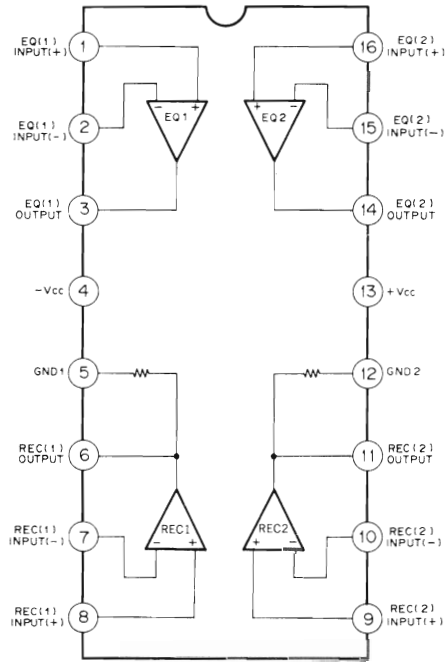
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	±10	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−40 to +125	°C
• Allowable power dissipation	PD	350	mW

Recommended Operating Conditions (Ta=25°C)

		Min.	Typ.	Max.	
• Supply voltage	Vcc	±6	±7	±8	V
• Voltage gain (EQ amp)	Gv	24	40	50	dB
• Voltage gain (REC Rg=220Ω)	Gv	10	20	30	dB
• Voltage gain (REC Rg=15 kΩ)	Gv	0	0	15	dB
• Input gain (EQ amp)	VI	0.02	1	10	mV
• Input gain (REC amp)	VI	24.5	40.0	77.5	mV

Block Diagram and Pin Configuration (Top View)



Equalizer Amplifier * f = 400 Hz Other $\begin{matrix}Rg = 220\Omega \\ R_L = 10\ k\Omega\end{matrix}$ G_V = 40 dB/1 kHz NAB

* Circuit Current entire characteristic

Electrical Characteristics

(Ta=25°C Vcc=±7V)

Item	Symbol	Test Circuit	Min.	Typ.	Max.	Unit
Circuit Current	Icc	Fig. 1*	–	6.8	10.4	mA
Open Voltage Gain	GVO	Fig. 2	81	91	–	dB
Total Harmonic Distortion	THD	Fig. 3	–	0.01	0.05	%
Maximum Output Voltage	Vom	Fig. 3	2.0	4.0	–	Vrms
Noise Output Voltage 1	NL1	Fig. 4	–	24.2	43.0	μVrms
Noise Output Voltage 2	NL2	Fig. 5	–	77.5	126.0	μVrms
Output Impedance	ZOUT	–	–	5	25	Ω
Cross-talk 1	CT1	Fig. 5	80	90	–	dB
Cross-talk 2	CT2	Fig. 5	80	90	–	dB
Ripple Rejection Ratio	RRR(+)	Fig. 6	29	39	–	dB
Ripple Rejection Ratio	RRR(−)	Fig. 6	40	50	–	dB
Maximum Noise Output Voltage 1	NP1	Fig. 4	–	90.4	160.0	μVp-p
Maximum Noise Output Voltage 2	NP2	Fig. 4	–	310	504	μVp-p
Input Offset Voltage	VIO	Fig. 11	–	0.9	3.5	mV

Recording Amplifier Rg=15 kΩ Gv=20 dB

Item	Symbol	Test Circuit	Min.	Typ.	Max.	Unit
Open Voltage Gain	Gvo	Fig. 7	70	80	–	dB
Total Harmonic Distortion	THD	Fig. 8	–	0.01	0.05	%
Total Harmonic Distortion	THD	Fig. 8	–	0.14	0.6	%
Maximum Output Current 1	Iom1	Fig. 12	0.7	1.0	–	mArms
Maximum Output Current 2	Iom2	Fig. 12	0.25	0.35	–	mArms
Output Impedance	Zout	–	50	100	–	kΩ
Cross-talk 1	CT1	Fig. 10	80	90	–	dB
Cross-talk 2	CT2	Fig. 10	60	70	–	dB
Ripple Rejection Ratio	RRR(+)	Fig. 6	62	72	–	dB
Ripple Rejection Ratio	RRR(−)	Fig. 6	56	66	–	dB
Noise Output Voltage 1	NL1	Fig. 9	–	46	92	μVrms
Noise Output Voltage 2	NL2	Fig. 9	–	60	120	μVrms
Maximum Noise Output Voltage 1	Np1	Fig. 9	–	260	368	μVp-p
Maximum Noise Output Voltage 2	Np2	Fig. 9	–	340	480	μVp-p
Input Offset Voltage	VIO	Fig. 11	–	0.5	9.0	mV

Test Circuit

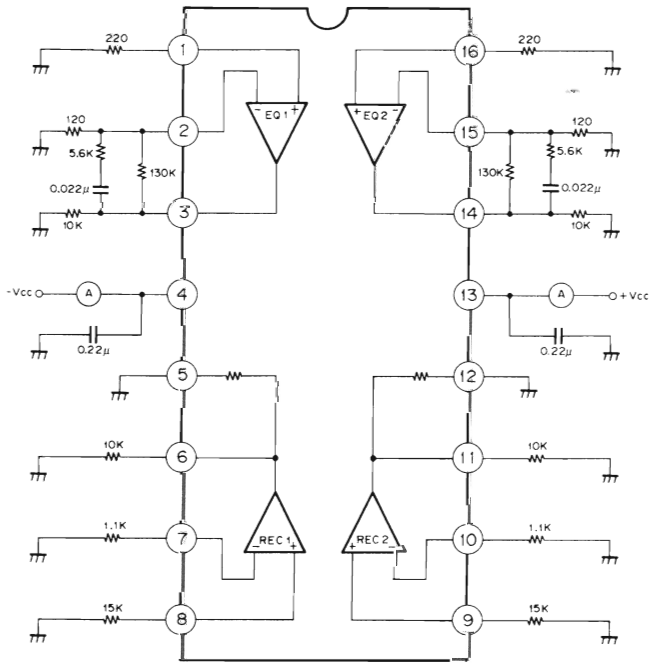


Fig. 1 Circuit current (ICC) test circuit

Open voltage gain (Gvo)

V_O = 0dBm

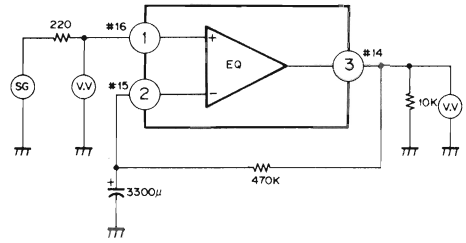


Fig. 2

Total harmonic distortion, maximum output voltage (THD, Vom)

THD : V_O = 5dBm
Vom : THD = 3%

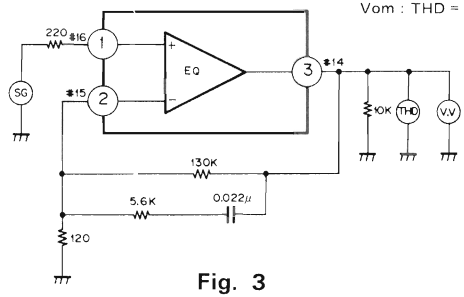


Fig. 3

Output noise level (NL1, 2), Peak noise level (Np1, 2)

NL 1, Np 1 : SW = a
NL 2, Np 2 : SW = b

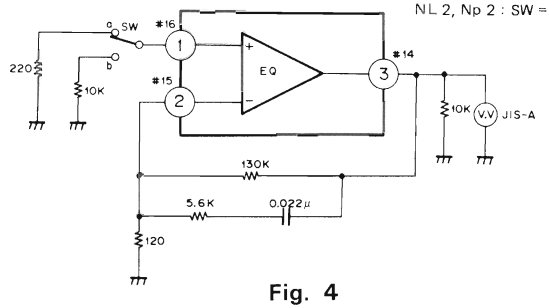


Fig. 4

Cross-talk (CT1, 2)

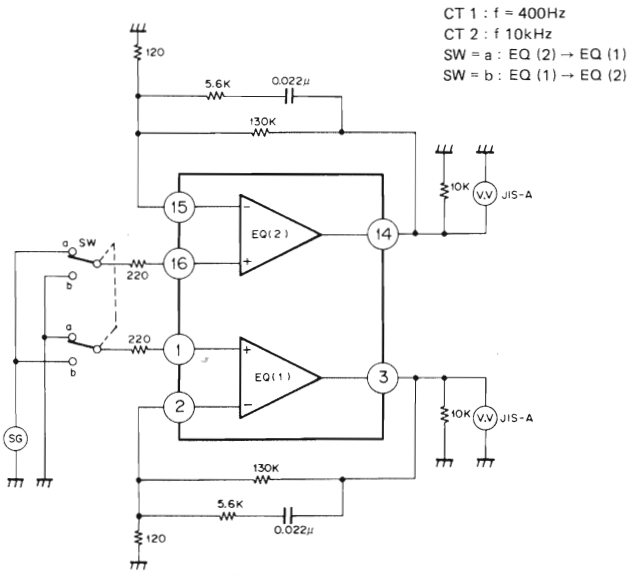


Fig. 5

Ripple rejection test circuit (RRR ±)

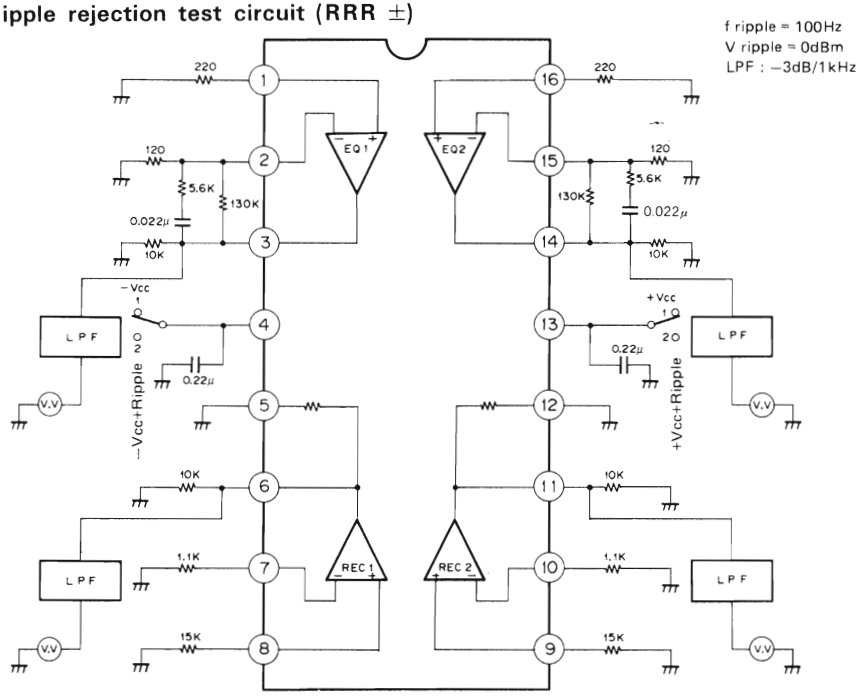


Fig. 6

Open voltage gain (Gvo)

V_O = 0dBm

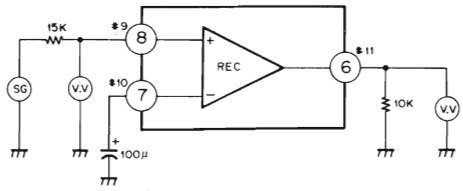


Fig. 7

Total harmonic distortion (THD)

I_O = 316μA
THD 1 : SW = a, f = 400Hz
THD 2 : SW = b, f = 400Hz

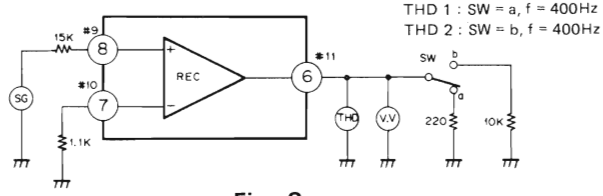


Fig. 8

Output noise level (NL1, 2), Peak noise level (Np1, 2)

NL 1, Np 1 : SW = a
NL 2, Np 2 : SW = b

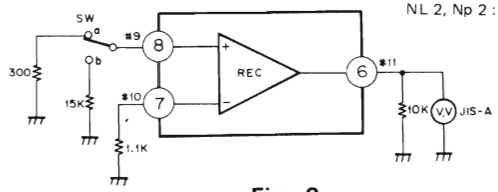


Fig. 9

Cross-talk (CT1, 2)

I_O = 316μA
SW_2, SW_3 = a : f = 400Hz
SW_2, SW_3 = b : f = 10kHz

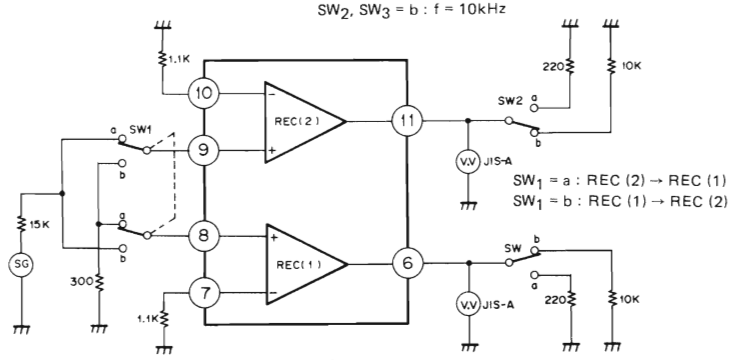


Fig. 10

Input offset voltage (V_{IO}) $V_{IO} = V_O/G_V$

$R_S \leq 10k\Omega$

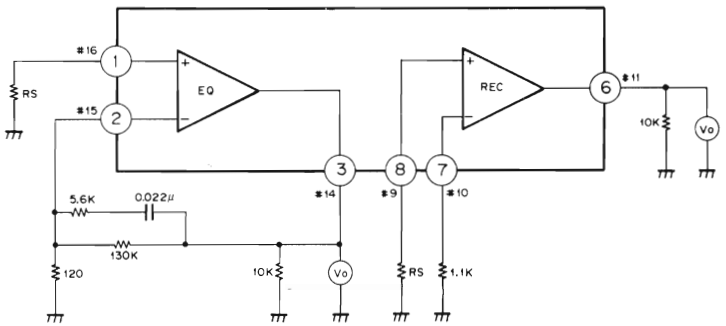


Fig. 11

Maximum output circuit (I_{OM}) $I_{OM} = V_O/R_L$

SW = a : f = 400Hz
SW = b : f = 400Hz

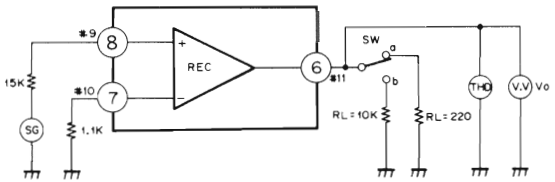
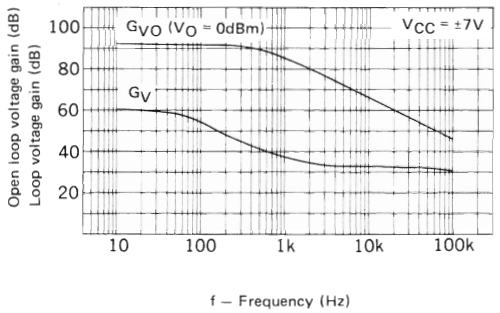
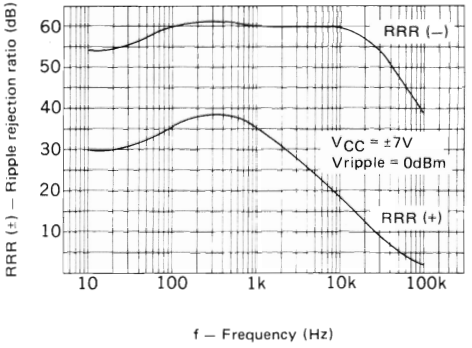


Fig. 12

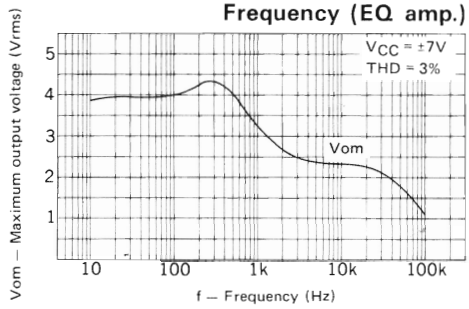
Open loop voltage gain, loop voltage gain vs. Frequency (EQ amp.)



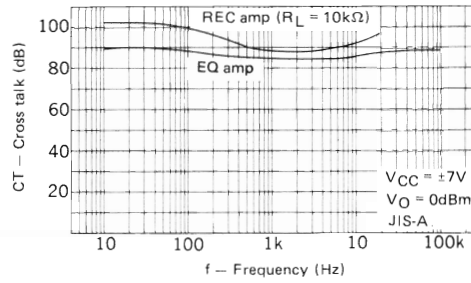
Ripple rejection ratio vs. Frequency (EQ amp.)



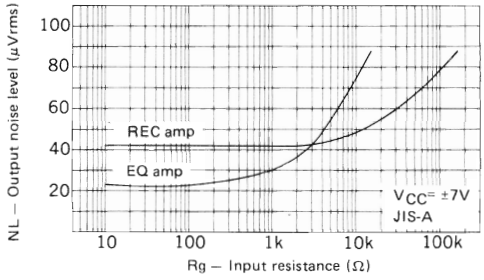
Maximum output voltage vs. Frequency (EQ amp.)



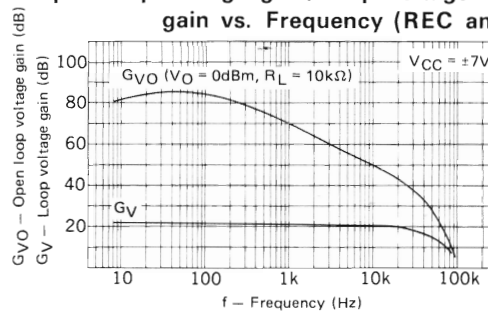
Cross-talk vs. Frequency



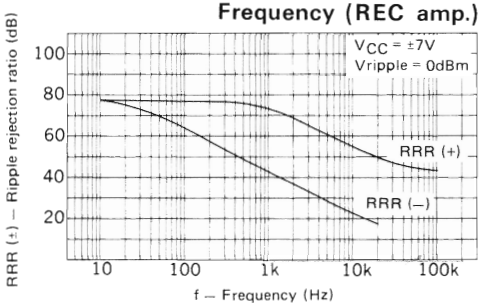
Output noise level vs. Input resistance



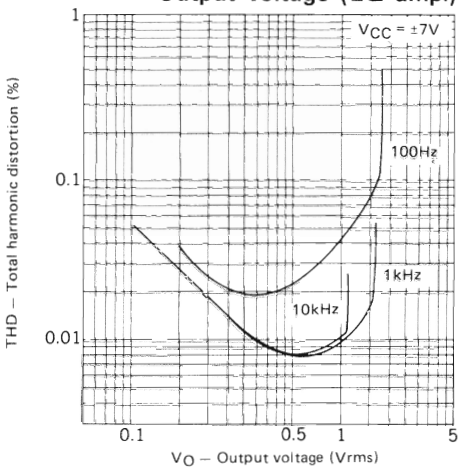
Open loop voltage gain, loop voltage gain vs. Frequency (REC amp.)



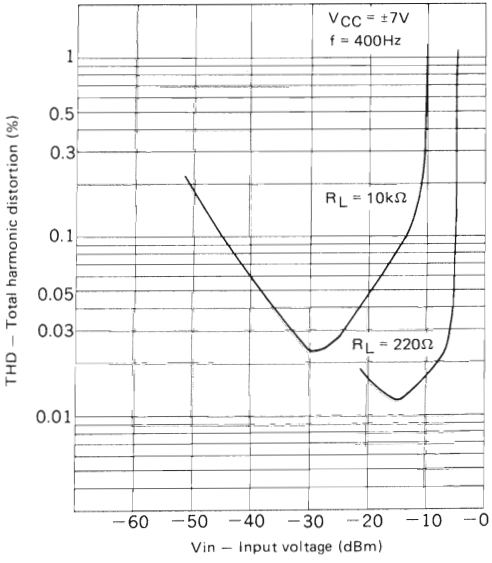
Ripple rejection ratio vs. Frequency (REC amp.)



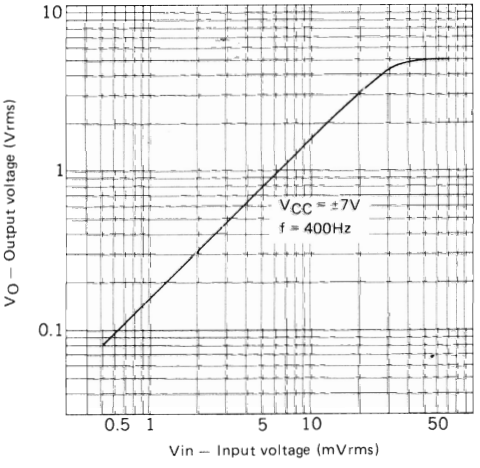
Total harmonic distortion vs. Output voltage (EQ amp.)



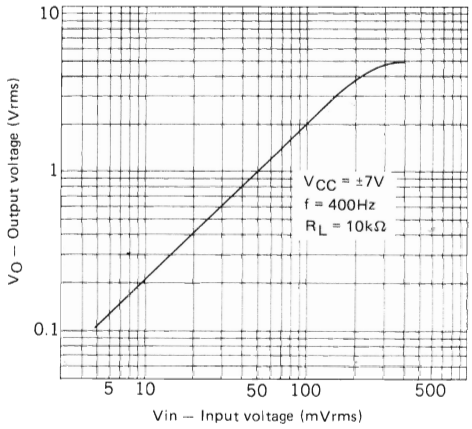
Total harmonic distortion vs. Input voltage (REC amp.)



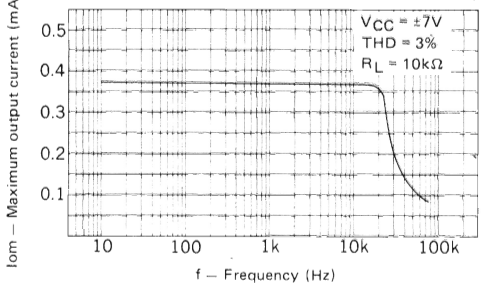
Output voltage vs. Input voltage (EQ amp.)



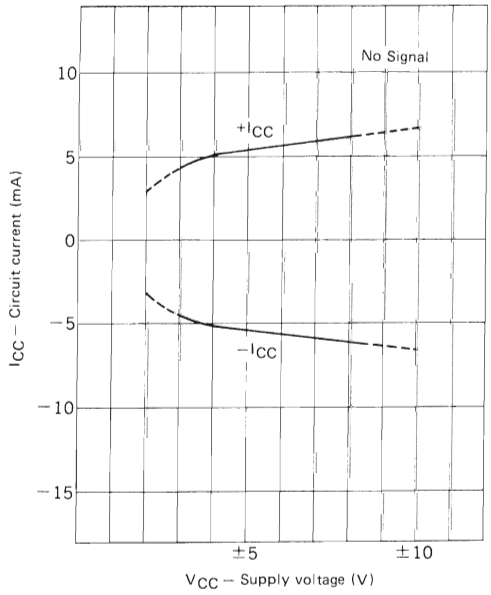
Output voltage vs. Input voltage (REC amp.)



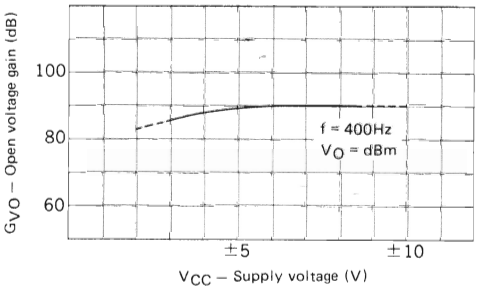
Maximum output current vs. Frequency (REC amp.)



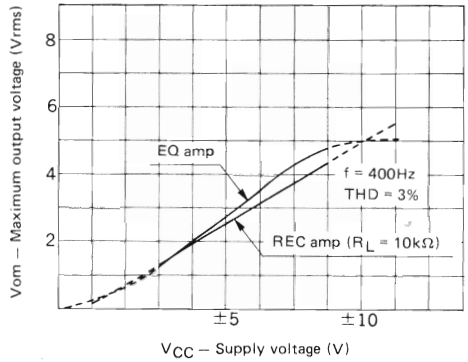
Circuit current vs. Supply voltage



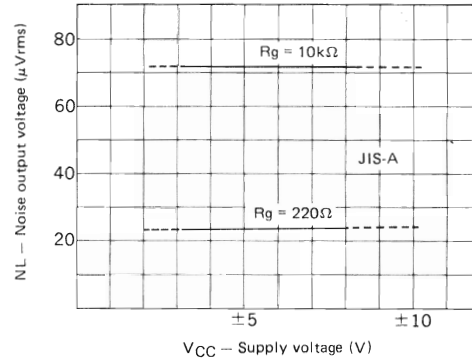
Open loop voltage gain vs. Supply voltage (EQ amp.)



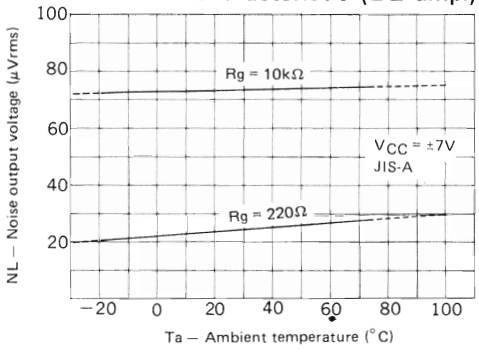
Maximum output voltage vs. Supply voltage



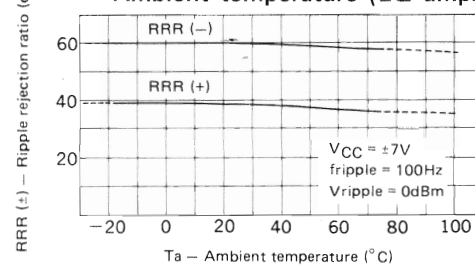
Output noise level vs. Supply voltage (EQ amp.)



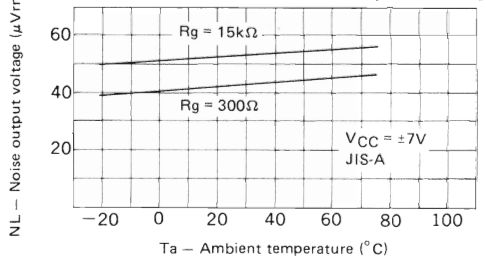
Output noise level characteristic (EQ amp.)



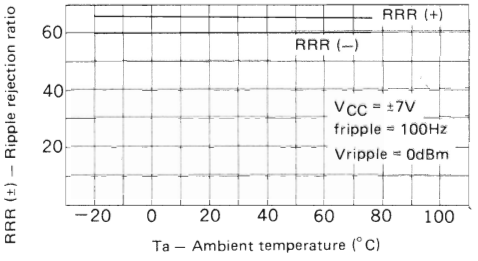
Ripple rejection ratio vs. Ambient temperature (EQ amp.)



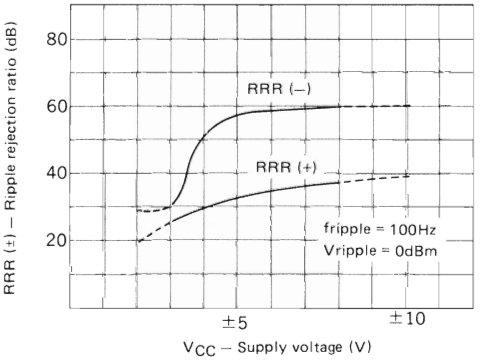
Output noise level voltage temperature characteristic (REC amp.)



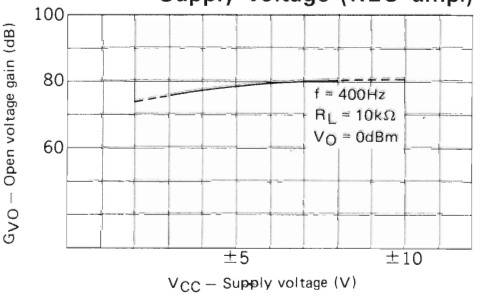
Ripple rejection ratio vs. Ambient temperature (REC amp.)



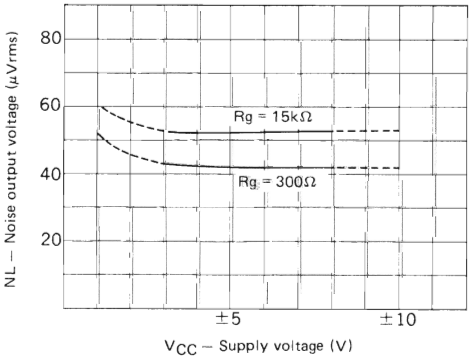
Ripple rejection ratio vs. Supply voltage (EQ amp.)



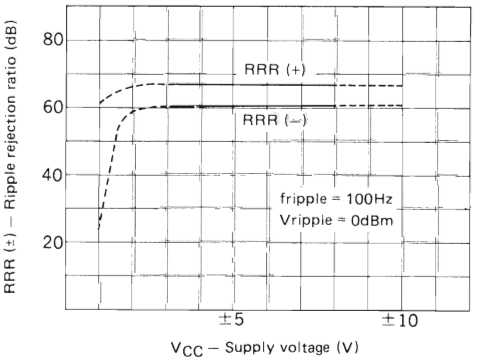
Open loop voltage gain vs. Supply voltage (REC amp.)



Output noise level vs. Supply voltage (REC amp.)



Ripple rejection ratio vs. Supply voltage (REC amp.)



Stereo Microphone/Buffer Amplifier

Description

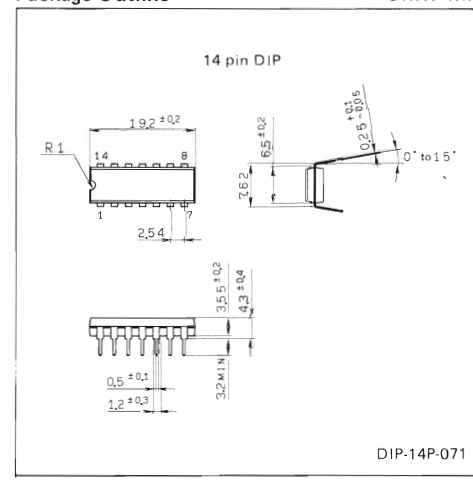
The CX10033A is an IC designed for cassette tape deck. It incorporates microphone amplifier and buffer amplifier 2 channels each in a single chip.

Features

- Split power supply (±7)
- Microphone amp is minimum-noise-designed to signal source resistance of 300 Ω.
- Buffer amplifier is minimum-noise-designed to signal source resistance of 5 kΩ.

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta=25°C)

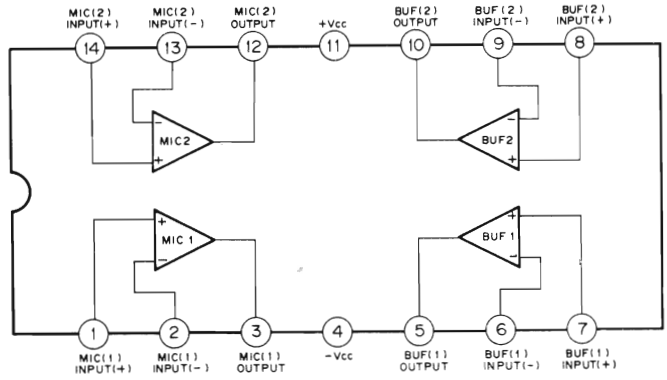
• Supply voltage	V_{CC}	±10	V
• Allowable power dissipation	P_D	350*	mW
• Operating temperature	Topr	−20 to +70	°C
• Storage temperature	Tstg	−40 to +125	°C

*Ta=75°C

Recommended Operating Conditions (Ta=25°C)

• Supply voltage	V_{CC}	±6 to ±8 (Typ. ±7)	V
• Voltage gain (MIC)	A_V	34 to 60 (Typ. 40)	dB
• Voltage gain (BUFF)	A_V	0 to 20	dB
• Load impedance (MIC)	R_L	6 to 10	kΩ
• Load impedance (BUFF)	R_L	2 to 3	kΩ

Block Diagram and Pin Configuration (Top View)



Electrical Characteristics (Ta=25°C, Vcc=±7V)

Mic Amplifier Rg=300Ω Gv=40 dB R_L=10 kΩ

Item	Symbol	Test Circuit	Min.	Typ.	Max.	Unit
Circuit Current	Icc	Fig. 1	–	8.3	14	mA
Open Voltage Gain	Gvo	Fig. 2	83	93	–	dB
Total Harmonic Distortion	THD	Fig. 3	–	0.01	0.05	%
Maximum Output Voltage	Vom	Fig. 3	3	4	–	Vrms
Equivalent Noise Input Voltage	Vnin	Fig. 4	–	0.60	0.95	μVrms
Maximum Noise Voltage	Np	Fig. 4	–	0.22	0.35	μVrms
Output Inpedance	Zout	–	–	1.6	4.8	Ω
Cross-talk 1	CT1	Fig. 5	70	80	–	dB
Cross-talk 2	CT2	Fig. 5	70	80	–	dB
Ripple Rejection Ratio	RRR(+)	Fig. 6	40	50	–	dB
Ripple Rejection Ratio	RRR(−)	Fig. 6	60	70	–	dB
Input Offset Voltage	Vio	Fig. 11	–	0.9	11	mV

Buffer Amplifier R_L=3 kΩ Rg=15 kΩ Gv=0 dB

Item	Symbol	Test Circuit	Min.	Typ.	Max.	Unit
Open Voltage Gain	Gvo	Fig. 7	51	61	–	dB
Total Harmonic Distortion	THD	Fig. 8	–	0.01	0.05	%
Maximum Output Voltage	Vom	Fig. 8	1.3	1.7	–	Vrms
Equivalent Noise Input Voltage	Vnin1	Fig. 9	–	0.51	0.85	μVrms
Equivalent Noise Input Voltage	Vnin2	Fig. 9	–	1.7	2.6	μVrms
Maximum Noise Voltage	Np1	Fig. 9	–	17.6	29.6	μVp-p
Maximum Noise Voltage	Np2	Fig. 9	–	68.0	104	μVp-p
Output Impedance	Zout	–	–	0.75	2.25	Ω
Cross-talk 1	CT1	Fig. 10	80	90	–	dB
Cross-talk 2	CT2	Fig. 10	62	72	–	dB
Ripple Rejection Ratio	RRR(+)	Fig. 6	55	65	–	dB
Ripple Rejection Ratio	RRR(−)	Fig. 6	70	80	–	dB
Input Offset Voltage	Vio	Fig. 11	–	2.4	21.3	mV

Test Circuit

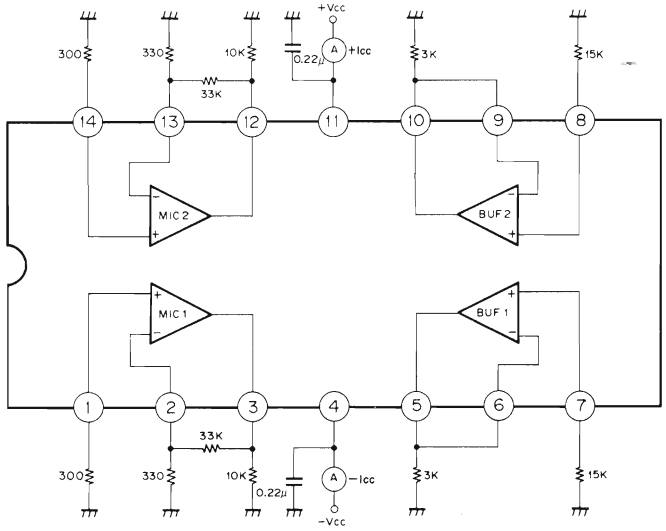


Fig. 1 Circuit Current (Icc)

Open Voltage Gain (Gvo)

V_O = 0dBm

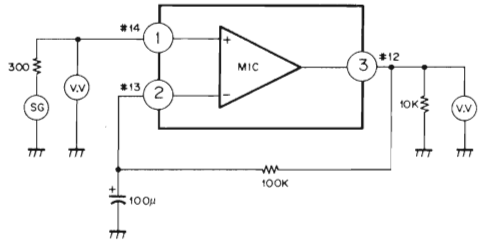


Fig. 2

Total Harmonic Distortion (THD)
Maximum Output Voltage (Vom)

THD : V_O = 10dBm
Vom : THD = 3%

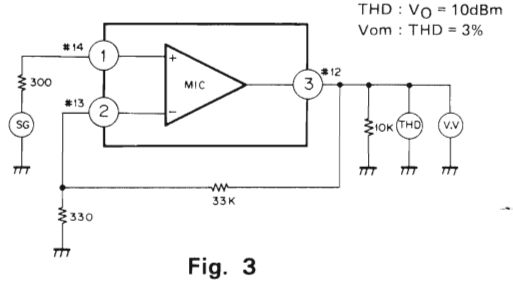


Fig. 3

Equivalent Input Noise Voltage (Vnin)
Maximum Noise Voltage (Np)

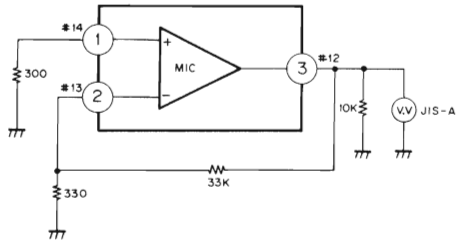


Fig. 4

Cross-talk 1 (CT1), Cross-talk 2 (CT2)

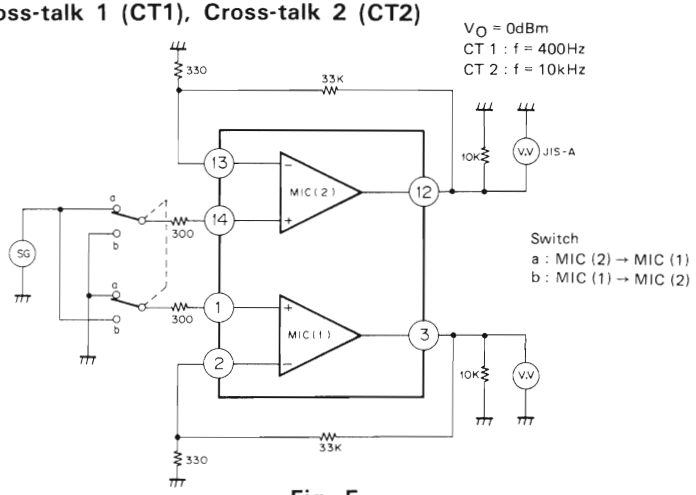


Fig. 5

Ripple Rejection RRR (±)

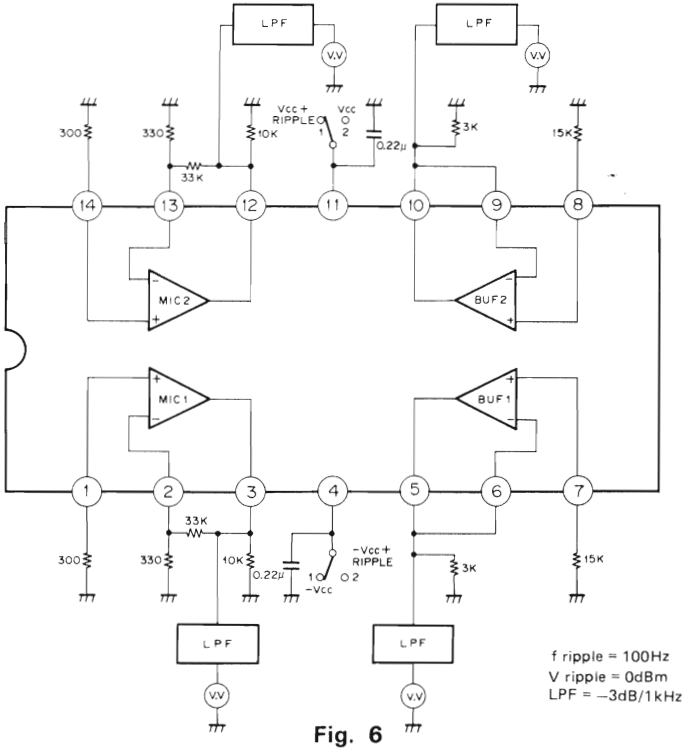


Fig. 6

Open Voltage Gain (Gvo)

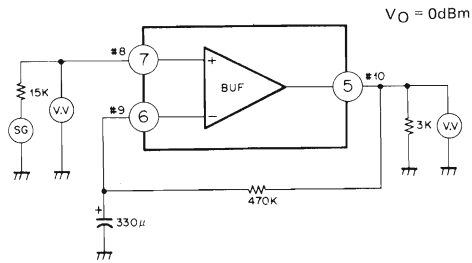


Fig. 7

Total Harmonic Distortion (THD)
Maximum Output Voltage (Vom)

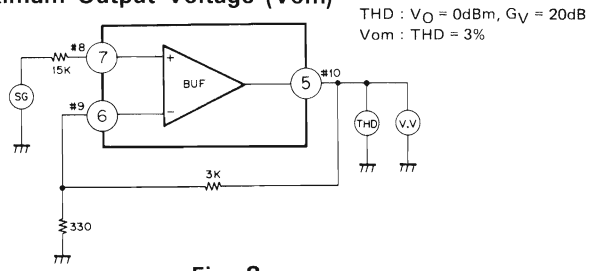


Fig. 8

Equivalent Input Noise Voltage 1, 2 (Vnin1, 2)
Maximum Noise Voltage 1, 2 (Np1, 2)

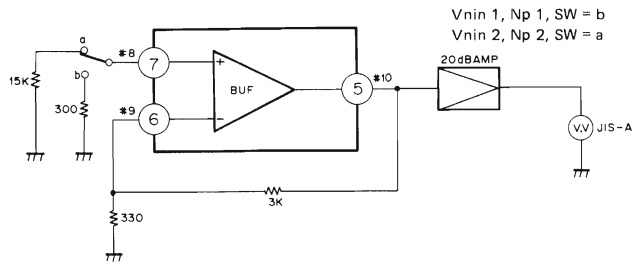


Fig. 9

Cross-talk 1, 2 (CT1, 2)

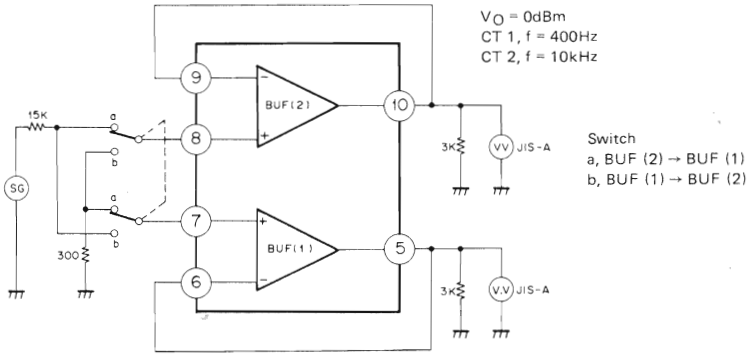


Fig. 10

Input Offset Voltage (VIO)

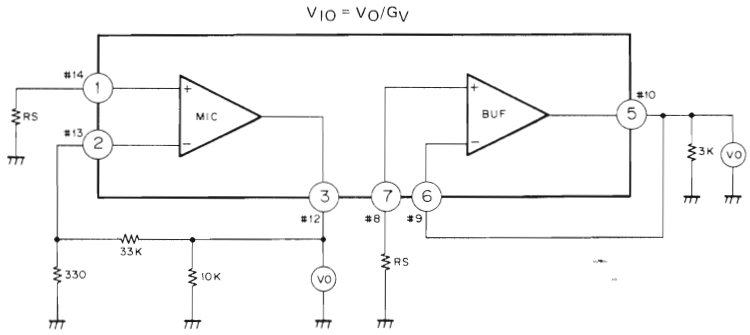
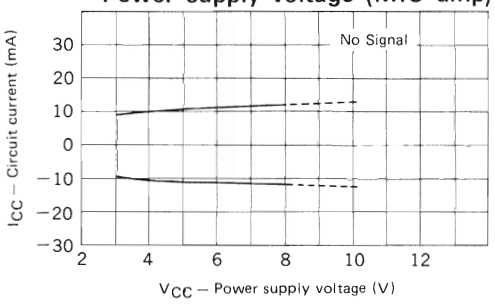
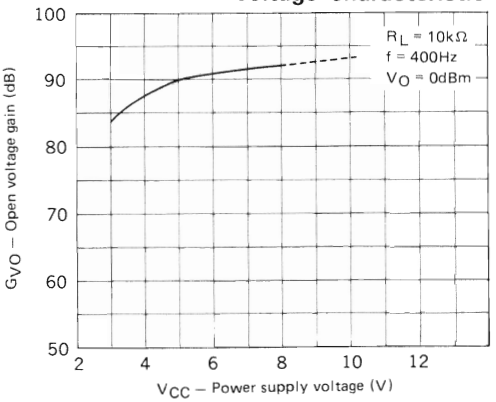


Fig. 11

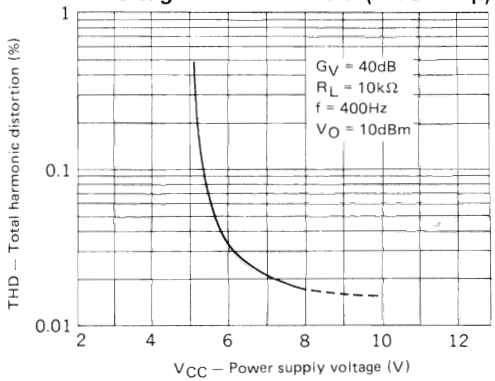
Circuit current vs. Power supply voltage (MIC amp)



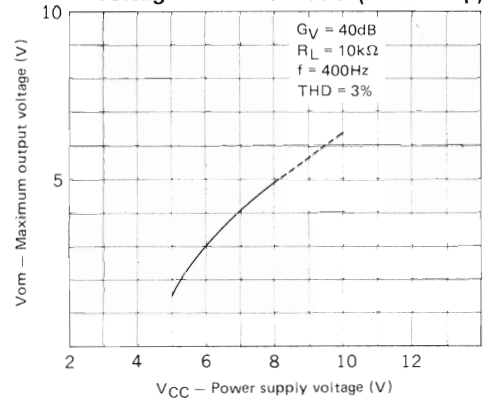
Open voltage gain vs. Power supply voltage characteristic



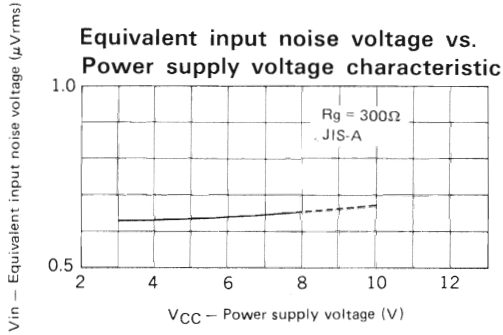
Total harmonic distortion vs. Power supply voltage characteristic (MIC amp)



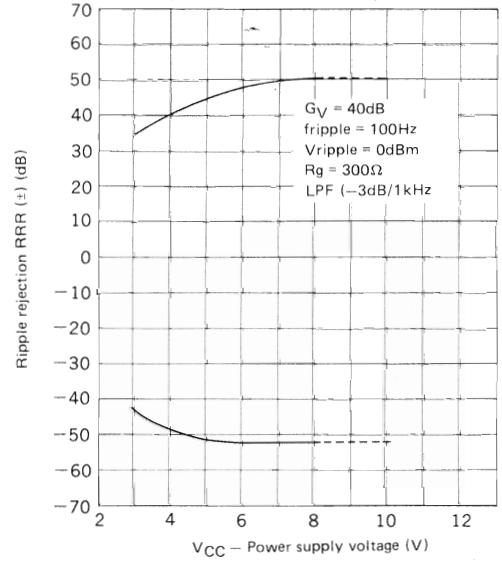
Maximum output voltage vs. Power supply voltage characteristic (MIC amp)



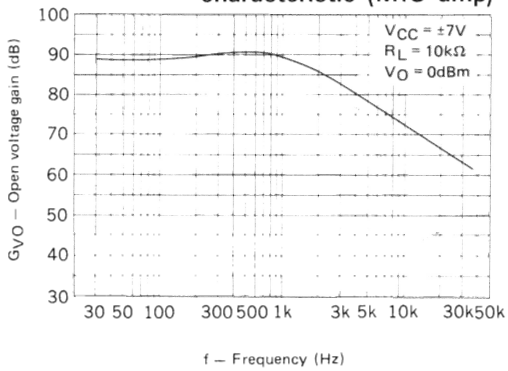
Equivalent input noise voltage vs. Power supply voltage characteristic



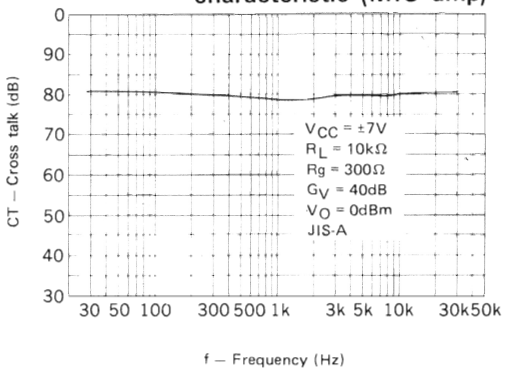
Ripple rejection power vs. Supply voltage characteristic (MIC amp)



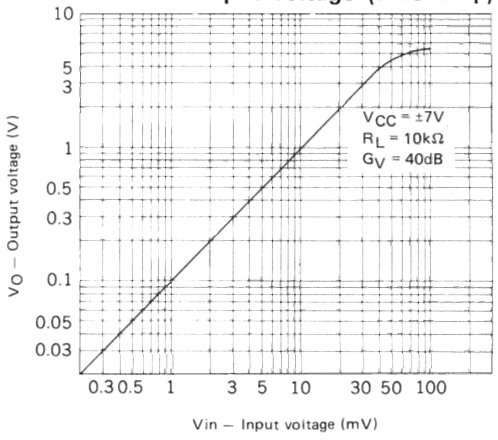
Voltage gain frequency characteristic (MIC amp)



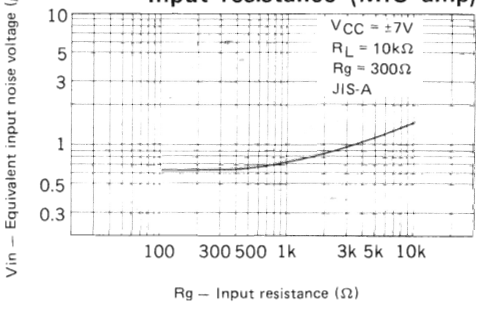
Cross-talk frequency characteristic (MIC amp)



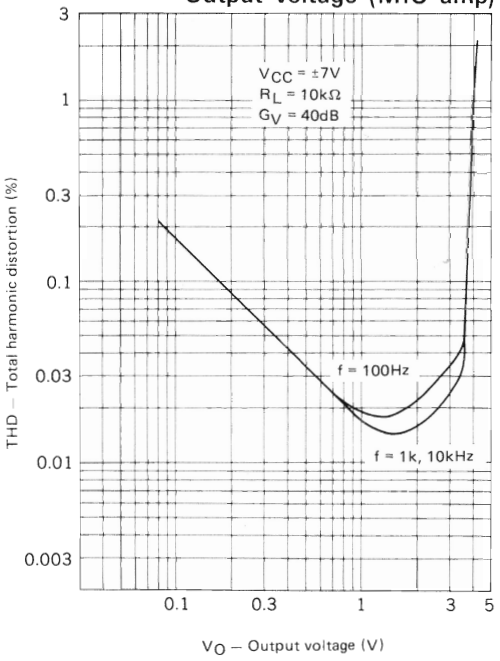
Output voltage vs. Input voltage (MIC amp)



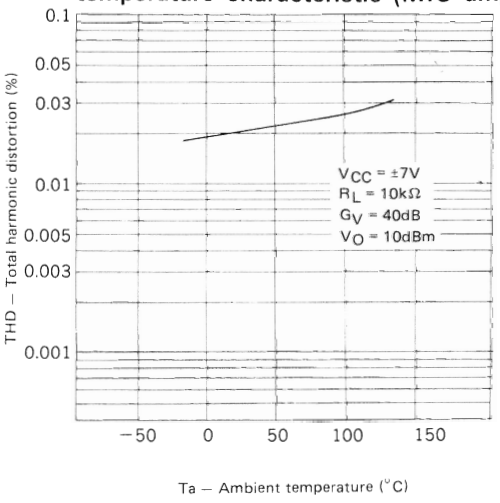
Equivalent input noise voltage vs. Input resistance (MIC amp)



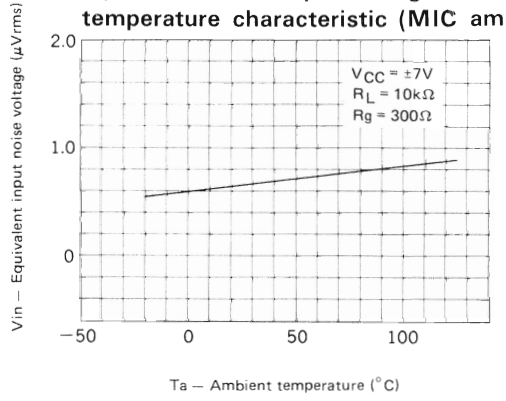
Total harmonic distortion vs. Output voltage (MIC amp)



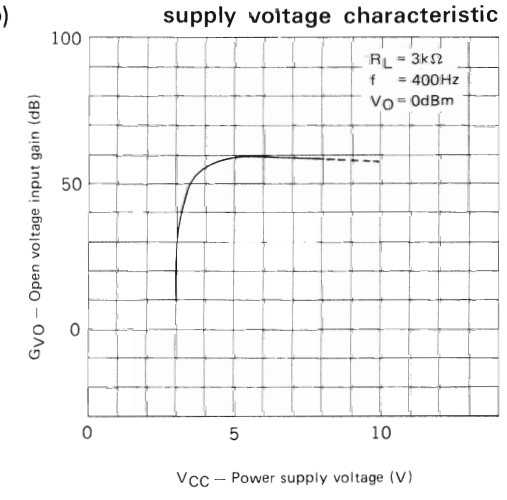
Total harmonic distortion temperature characteristic (MIC amp)



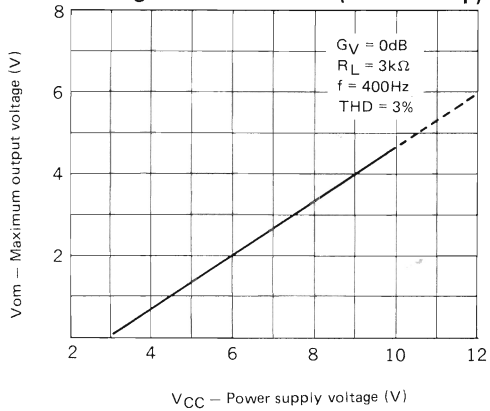
Equivalent noise input voltage temperature characteristic (MIC amp)



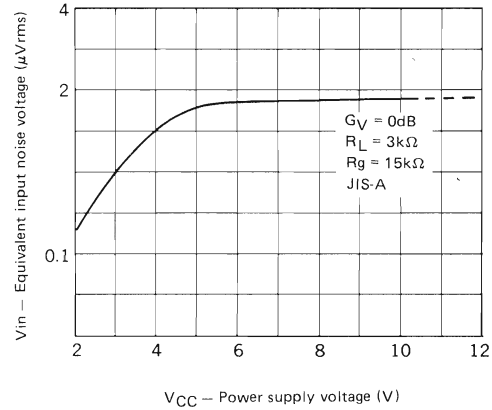
Open voltage gain power supply voltage characteristic



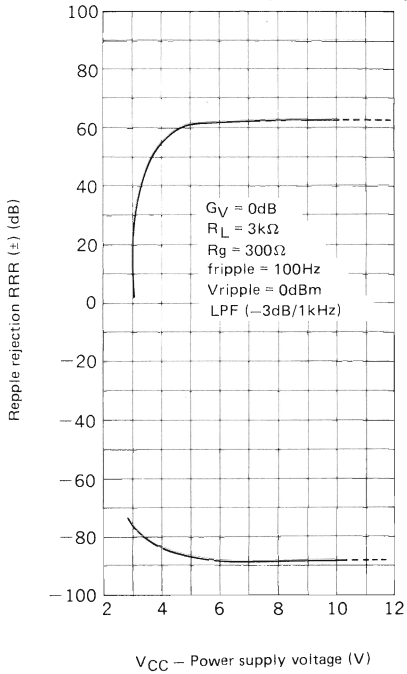
Maximum output voltage vs. Power supply voltage characteristic (Buffer amp)



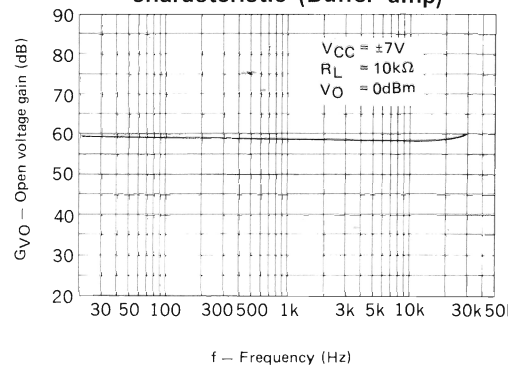
Equivalent noise input voltage vs. Power supply voltage characteristic



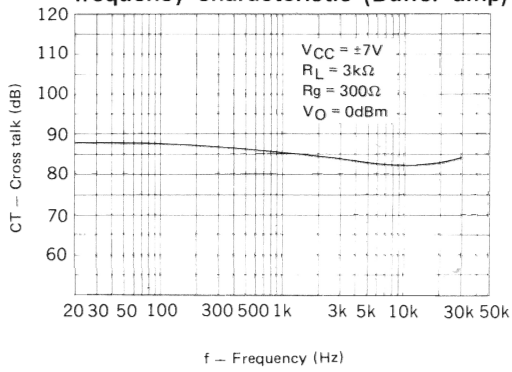
Ripple rejection power supply voltage characteristic (Buffer amp)



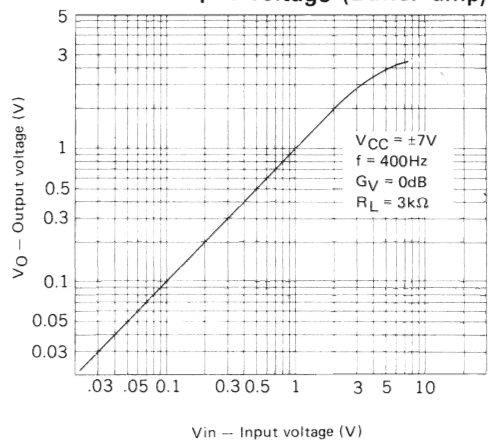
Open voltage gain frequency characteristic (Buffer amp)



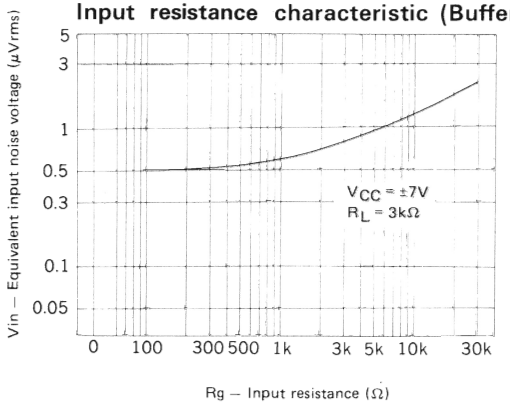
Cross-talk frequency characteristic (Buffer amp)



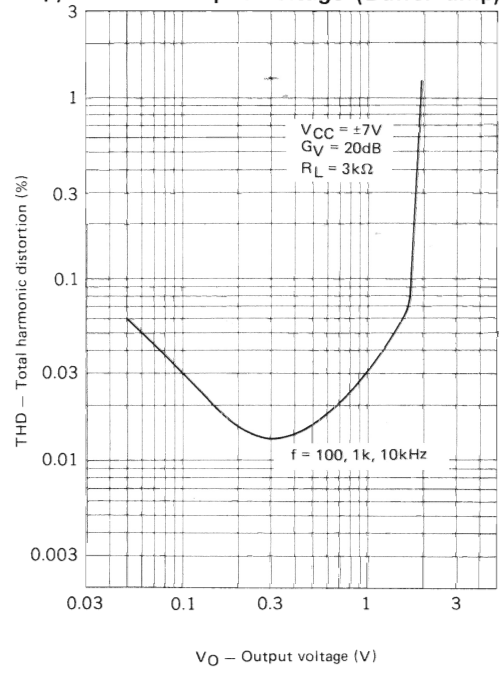
Output voltage vs. Input voltage (Buffer amp)



Equivalent input noise voltage vs. Input resistance characteristic (Buffer amp)



Total harmonic distortion vs. Output voltage (Buffer amp)



Stereo Recording/Playback Preamplifier

Description

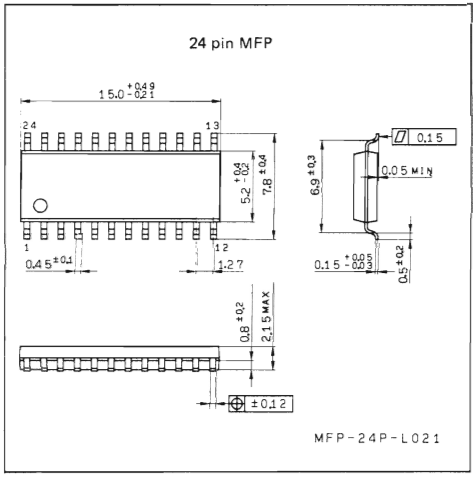
The CX20023 is a recording/playback dual preamplifier system bipolar IC which has been developed for the low voltage operating cassette tape recorder.

Amplifier section
(Recording/playback preamplifier, line amplifier, recording amplifier, each of them having two channels)

System control section
(Ripple filter, LED drive)

Package Outline

Unit: mm



Features

- Easy recording/playback selection
- Has excellent characteristics against the power supply ripples, as a ripple filter is incorporated within
- Incorporates a muting circuit
- Incorporates an LED drive circuit
- The number of external parts is small

Structure

Bipolar silicon monolithic IC

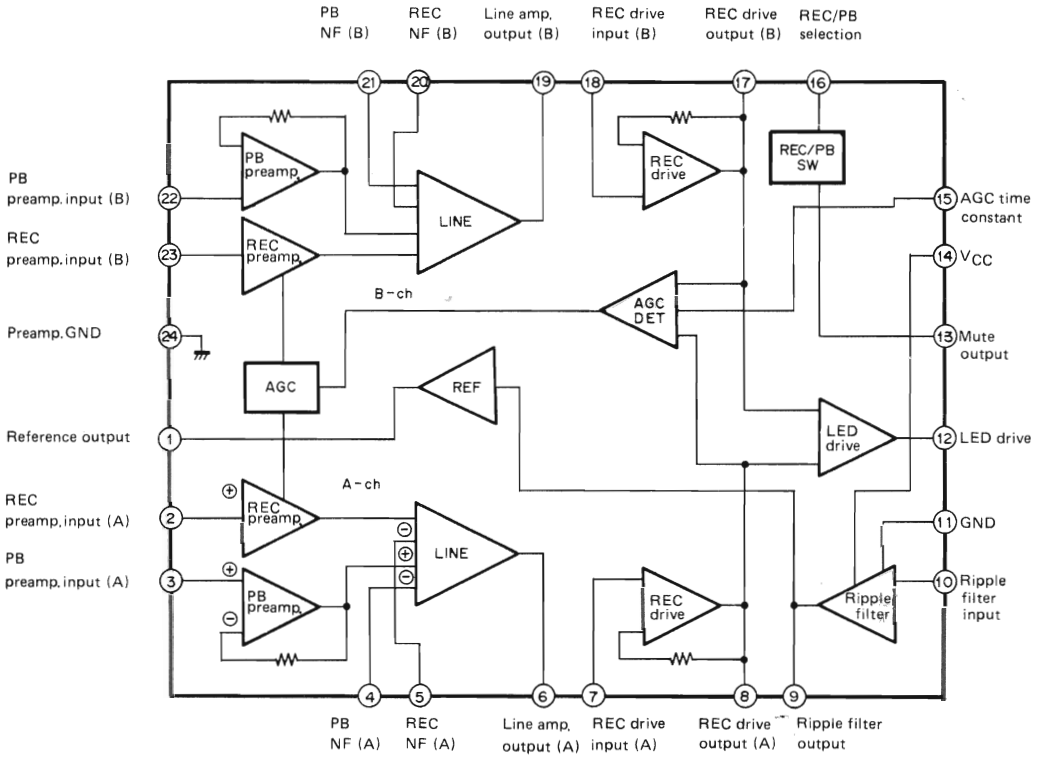
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	670	mW

Recommended Operating Condition

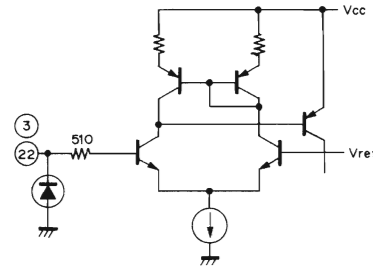
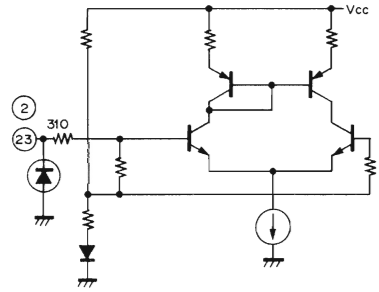
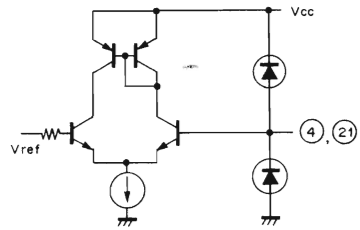
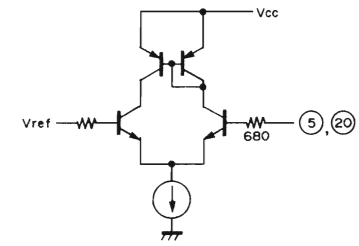
• Supply voltage	V_{CC}	1.6 to 3.5	V

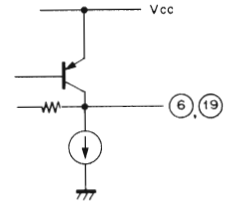
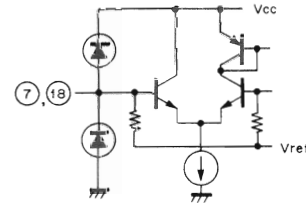
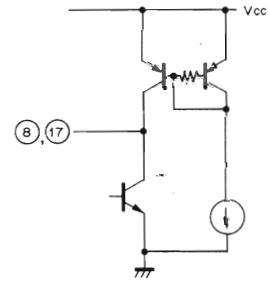
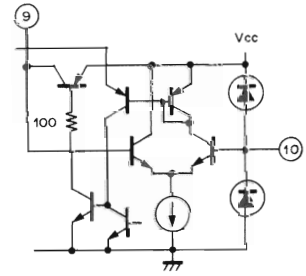
Block Diagram

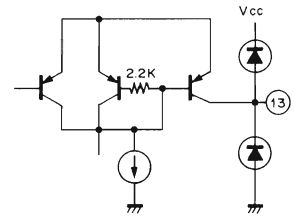
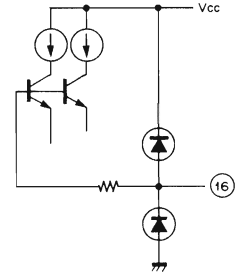
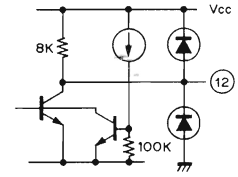
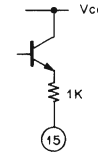


Pin Description and Equivalent Circuit

(Pin voltage is during Vcc=2.3V)

No.	Symbol	Voltage (Typ.)	Description	Equivalent circuit
3 22	PB IN (A) PB IN (B)	1.5V	PB preamplifier input	
2 23	REC-IN (A) REC-IN (B)	1.1V	REC preamplifier input	
4 21	PB-NF (A) PB-NF (B)	1.5V	PB equalizer circuit input pin	
5 20	REC-NF (A) REC-NF (B)	1.5V	REC equalizer circuit input pin	

No.	Symbol	Voltage (Typ.)	Description	Equivalent circuit
6 19	OUT (A) OUT (B)	1.5V	Line amplifier output	
7 18	REC AMP IN (A) REC AMP IN (B)	1.4V	REC drive input	
8 17	REC AMP OUT (A) REC AMP OUT (B)	1.4V	REC drive output	
9 10	NF NF-IN	2.1V 2.1V	Power supply filter time constant pin	

No.	Symbol	Voltage (Typ.)	Description	Equivalent circuit
13	V_{MUTE}	0V	Mute output Pulse is generated when pin 16 is changed from L→H	
16	REC/PB	0V (2.1V)	LED/PB selection During PB=0V During REC=2.1V	
12	LED	1.45V	LED drive Normally both PB/REC are at "H". It becomes "L" when the input is too large during REC and when the BATT voltage is reduced.	
15	AGC	0.9V	AGC time constant	
1	Vref	1.5V	Reference voltage output	

Electrical Characteristics

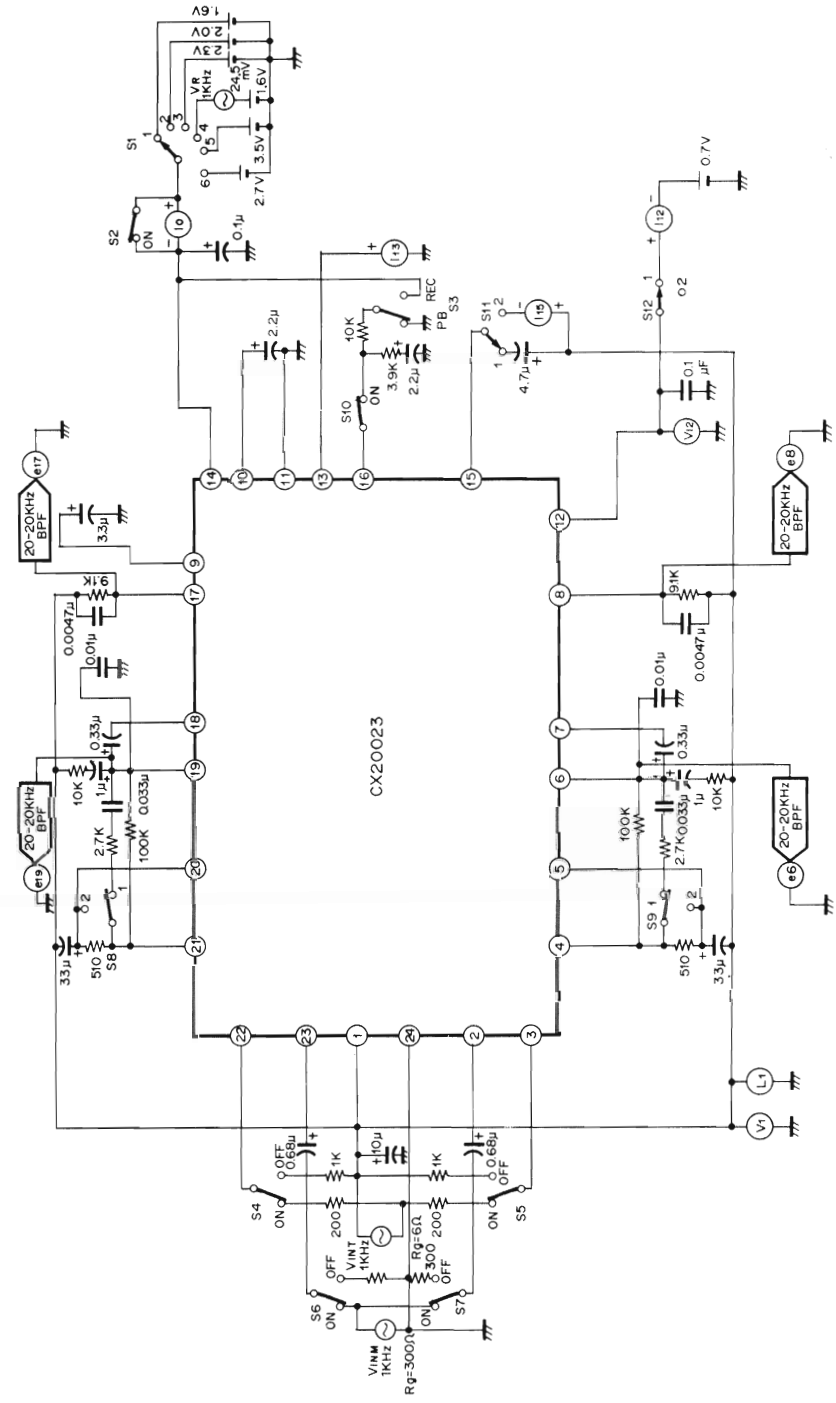
(Ta=25°C, f=1 kHz)

Item	Symbol	SW condition												Input condition			Measuring point	Condition	Min.	Typ.	Max.	Unit
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	V_{INT}	V_{INM}	Unit						
Circuit current (2)	I_{CC} (2)	2	OFF	REC	OFF	OFF	OFF	OFF	1	1	ON	1	2				I_0	V_{CC}=2.0V No signal REC	5.5	10.0	15.5	mA
AGC recovery current	I_{15}	2	ON	REC	OFF	OFF	OFF	OFF	1	1	ON	2	2				I_{15}	V_{CC}=2.0V No signal REC	0.01	0.1	0.4	μA
Circuit current (1)	I_{CC} (1)	2	OFF	PB	OFF	OFF	OFF	OFF	1	1	ON	1	2				I_0	V_{CC}=2.0V No signal PB	4.5	7.0	10.0	mA
Mute current	I_{13}	1	ON	PB	OFF	OFF	OFF	OFF	1	1	OFF	1	2				I_{13}	V_{CC}=1.6V No signal PB	60	90	130	μA
LED current (1)	I_{12} (1)	1	ON	PB	OFF	OFF	OFF	OFF	1	1	ON	1	1				I_{12}	V_{CC}=1.6V No signal PB	70	112	160	μA
Reference voltage (3)	V_1 (3)	1	ON	PB	OFF	OFF	OFF	OFF	1	1	ON	1	2				$V_{1'}$	V_{CC}=1.6V No signal PB	0.84	0.92	1.00	V
Reference voltage (2)	V_1 (2)	5	ON	PB	OFF	OFF	OFF	OFF	1	1	ON	1	2				V_1	V_{CC}=3.5V No signal PB	2.10	2.25	2.40	V
LED current (2)	I_{12} (2)	6	ON	REC	OFF	OFF	OFF	OFF	1	1	ON	1	1				I_{12}	V_{CC}=2.7V No signal REC	130	250	390	μA
LED voltage	V_{12}	6	ON	REC	OFF	OFF	ON	ON	1	1	ON	1	2		24.5	mV	V_{12}	V_{CC}=2.7V V_{INM}=24.5mV 1kHz REC	—	0.1	0.35	V
Reference voltage (1)	V_1 (1)	3	ON	PB	OFF	OFF	OFF	OFF	1	1	ON	1	2				V_1	V_{CC}=2.3V No signal PB	1.25	1.35	1.45	V
Playback voltage gain	PB G_V	1	ON	PB	ON	ON	OFF	OFF	2	2	ON	1	2	14		μV	e_6	V_{CC}=1.6V V_{INT}=14μV 1kHz PB	59	68	77	dB
Playback gain CH balance	PB Δ G_V	1	ON	PB	ON	ON	OFF	OFF	2	2	ON	1	2	14		μV	e_6/e_{19}	V_{CC}=1.6V V_{INT}=14μV 1kHz PB	−1.5	0	1.5	dB

Item	Symbol	SW condition												Input condition			Measuring point	Condition	Min.	Typ.	Max.	Unit
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	V_{INT}	V_{INM}	Unit						
Playback distortion ratio (A)	PB THD (A)	1	ON	PB	ON	ON	OFF	OFF	1	1	ON	1	2	2.2		mV	e_6	V_{CC}=1.6V V_{INT}=2.2mV EQ with PB	—	0.3	1.0	%
Playback distortion ratio (B)	PB THD (B)	1	ON	PB	ON	ON	OFF	OFF	1	1	ON	1	2	2.2		mV	e_{19}	V_{CC}=1.6V V_{INT}=2.2mV EQ with PB	—	0.3	1.0	%
Playback noise (A)	PB V_{NO} (A)	5	ON	PB	OFF	OFF	OFF	OFF	1	1	ON	1	2				e_6	V_{CC}=3.5V BW=20 to 20kHz EQ with PB	—	0.19	0.55	mV
Playback noise (B)	PB V_{NO} (B)	5	ON	PB	OFF	OFF	OFF	OFF	1	1	ON	1	2				e_{19}	V_{CC}=3.5V BW=20 to 20kHz EQ with PB	—	0.19	0.55	mV
Playback ripple output (A)	PB RR (A)	4	ON	PB	OFF	OFF	OFF	OFF	1	1	ON	1	2				e_6	1.6V+V_R V_R=24.5mV PB	—	0.15	0.44	mV
Playback ripple output (B)	PB RR (B)	4	ON	PB	OFF	OFF	OFF	OFF	1	1	ON	1	2				e_{19}	1.6V+V_R V_R=24.5mV PB	—	0.15	0.44	mV
Recording voltage gain (1)	REC G_V (1)	1	ON	REC	OFF	OFF	ON	ON	1	1	ON	1	2		78	mV	e_8	1.6V V_{INM}=78μV REC	61	65	69	dB
Recording gain CH balance	REC Δ G_V (1)	1	ON	REC	OFF	OFF	ON	ON	1	1	ON	1	2		78	mV	e_8/e_{17}	1.6V V_{INM}=78μV REC	−1.5	0	1.5	dB
Recording distortion ratio (A)	REC THD (A)	1	ON	REC	OFF	OFF	ON	ON	1	1	ON	1	2		24.5	mV	e_8	1.6V V_{INM}=24.5mV REC	—	2.5	5.0	%
Recording distortion ratio (B)	REC THD (B)	1	ON	REC	OFF	OFF	ON	ON	1	1	ON	1	2		24.5	mV	e_{17}	1.6V V_{INM}=24.5mV REC	—	2.5	5.0	%
AGC characteristics (1)	V_{OUT} (1)	2	ON	REC	OFF	OFF	ON	ON	1	1	ON	1	2		0.8	mV	e_8	2.0V V_{INM}=0.8mV REC	320	410	520	mV

Item	Symbol	SW condition												Input condition			Measuring point	Condition	Min.	Typ.	Max.	Unit
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	V_{INT}	V_{INM}	Unit						
AGC balance (1)	BL (1)	2	ON	REC	OFF	OFF	ON	ON	1	1	ON	1	2		0.8	mV	e_8/e_{17}	2.0V V_{INM}=0.8mV REC	730	775	820	mV
AGC characteristics (2)	V_{OUT} (2)	2	ON	REC	OFF	OFF	ON	ON	1	1	ON	1	2		24.5	mV	e_8	2.0V V_{INM}=24.5mV REC	388	490	615	mV
AGC balance (2)	BL (2)	2	ON	REC	OFF	OFF	ON	ON	1	1	ON	1	2		24.5	mV	e_8/e_{17}	2.0V V_{INM}=24.5mV REC	690	775	870	mV
Recording noise (A)	REC V_{NO} (A)	5	ON	REC	OFF	OFF	OFF	OFF	1	1	ON	1	2				e_8	3.5V BW=20 to 20kHz REC	—	6.1	13.8	mV
Recording noise (B)	REC V_{NO} (B)	5	ON	REC	OFF	OFF	OFF	OFF	1	1	ON	1	2				e_{17}	3.5V BW=20 to 20kHz REC	—	6.1	13.8	mV
Reference impedance	R REF	5	ON	REC	OFF	OFF	ON	ON	1	1	ON	1	2		24.5	mV	L_1	3.5V V_{INM}=24.5mV REC	—	0.25	0.87	mV
Recording ripple output (A)	REC RR (A)	4	ON	REC	OFF	OFF	OFF	OFF	1	1	ON	1	2				e_8	1.6V+V_R V_R=24.5mV REC	—	62	123	mV
Recording ripple output (B)	REC RR (B)	4	ON	REC	OFF	OFF	OFF	OFF	1	1	ON	1	2				e_{17}	1.6V+V_R V_R=24.5mV REC	—	62	123	mV

Elecerical Characteristic Measuring Circuit



Standard Circuit Design Data

(See the measuring circuit)

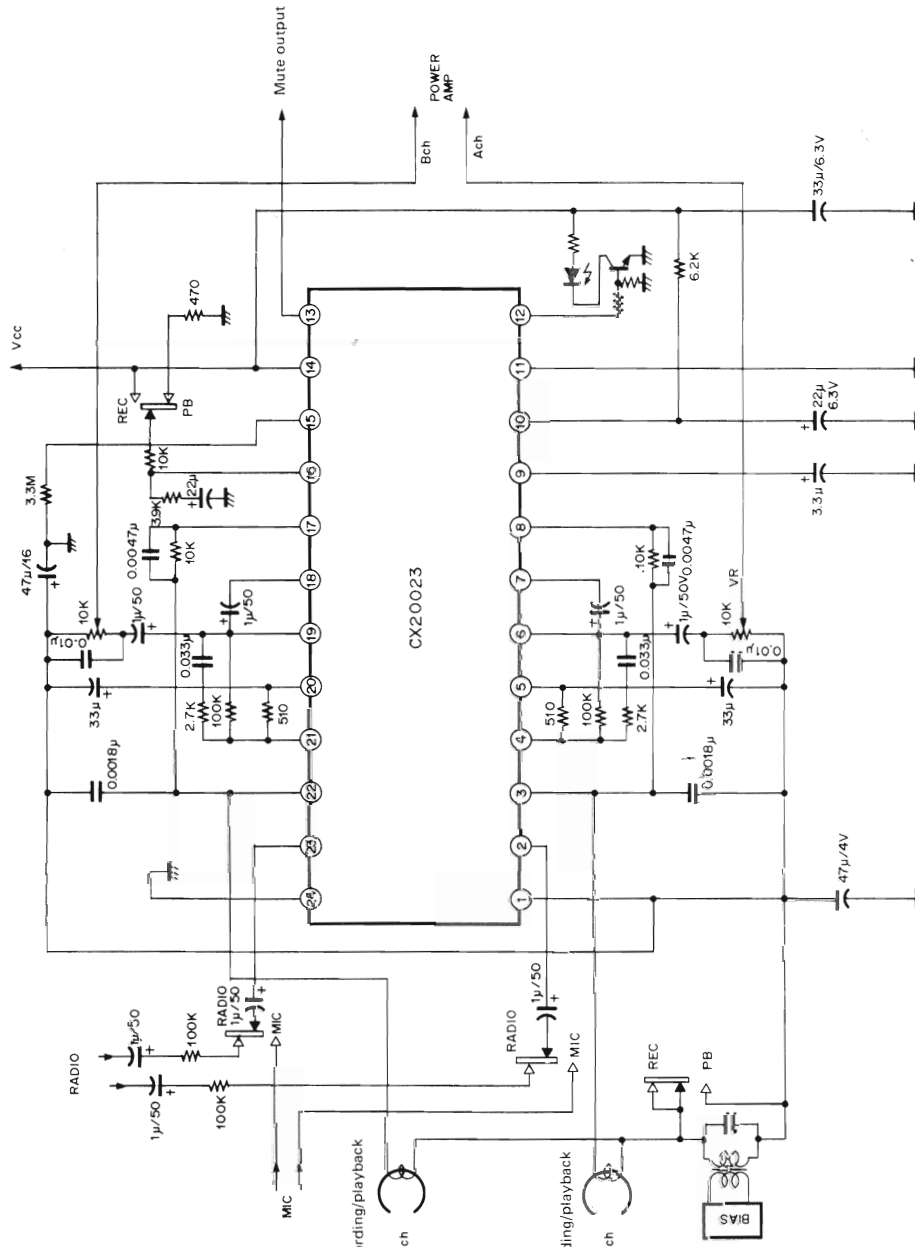
Item	Symbol	Condition	Typ.	Unit
Playback crosstalk B→A	PB CT (A)	V_{CC}=2.0V B-ch V_{INT}=0.35mV PB	0.24	mV
Playback crosstalk A→B	PB CT (B)	V_{CC}=2.0V A-ch V_{INT}=0.35mV PB	0.24	mV
Recording crosstalk B→A	REC CT (A)	V_{CC}=2.0V B-ch V_{INM}=0.78mV REC	4.4	mV
Recording crosstalk A→B	REC CT (B)	V_{CC}=2.0V A-ch V_{INM}=0.78mV REC	4.4	mV
Recording voltage gain (2)	REC G_V (2)	V_{CC}=3.5V V_{INM}=0.078mV REC	67	dB
Recording gain CH balance	REC Δ G_V (2)	V_{CC}=3.5V V_{INM}=0.078mV REC	0	dB
AGC characteristics (3)	V_{OUT} (3)	V_{CC}=3.5V V_{INM}=24.5mV REC	775	mV
AGC balance (3)	BL (3)	V_{CC}=3.5V V_{INM}=24.5mV REC	0	dB

Measuring Condition

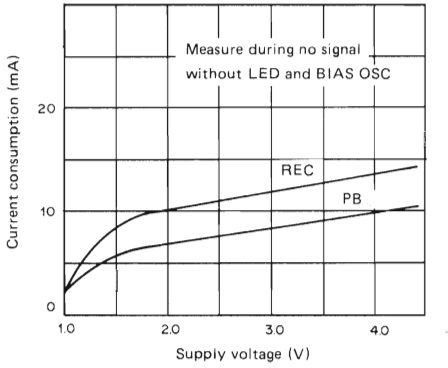
(Ta=25°C, f=1 kHz)

Item	Symbol	SW condition												Input condition			Measurement
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	V_{INT}	V_{INM}	Unit	
Playback crosstalk B→A	PB CT (A)	2	ON	PB	ON	OFF	OFF	OFF	1	1	ON	1	2	0.35		mV	e_6
Playback crosstalk A→B	PB CT (B)	2	ON	PB	OFF	ON	OFF	OFF	1	1	ON	1	2	0.35		mV	e_{19}
Recording crosstalk B→A	REC CT (A)	2	ON	REC	OFF	OFF	ON	OFF	1	1	ON	1	2		0.78	mV	e_8
Recording crosstalk A→B	REC CT (B)	2	ON	REC	OFF	OFF	OFF	ON	1	1	ON	1	2		0.78	mV	e_{17}
Recording voltage gain (2)	REC G_V (2)	5	ON	REC	OFF	OFF	ON	ON	1	1	ON	1	2		0.078	mV	e_8
Recording gain CH balance	REC Δ G_V (2)	5	ON	REC	OFF	OFF	ON	ON	1	1	ON	1	2		0.078	mV	e_8/e_{17}
AGC characteristics (3)	V_{OUT} (3)	5	ON	REC	OFF	OFF	ON	ON	1	1	ON	1	2		24.5	mV	e_8
AGC balance (3)	BL (3)	5	ON	REC	OFF	OFF	ON	ON	1	1	ON	1	2		24.5	mV	e_8/e_{17}

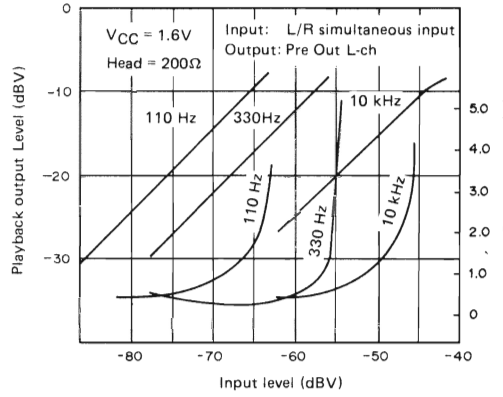
Application Circuit



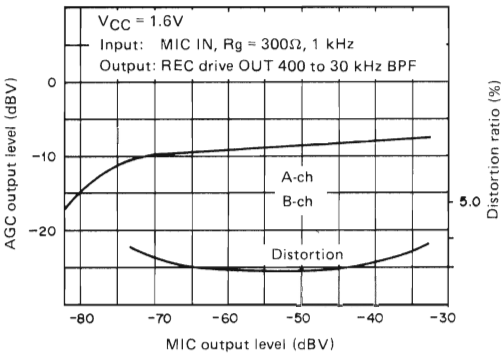
Current consumption vs. Supply voltage



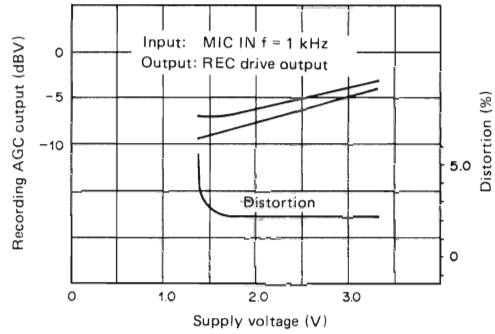
Playback output/input characteristics



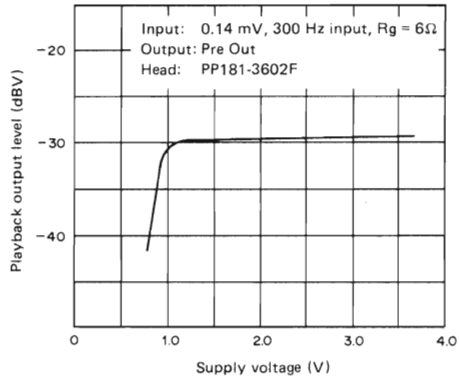
Recording AGC characteristics



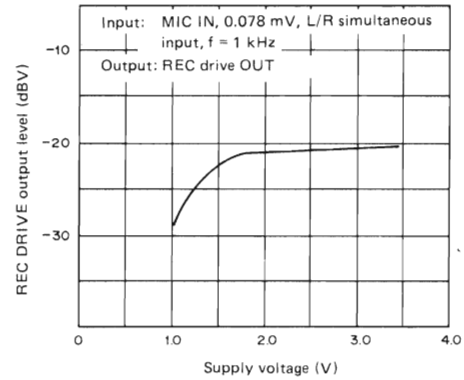
Playback amp. vs. Supply voltage characteristics



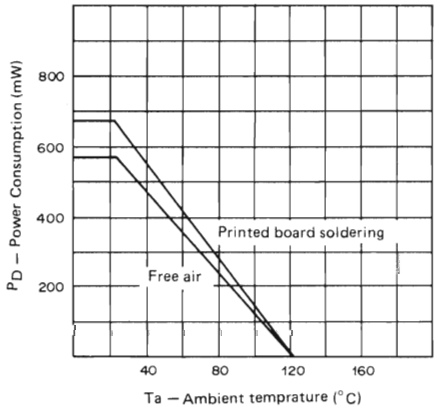
Playback amp. vs. Power supply voltage characteristics



Playback amp. vs. Power supply voltage



Maximum power consumption decreasing curve



SONY

CX20089A

Low-Voltage Power-amplifier

Description

The CX20089A is a low-voltage power amplifier which has been developed for stereo headphone driving. It has function such as headphone driving (32Ω load and gain of 22 dB), POWER (ON/OFF) control pin, and MUTE (ON/OFF) control pin.

Features

- Minimum operating voltage is 0.9V. (Enables to be used for models using a single manganese dry cell)
- Low-power consumption with large output (Typ. 4 mW EIAJ 32Ω load Vcc=1.25V)
- Incorporates a POWER ON/OFF control pin
- Incorporates a MUTE ON/OFF control pin
- Excellent in ripple rejection ratio.

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta=25°C)

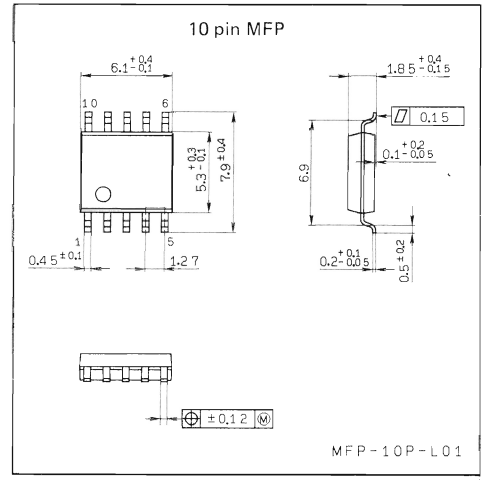
• Supply voltage	Vcc	4.5	V
• Operating temperature	Topr	−1.0 to +60	°C
• Storage temperature	Tstg	−50 to +125	°C
• Allowable power dissipation	PD	377	mW

Recommended Operating Condition

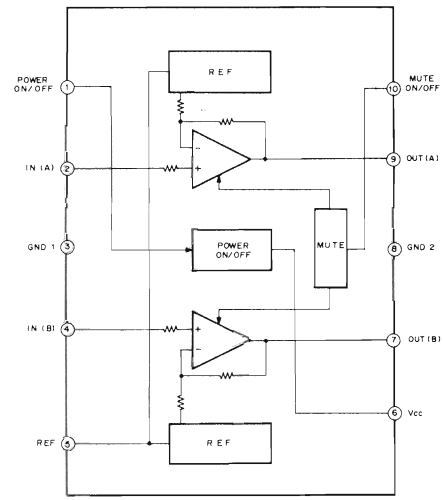
• Supply voltage	Vcc	0.9 to 2.2	V

Package Outline

Unit: mm



Block Diagram



Pin Description

See the Pin voltage electrical characteristic test circuit (Ta=25°C, Power supply voltage 1.25V)

No.	Symbol	Standard voltage (V)	Description
1	POWER ON/OFF	1.25	SW pin which switches the entire REF block ON and OFF. In accordance with it, all the IC functions are turned ON and OFF. H: Vcc and all the functions ON L: GND and all the functions OFF
2	IN (A)	0.7	Input pin of CH (A) AMP. Typical input resistance is 9 kΩ.
3	GND 1	0 (GND)	GND to be connected mainly to the front stage.
4	IN (B)	0.7	Input pin of CH (B) AMP. Typical input resistance is 9 kΩ.
5	REF	0.7	Internal reference voltage output.
6	Vcc	1.25 (Vcc)	Power supply pin.
7	OUT (B)	0.5	Output pin of CH (B).
8	GND 2	0	GND to be connected mainly to output stage.
9	OUT (A)	0.5	Output pin of CH (A).
10	MUTE ON/OFF	0	SW pin which determines the MUTE operation. H: Vcc MUTE. L: GND. Normal operation.

Note) The input impedance is typical 9 kΩ for both A and B CHs with R_L=32Ω.

Electrical Characteristics

See the Electrical Characteristic Test Circuit

(0 dBm=0.775 Vrms, Output loading resistance R_L=32Ω)

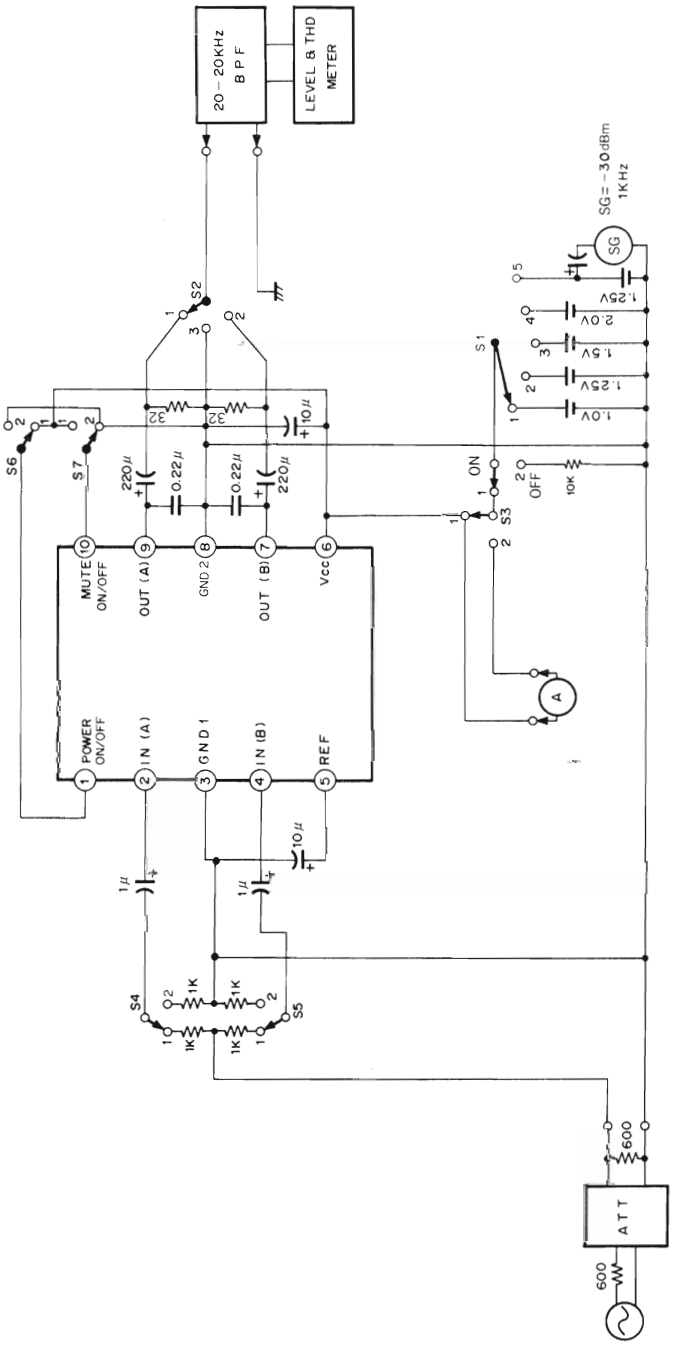
Test item	Symbol	Test condition		Min.	Typ.	Max.	Unit
		Vcc(V)	Condition				
Quiescent current	Icc (ON)	1.25	Without input	2.7	5.5	8.8	mA
Quiescent current	Icc (OFF)	2.00	Connect pin 1 to GND	–	0.1	5.0	μA
Gain 1 (A)	Gain 1 (A)	1.25	−20dBm Output	19.0	22.0	24.0	dB
Gain 1 (B)	Gain 1 (B)	1.25	−20dBm Output	19.0	22.0	24.0	dB
Gain difference 1	ΔGain 1	1.25	−20dBm Output	−1.5	0.0	1.5	dB
Gain difference 1/2 (A)	ΔGain 1/2 (A)	Reduce the voltage to 1.0V from 1.25V	−20dBm Output	0	0.5	1.5	dB
Gain difference 1/2 (B)	ΔGain 1/2 (B)	Reduce the voltage to 1.0V from 1.25V	−20dBm Output	0	0.5	1.5	dB
Total harmonic distortion 1 (A)	THD 1 (A)	1.25	−20dBm Output	–	0.5	2.2	%
Total harmonic distortion 1 (B)	THD 1 (B)	1.25	−20dBm Output	–	0.5	2.2	%
Total harmonic distortion 2 (A)	THD 2 (A)	1.25	−30dBm Output	–	0.5	2.2	%
Total harmonic distortion 2 (B)	THD 2 (B)	1.25	−30dBm Output	–	0.5	2.2	%
EIAJ maximum output (A)	Vmax (A)	1.50	10% THD Output	(335mV) 3.2	(358mV) 4.0	–	mW
EIAJ maximum output (B)	Vmax (B)	1.50	10% THD Output	3.2	4.0	–	mW
Crosstalk (A)	CT (A→B)	1.25	A−ch, −20dBm Output	39	50	–	dB
Crosstalk (B)	CT (B→A)	1.25	B−ch, −20dBm Output	39	50	–	dB

Test item	Symbol	Test condition		Min.	Typ.	Max.	Unit
		Vcc(V)	Condition				
Ripple output voltage (A)	Ripple Out (A)	1.25+ (−30dBm)	Short-circuit the input pin with Rg=1kΩ	−	−72.0	−64.0	dBm
Ripple output voltage (B)	Ripple Out (B)	1.25+ (−30dBm)	Short-circuit the input pin with Rg=1kΩ	−	−72.0	−64.0	dBm
Noise (A)	Noise (A)	2.0	Use 20 to 20kHz BPF Short-circuit the input pin with Rg=1kΩ	−	−85.0	−79.0	dBm
Noise (B)	Noise (B)	2.0	Use 20 to 20kHz BPF Short-circuit the input pin with Rg=1kΩ	−	−85.0	−79.0	dBm
Mute effect (A)	Mute (A)	1.0	Input −20dBm Apply Vcc to pin 10	−	−100.0	−89.0	dBm
Mute effect (B)	Mute (B)	1.0	Input −20dBm Apply Vcc to pin 10	−	−100.0	−89.0	dBm

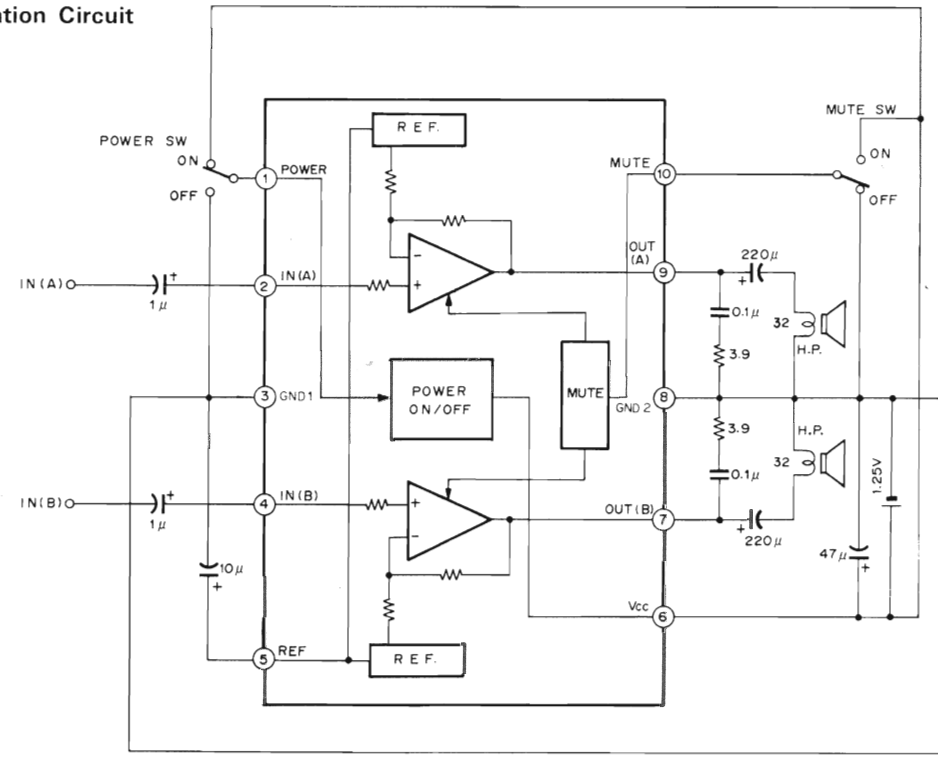
Test Condition

Test item	Symbol	SW condition							
		SW1	SW2	SW3	SW4	SW5	SW6	SW7	ATT
Quiesent current	Icc (ON)	2	1	2	2	2	1	2	–
Quiesent current	Icc (OFF)	4	1	2	2	2	2	2	–
Gain 1 (A)	G1A	2	1	1	1	1	1	2	Variable
Gain 1 (B)	G1B	2	2	1	1	1	1	2	Variable
Gain 2 (A)	G2A	1	1	1	1	1	1	2	Variable
Gain 2 (B)	G2B	1	2	1	1	1	1	2	Variable
Total harmonic distortion ratio 1 (A)	THD 1 (A)	2	1	1	1	1	1	2	Variable
Total harmonic distortion ratio 1 (B)	THD 1 (B)	2	2	1	1	1	1	2	Variable
Total harmonic distortion ratio 2 (A)	THD 2 (A)	2	1	1	1	1	1	2	Variable
Total harmonic distortion ratio 2 (B)	THD 2 (B)	2	2	1	1	1	1	2	Variable
Crosstalk (A)	CT (A→B)	2	1	1	2	1	1	2	Variable
Crosstalk (B)	CT (B→A)	2	2	1	1	2	1	2	Variable
Ripple output voltage (A)	RIP A	5	1	1	2	2	1	2	30dB
Ripple output voltage (B)	RIP B	5	2	1	2	2	1	2	30dB
Noise (A)	NO (A)	4	1	1	2	2	1	2	–
Noise (B)	NO (B)	4	2	1	2	2	1	2	–
Mute effect (A)	Mute (A)	1	1	1	1	1	1	1	20dB
Mute effect (B)	Mute (B)	1	2	1	1	1	1	1	20dB
EIAJ maximum output (A)	Vmax (A)	3	1	1	1	1	1	2	Variable
EIAJ maximum output (B)	Vmax (B)	3	2	1	1	1	1	2	Variable

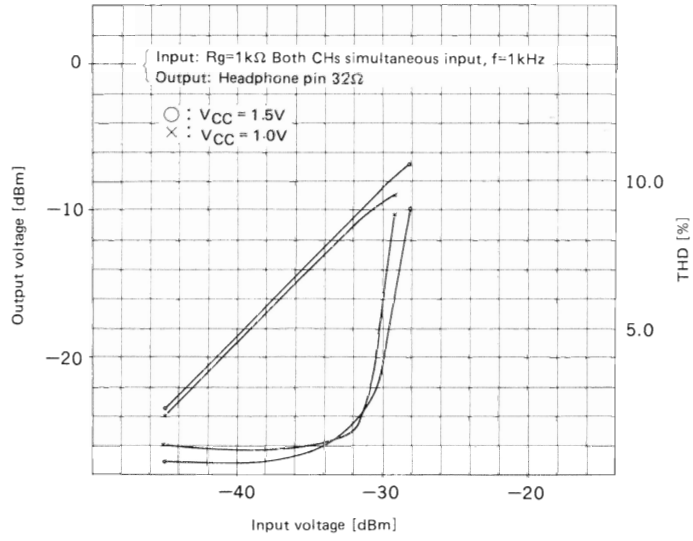
Electrical Characteristics Test Circuit



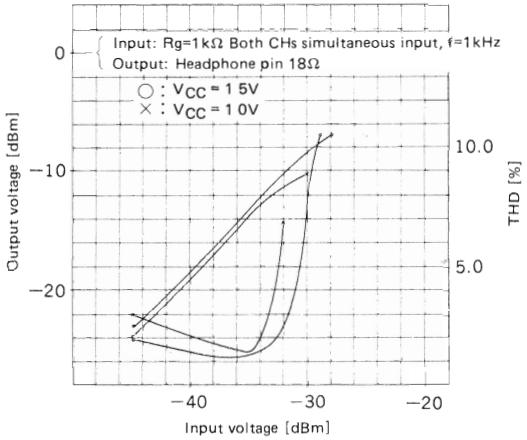
Application Circuit



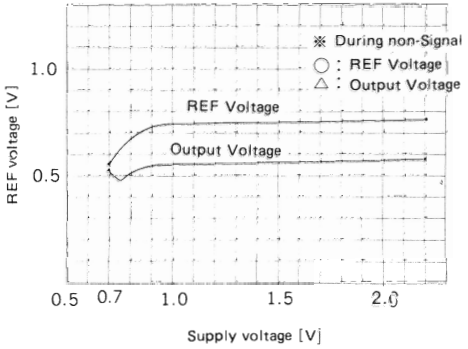
I/O characteristics



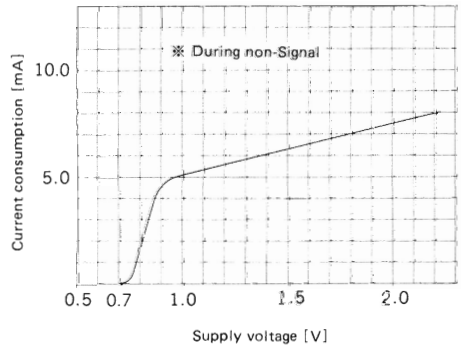
I/O characteristics



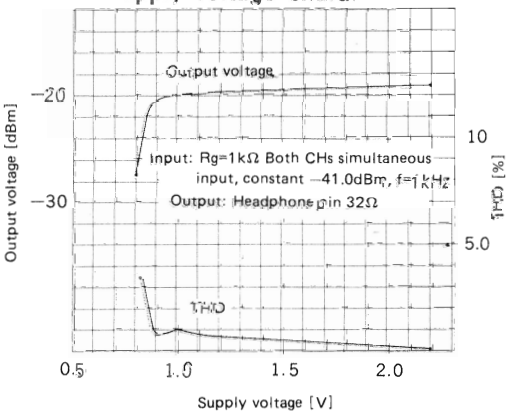
REF voltage/output voltage Supply voltage characteristics



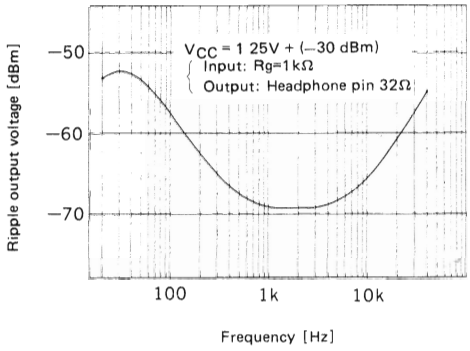
Current consumption Supply voltage characteristics



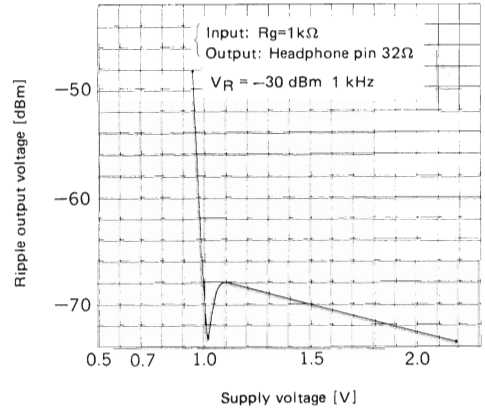
Output voltage and THD Supply voltage characteristics



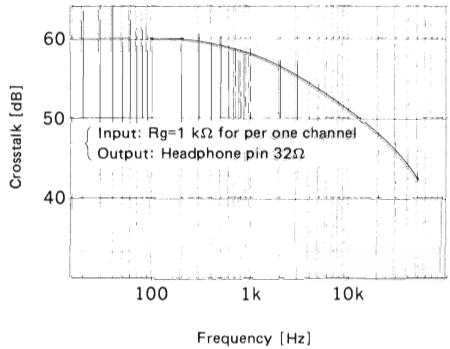
Ripple output voltage frequency characteristics



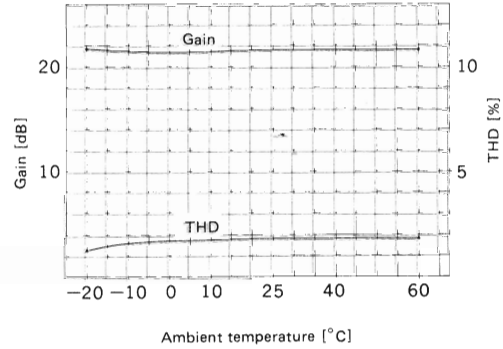
Ripple output voltage Supply voltage characteristics



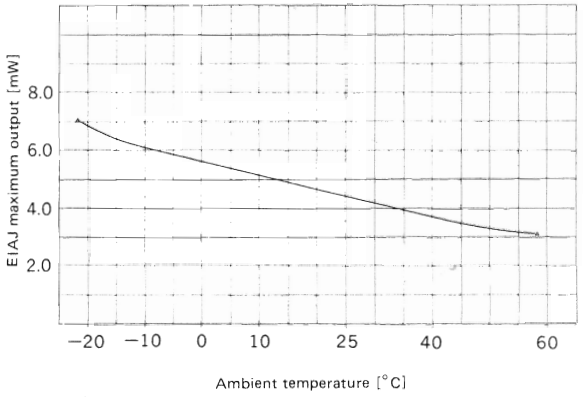
Crosstalk frequency characteristics Vcc=1.25(V)



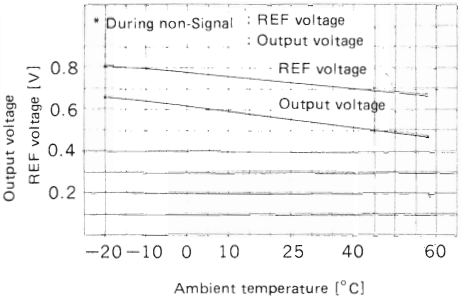
Gain/distortion temperature characteristics



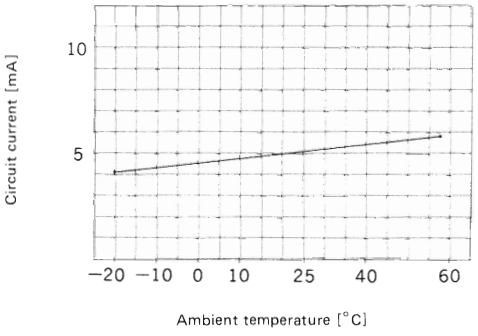
EIAJ maximum output power temperature characteristics



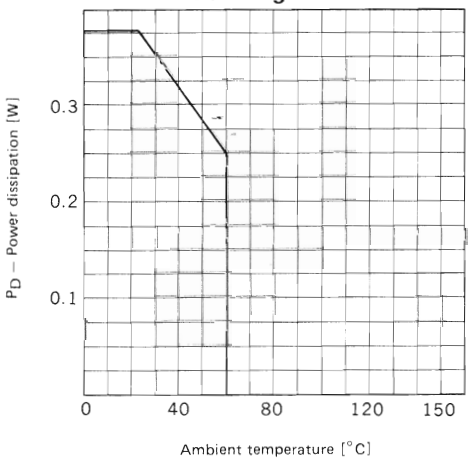
Output voltage/REF voltage temperature characteristics



Quiesent current temperature characteristics



Derating curve



Preamplifier/Power-amplifier

Description

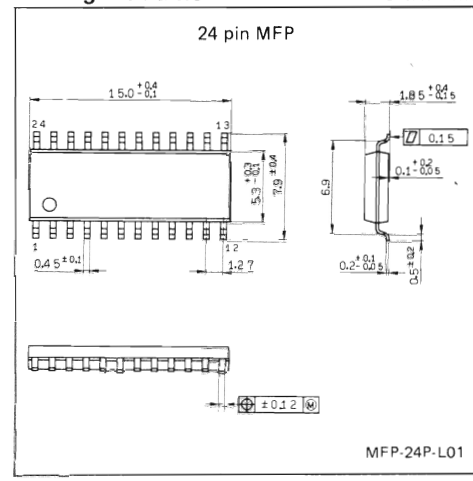
The CX20107 is designed for low voltage portable tape recorder. It integrates monaural recording/playback pre/power amplifier into one chip.

Features

- Large output power 400 mW typical (EIAJ 8Ω load V_{CC}=3V)
- Radio signal recording and playback
- AGC incorporated
- 1.6V Regulator incorporated
- LED Drive Amplifier incorporated
- Excellent ripple rejection

Package Outline

Unit: mm



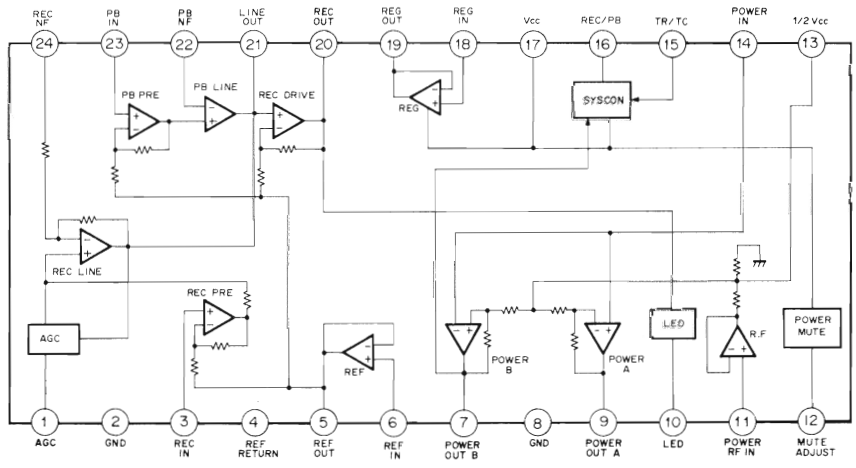
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	4.5	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	780	mW

Recommended Operating Condition

• Supply voltage	V_{CC}	1.8 to 4.2	V

Block Diagram



Pin Description

No.	Name	Description
1	AGC	RC filter between filter connecting pin for AGC and GND connects.
2	GND1	GND for input.
3	REC IN	Input for recording
4	REF RETURN	Filter connecting pin for internal reference voltage. Connects Pin 4 and Pin 5 and connect capacitor between, GND.
5	REF	Internal reference voltage output.
6	REF IN	Internal reference voltage input.
7	OUT (B)	CH (B) power amplifier output.
8	GND2	GND for output.
9	OUT (A)	CH (A) power amplifier output.
10	LED	LED connecting pin. Connects LED between power supply.
11	POWER R.F.IN	Ripple filter connecting pin for power amplifier. Connects capacitor between GND.
12	MUTE ADJUST	MUTE time adjust pin. Connects resistance between GND.
13	1/2 Vcc	Filter connecting pin for internal reference voltage in power amplifier part. Connects capacitor between GND.
14	POWER IN	Power amplifier input.
15	TR/TC	Switch for Radio/Tape recorder.
16	PB/REC	Switch for Playback mode/Recording mode
17	Vcc	Power supply.
18	REG IN	Ripple filter input for internal power supply. Connects capacitor between GND.
19	REG OUT	Output for internal power supply. Connects capacitor between GND.
20	REC DRIVE OUT	Drive amplifier output for recording.
21	LINE OUT	Main signal output.
22	PB NF	Negative feedback pin for playback equalizer.
23	PB IN	Input for playback.
24	REC NF	Negative feedback pin for recording.

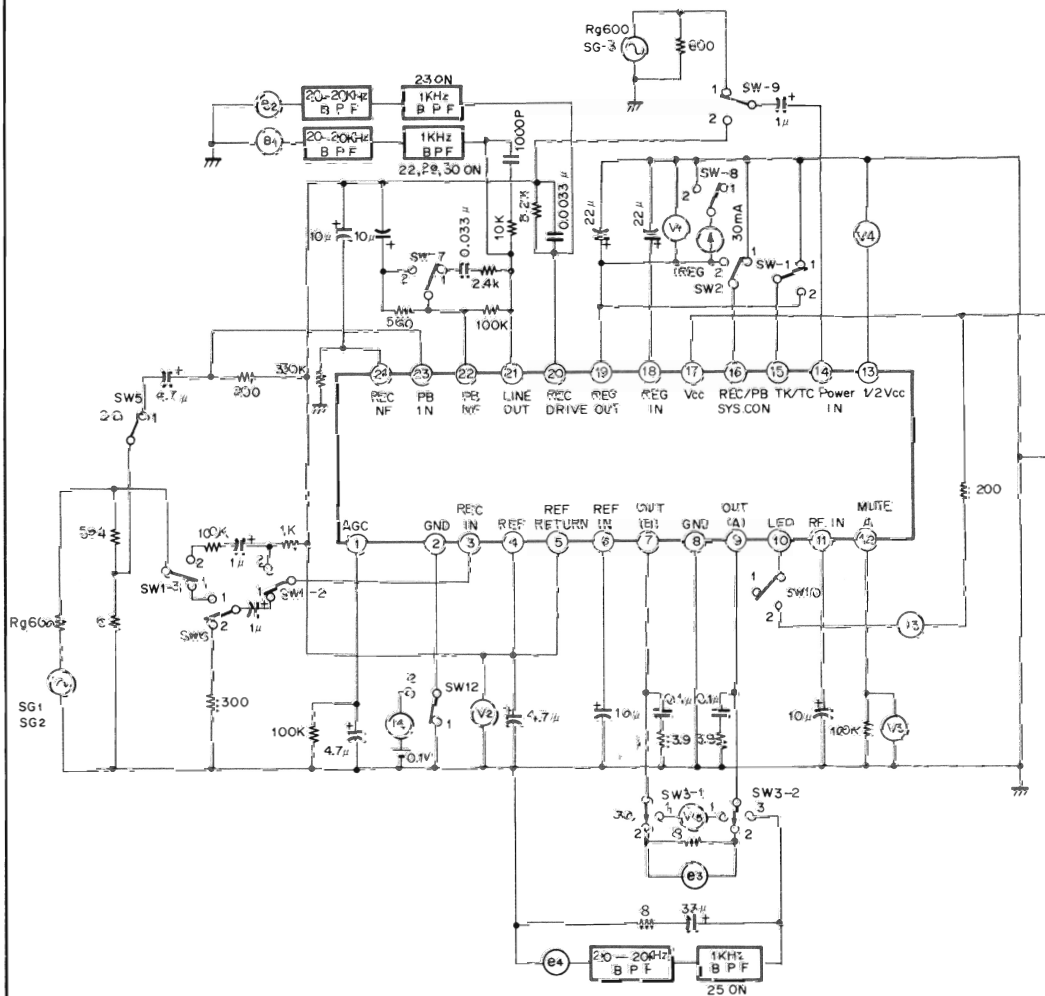
Electrical Characteristic and Test Condition

(Ta=25°C See the Electrical Characteristics Test Circuit)

Test No.	Test Item	Symbol	Switch condition												Bias condition			Test point	Description of output waveform and test method	Min.	Typ.	Max.	Unit
			1	2	3	4	5	6	7	8	9	10	11	12	V_{CC} (V)	Input point	Input level (dBm)						
1	Quiescent current (1)	I_{CC1}	1	1	2	2	2	2	1	1	2	1	3	1	2.5	—	—	I_1		10	16	26	mA
2	Quiescent current (2)	I_{CC2}	1	2	3	2	2	2	1	1	2	1	3	1	2.5	—	—	I_1		9	15	21	mA
3	Regulator output voltage	V_{19}	1	2	2	1	2	2	1	2	2	1	4	1	2.0	—	—	V_1	I_{REG}=30mA	1.26	1.50	1.83	V
4	Reference output voltage	V_4	1	1	2	1	2	2	1	1	2	1	4	1	2.0	—	—	V_2		0.83	1.04	1.22	V
5	MUTE B.W. pin 12 connection check	V_{12}	1	1	2	1	2	2	1	1	2	1	4	1	2.0	—	—	V_3		0.63	0.82	1.10	V
6	1/2V_{CC} B.W. pin 13 connection check	V_{13}	1	1	2	1	2	2	1	1	2	1	4	1	2.0	—	—	V_4		0.81	1.05	1.38	V
7	GND B.W. connection check	I_G	2	2	2	1	2	1	1	1	2	1	7	2	2.0	—	—	I_4		9	24	44	Ω
8	Voltage between power output	V_{7-9}	1	1	1	1	2	2	1	1	2	1	3	1	2.5	—	—	V_5		−54	0	66	mV
9	PB amp open Gain	G_{PB}	1	1	2	1	1	2	2	1	2	1	4	1	2.0	SG1	−90	e_1		66	70	80	dB
10	AGC Characteristic (1)	V_{A-1}	1	2	2	1	2	1	1	1	2	1	4	1	2.0	SG2	−80	e_2		−19	−15	−11	dBm
11	AGC Characteristic (2)	V_{A-2}	1	2	2	1	2	1	1	1	2	1	3	1	2.5	SG2	−60	e_2		−8.5	−5.0	−1.5	dBm
12	AGC Characteristic (3)	V_{A-3}	1	2	2	1	2	1	1	1	2	1	3	1	2.5	SG2	−30	e_2		−6.0	−3.5	−1.0	dBm
13	Power amp Gain	G_{PWR}	1	1	2	1	2	2	1	1	1	1	4	1	2.0	SG3	−37	e_3		25.5	28.0	30.5	dB
14	THD (1)	THD1	1	1	2	1	1	2	1	1	2	1	4	1	2.0	SG1	Vari-able	e_1	Line out=−10dBm output	—	1.0	2.2	%
15	THD (2)	THD2	1	2	2	1	2	1	1	1	2	1	4	1	2.0	SG2	−60	e_2		—	1.0	2.2	%
16	THD (3)	THD3	1	2	2	1	2	1	1	1	2	1	4	1	2.0	SG2	−30	e_2		—	2.0	3.3	%
17	THD (4)	THD4	2	2	2	1	2	2	1	1	1	1	3	1	2.5	SG3	−37	e_3	Turn off SG_1 and SG_2 fully	—	1.0	1.7	%
18	THD (5)	THD5	1	1	3	1	2	2	1	1	1	1	3	1	2.5	SG3	−37	e_4		—	1.0	1.7	%
19	EIAJ Maximum output	V_P	1	1	2	1	2	2	1	1	1	1	2	1	3.0	SG3	—	e_3	THD=10%	330	400	—	mW
20	Noise (1)	N_1	1	1	2	1	2	2	1	1	2	1	1	1	4.0	—	—	e_1	20 to 20kHz BPF	—	−65	−57	dBm

Test No.	Test Item	Symbol	Switch condition												Bias condition			Test point	Description of output waveform and test method	Min.	Typ.	Max.	Unit
			1	2	3	4	5	6	7	8	9	10	11	12	V_{CC} (V)	Input point	Input level (dBm)						
21	Noise (2)	N_2	1	2	2	1	2	2	1	1	2	1	1	1	4.0	—	—	e_2	20 to 20kHz BPF	—	−40	−33	dBm
22	Ripple rejection (1)	R_1	1	1	2	1	2	2	1	1	2	1	6	1	2.0	—	—	e_1	V_R=−20dBm, 1kHz BPF	55	64	—	dB
23	Ripple rejection (2)	R_2	1	2	2	1	2	2	1	1	2	1	6	1	2.0	—	—	e_2	V_R=−20dBm, 1kHz BPF	22	35	—	dB
24	Ripple rejection (3)	R_3	1	1	3	1	2	2	1	1	2	1	6	1	2.0	—	—	e_3	V_R=−20dBm, 1kHz BPF	46	50	—	dB
25	Ripple rejection (4)	R_4	1	1	2	1	2	2	1	1	2	1	6	1	2.0	—	—	e_4	V_R=−20dBm, 1kHz BPF	32	39	—	dB
26	LED current (1)	IL-1	2	1	2	1	1	2	1	1	2	2	3	1	2.5	SG2	−30	I_3		8.5	11	13.5	mA
27	LED current (2)	IL-2	2	2	2	1	2	1	1	1	2	2	3	1	2.5	SG2	−30	I_3		0.9	1.6	2.4	mA
28	LED current (3)	IL-3	1	2	2	1	2	1	1	1	2	2	3	1	2.5	—	—	I_3		5	8	—	mA
29	System controller operation (1)	V_{S-1}	1	2	2	1	2	2	1	1	1	1	5	1	1.6	SG3	0	e_1		—	−86	−80	dBm
30	System controller operation (2)	V_{S-2}	1	1	2	1	2	1	1	1	2	1	5	1	1.6	SG2	−40	e_1	1kHz BPF	—	−42	−38	dBm
31	System controller operation (3)	V_{S-3}	1	2	2	1	1	2	1	1	2	1	5	1	1.6	SG1	−40	e_1	1kHz BPF	—	−71	−61	dBm

Electrical Characteristic Test Circuit



$SW1_{1-3}$	TR/TC	I_1	I_{CC}
SW2	REC/PB	I_2	IREG
$SW3_{1-2}$	EAR/SP	I_3	ILED
SW4	I_{CC}	I_4	IGND
SW5	PB IN	V_1	REG. OUT
SW6	REC IN	V_2	REF. OUT
SW7	GAIN	V_3	MUTE
SW8	IREG	V_4	$1/2V_{CC}$
SW9	Power IN	V_5	Power output A/B
SW10	LED	e1	LINE OUT
SW11	V_{CC}	e2	REC. DRIVE. OUT
SW12	GND 2 Pin	e3	SP
		e4	EAR
		SG_1	TC-PB input (Rg=6Ω)
		SG_2	TC-REC. TR input (Rg=300Ω)
		SG_3	Power. IN (Rg=300Ω)

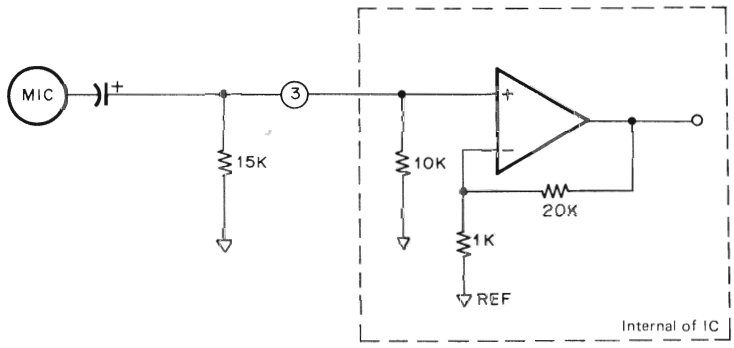
SONY

Description of Operation

① Connect RC filter between filter connecting pin for AGC and GND. Attack time is determined by IC internal resistance R=510(Ω) and external resistance C. Recovery time is determined by external RC.

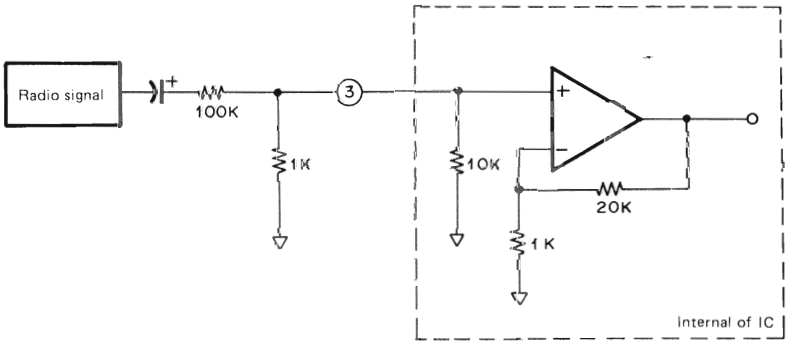
③ REC-IN pin

(i) TC-REC mode (MIC input)



External resistance of 15 kΩ must be connected between pin 3 and REF as in the figure above, because OFF SET occurs in REC AMP output and LED does not light, without external resistance. Therefore input impedance is 6 kΩ.

(ii) TR-REC mode (Radio input)



In oder to prevent distortion at high frequency, an external resistance of 1 kΩ must be connected between pin 3 and REF as shown in the figure above. The reference input of the radio signal is −20 dBm and its level is lowered by 40 dBm with a resistance of 100 kΩ so that the reference input becomes −60 dBm.

④ REF RETURN
Current comes out from REF, goes through filter and returns to IC as reference voltage.

⑤ Internal reference output pin. Low impedence.

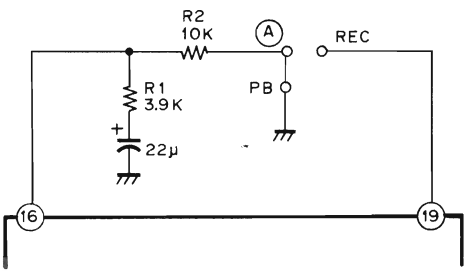
⑩ LED connecting pin
Connects LED with pin 17 V_{CC}. Connects resistance in series in order to protect LED drive transistor.

⑪ Ripple filter pin for Power Amplifier
Capacitor must be connected between GND in order to suppress the ripple.

⑫ POWER MUTE pin
MUTE function operates at power supply rise and put OFF the power amplifier. Then MUTE function is automatically put off and power amplifier is put ON.
Resistance of 100 kΩ must be connected between GND in order to prevent misoperation of MUTE function in high temperature.

⑮ TC/TR mode switch
Connect pin 15 with GND→TC mode
Connect pin 15 with REG OUT 19 →TR mode

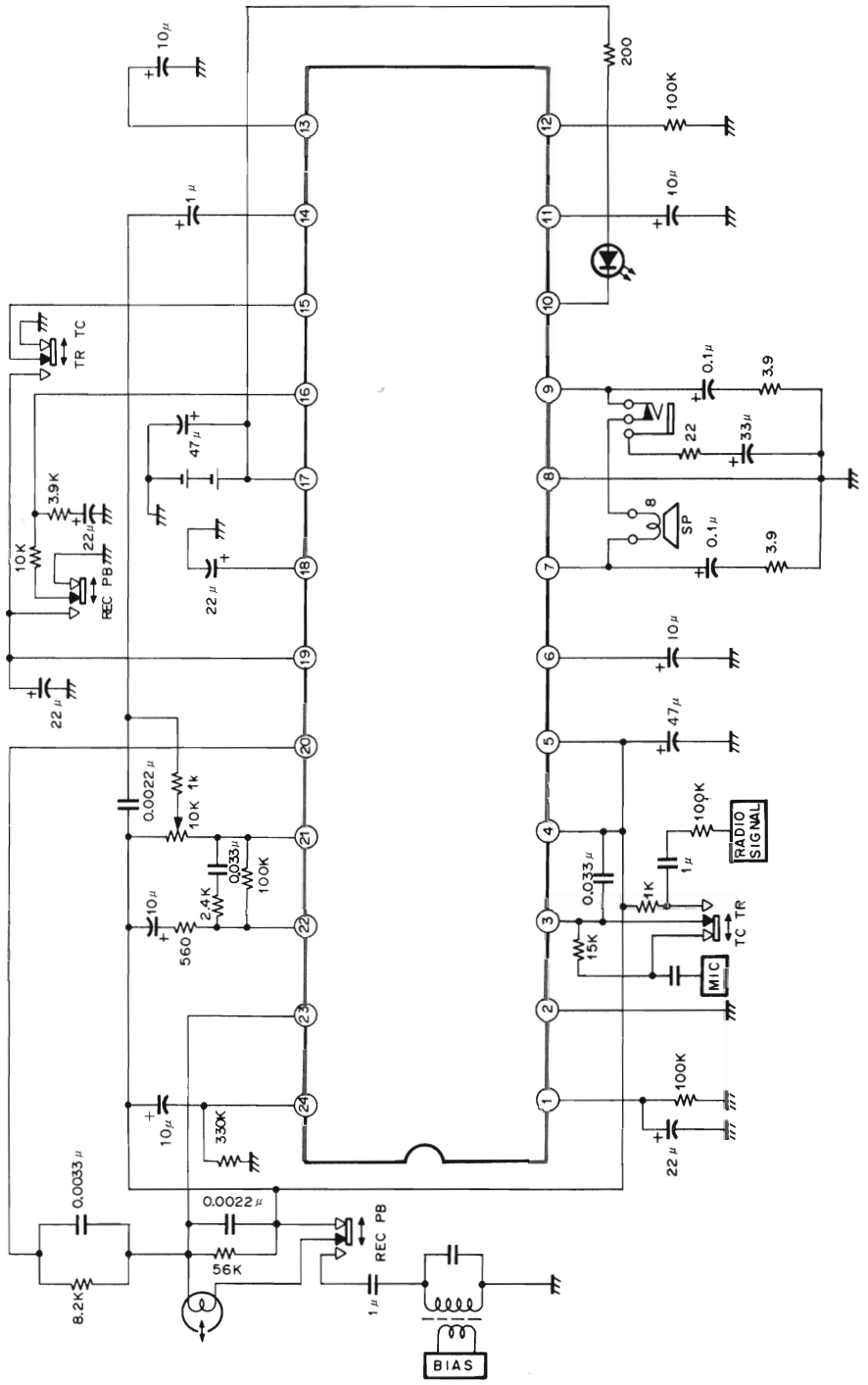
⑯ Connect PB/REC mode switch (pin A in the right figure) with GND→PB mode. Connect pin A with pin 19→REC mode. The moment when PB mode is switched to REC mode, devided voltage value of R1 and R2 is produced in pin 16, and MUTE function operates. Then, it becomes same electrical potential as pin 19, MUTE function is put off and all circuite is switched to REC mode.



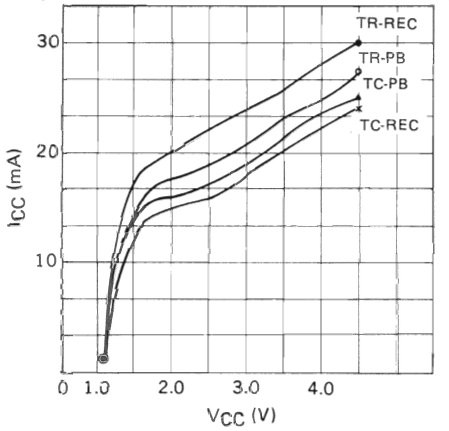
⑲ REG OUT
30 mA current source is available from this pin. In this case, the electrical potential decreases 50 mV. (V_{CC}=2V)

㉔ REC NF
Resistance of 330 kΩ must be connected with GND, in order to reduce OFF SET between pin 24 and pin 20 and prevent LED (TR-PB mode) from unlighting.

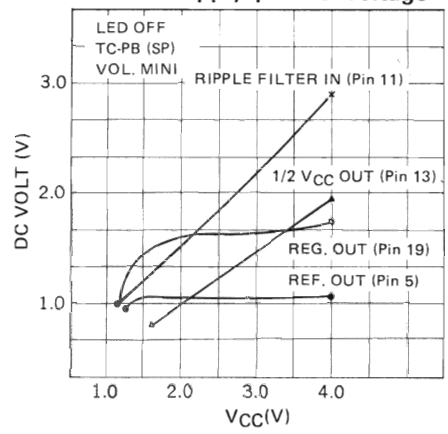
Application Circuit



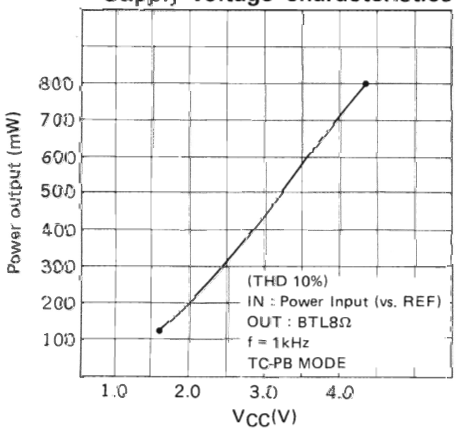
Quiescent current
(With loud speakers, Vol minimum)



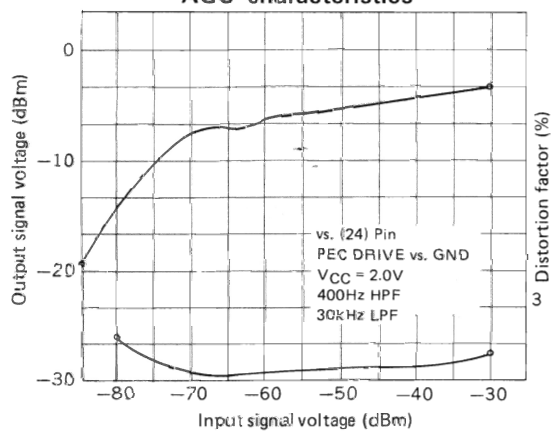
Power supply pin DC voltage



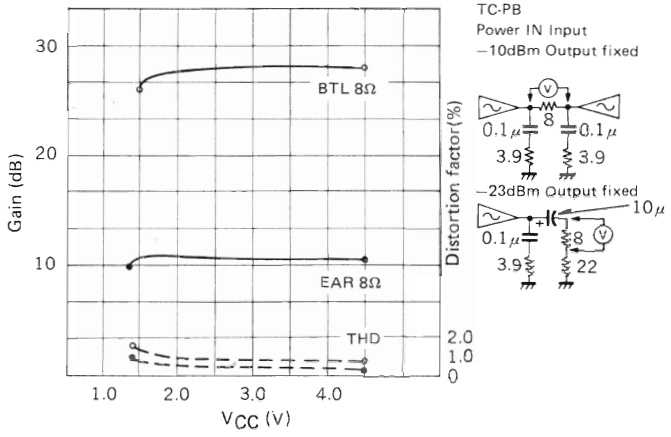
Power output vs.
Supply voltage characteristics



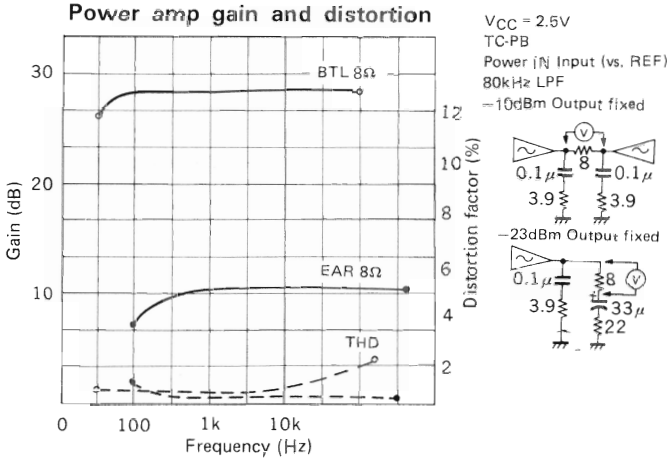
AGC characteristics



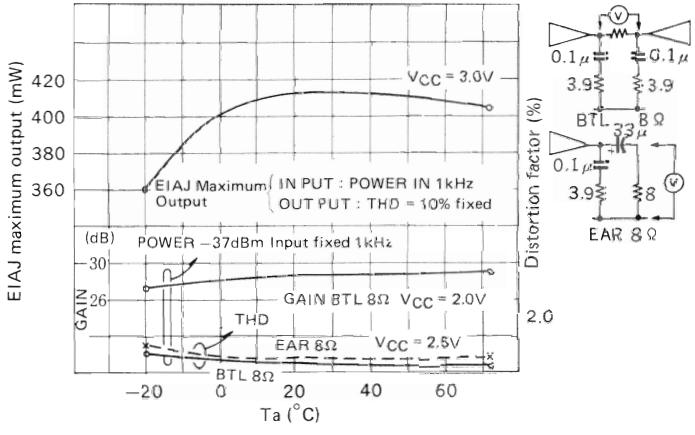
Power amp gain and distortion



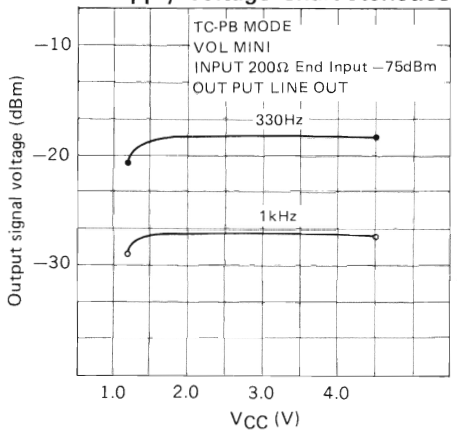
Power amp gain and distortion



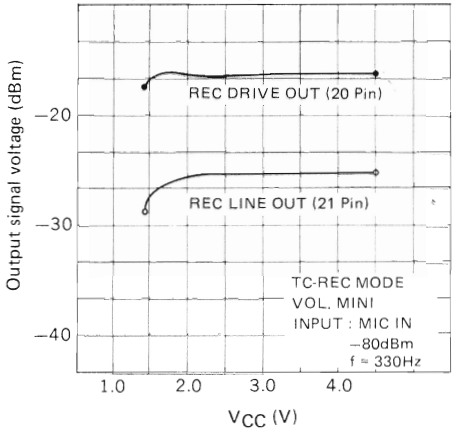
Power output temperature characteristics



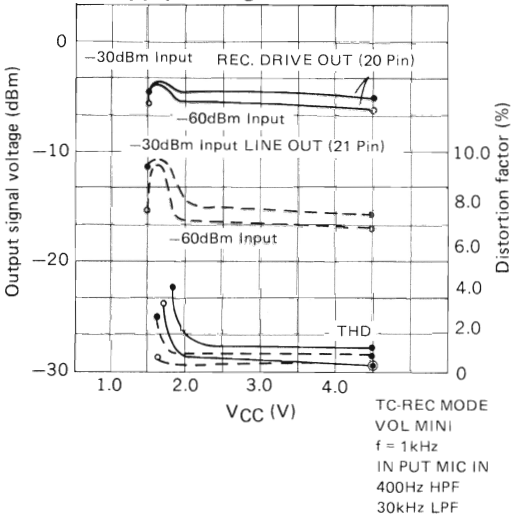
PB amp output voltage vs. Supply voltage characteristics



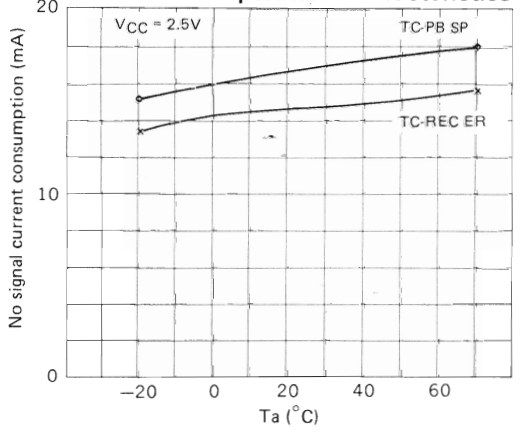
REC amp output voltage vs. Supply voltage characteristics



AGC output voltage vs. Supply voltage characteristics

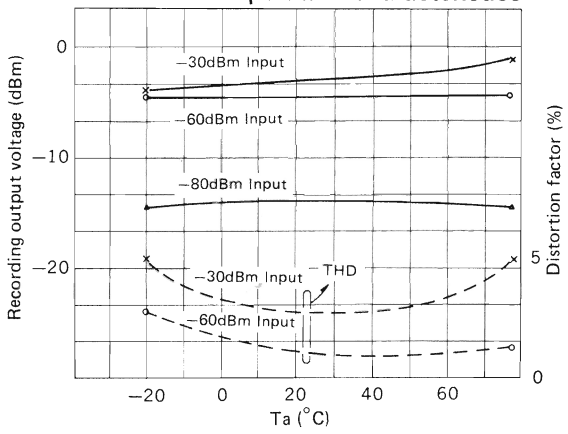


No signal current consumption vs. Temperature characteristics



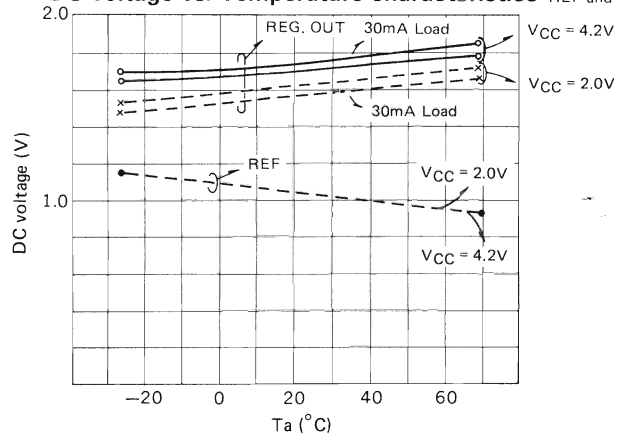
AGC characteristics vs. Temperature characteristics

TC-REC
V_{CC} = 2.0V
RAGC = 100kΩ · CAGC = 22μF



DC voltage vs. Temperature characteristics

REF and REG. OUT



Balanced Transformer-less Dual Amplifier for Audio Use

Description

The CX20172 is a bipolar IC designed as a BTL (balanced transformer-less) amplifier or a DUAL amplifier which can drive an 8Ω load with one dry cell (1.5 V).

Features

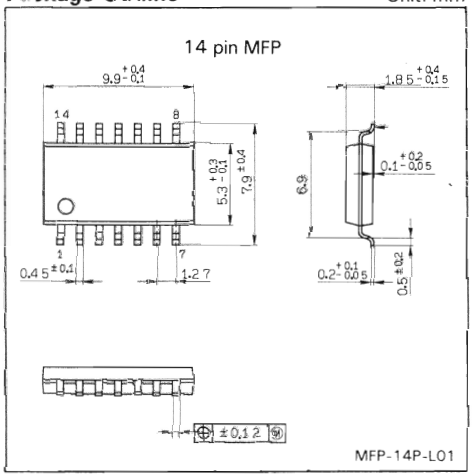
- Operates with one dry cell (operable if Vcc is reduced down to 0.9 V)
- Low power consumption (standard current without signals; 5 mA, 8Ω load, BTL, Vcc=1.25V)
- Large output (BTL: 80 mW/8 Ω, EIAJ;
  DUAL: 21 mW/CH, 8 Ω load, EIAJ;
  Vcc = 1.5 V for both BTL and DUAL)
- The mode of either BTL amplifier or DUAL amplifier, as well as their gain setting, is selected by combining the IC with external components.
- Muting and power ON/OFF functions incorporated.

Structure

Bipolar silicon monolithic IC

Package Outline

Unit: mm



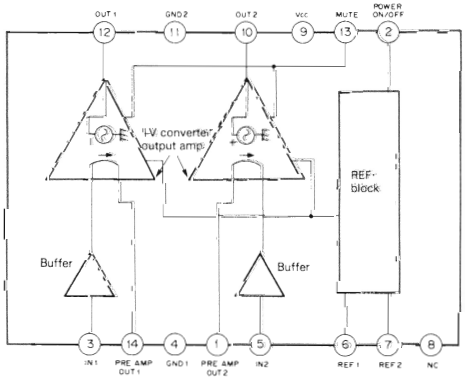
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	4.5	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	560	mW

Recommended Operating Condition

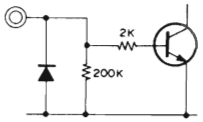
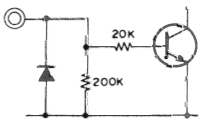
• Supply voltage	Vcc	0.9 to 2.2	V

Block Diagram



Pin Description

(Ta = 25°C, Supply voltage: 1.25 V)

No.	Symbol	Description	Standard pin voltage (V)
1	Pre Amp out 2	Pin to be connected with a load resistor in the preceding-stage buffer amplifier of CH2. See the Electrical Test Circuit application circuit of BTL mode, and DUAL mode.	0.7
2	Power ON/OFF	ON/OFF switching pin for the whole of the IC. H: (power supply) IC ON L: (ground) IC OFF  (standard internal equivalent circuit)	–
3	IN1	Input pin for CH1. This pin is connected to the ground via a coupling capacitor, the same one as used for the input pin, when the pin is not used as an input pin in the BTL mode. Standard input resistance: 10 kΩ	–
4	GND1	Grounding mainly for the preceding stage	–
5	IN2	Input pin for CH2. This pin is connected to the ground via a coupling capacitor, the same one as used for the input pin, when the pin is not used as an input pin in the BTL mode. Standard input resistance: 10 kΩ	0.7
6	REF1	Output pin for internal reference voltage (high impedance) for phase compensation	0.7
7	REF2	Output pin for internal reference voltage (low impedance)	0.7
8	NC		–
9	Vcc	Power supply pin	–
10	OUT2	Output pin for CH2	0.55 (0.74 during MUTE)
11	GND2	Grounding mainly for the output stage	–
12	OUT1	Output pin for CH1	0.55 (0.74 during MUTE)
13	MUTE	Switch pin to activate the MUTE operation H: (power supply) normal operation L: (ground) MUTE  (standard internal equivalent circuit)	–
14	Pre Amp out 1	Pin to be connected with a load resistor in the preceding stage buffer amplifier of CH1. See the Electrical Test Circuit application circuit of BTL mode, and DUAL mode.	0.7

Electrical Characteristics

(Ta = 25°C, See the Electrical Characteristics Test Circuit)

No.	Test Item		Symbol	Switches to be set ON	Power Source I/O Conditions: Supply Voltage V_{CC}	Signal Input V_{IN}	Signal Output V_{OUT}	Test Points	Measurement Method and Contents		Min.	Typ.	Max.	Unit
1	Current consumption 1		I_{ON}	S5	1.25(V)			A METER(DC)	Current consumption in BTL with an 8 Ω load and no signal input		2.5	5.0	11.0	mA
2	Output offset voltage		$V_{\triangle 12}$	S7	↓			V_{OUT}(DC)	CH1 DC Output voltage	(CH1 DC output voltage) − (CH2 DC output voltage) is calculated in BTL with an 8 Ω load	−30	0	+30	mV
				S6	↓			V_{OUT}(DC)	CH2 DC Output voltage					
3	Current consumption 2		I_{OFF}	S3, S4, S5	2.0(V)			A METER(DC)	Current consumptions in Power OFF, MUTE			0	10	μA
4	Gain BTL 1		G_{BTL1}	S1	1.25(V)	Adjustment	−20dBm	V_{IN}, V_{OUT}(AC)	Gain for the output of −20 dBm		23.5	25.5	28.0	dB
5	Gain BTL 2		G_{BTL2}	S2	0.9(V)	↓	↓	↓			22.5	24.5	28.0	dB
6	△Gain BTL		$\triangle G_{BTL}$	Arithmetic	—	—	—	—	$\triangle G_{BTL} = G_{BTL1} - G_{BTL2}$			1.0	3.0	dB
7	THD BTL		T_{HDBTL}	S1	1.25(V)	Adjustment	−10dBm	V_{OUT}(AC)	THD (BTL) for the output of −10 dBm			1.5	2.5	%
8	EIAJ maximum output BTL		P_{BTLMAX}	S1	1.5(V)	↓	THD10%	V_{OUT}(AC)	BTL output for the output THD of 10%		70	82		mW
9	Ripple output voltage BTL		R_{IPBTL}		1.0(V) +(−30dBm)			V_{RIP}, V_{OUT}(AC)	Check the PTL output by overlaying the ripple voltage with 1 V power supply.			−79	−65	dBm
10	Noise output voltage BTL		N_{BTL}		2.0(V)			V_{OUT}(AC)	Noise output voltage in BTL with an 8 Ω load and no signal input			−80	−75	dBm
11	Output during MUTE		M_{BTL}	S1, S4	1.0(V)	−20dBm		V_{OUT}(AC)	BTL output in the MUTE state				−100	dBm
12	Gain DUAL	CH1	G_{DUAL1}	S1, S7, S8, S9, S10, S11, S12	1.25(V)	Adjustment	−26dBm	V_{IN}, V_{OUT}(AC)	CH1 input CH1 output	Gain for individual outputs of −26 dBm. 8 Ω load	19.0	21.0	24.0	dB
		CH2	G_{DUAL2}	S2, S6, S8, S9, S10, S11, S12	↓	↓	↓	↓	CH2 input CH2 output					
13	Channel balance		$\triangle G_{D12}$	Arithmetic	—	—	—	—	$\triangle G_{D12} = G_{DUAL1} - G_{DUAL2}$		−1.5	0	+1.5	dB
14	THD DUAL	CH1	$T_{HD\ D1}$	S1, S7, S8, S9, S10, S11, S12	1.25(V)	Adjustment	−16dBm	V_{OUT}(AC)	CH1 input CH1 output	THD for individual outputs of −16 dBm.		0.9	2.5	%
		CH2	$T_{HD\ D2}$	S2, S6, S8, S9, S10, S11, S12	↓	↓	↓	↓	CH2 input CH2 output					
15	EIAJ maximum output dUAL	CH1	$P_{D1\ MAX}$	S1, S7, S8, S9, S10, S11, S12	1.5(V)	↓	THD10%	↓	CH1 input CH1 output	Output for the individual CH THD's of 10%. 8 Ω load	16	20		mW
		CH2	$P_{D2\ MAX}$	S2, S6, S8, S9, S10, S11, S12	↓	↓	↓	↓	CH2 input CH2 output					
16	Cross talk between DUAL CH'S	CH1 →CH2	C_{TAB}	S1, S6, S8, S9, S10, S11, S12	1.25(V)	Test 12 equivalent to OSC in G_{DUAL1}		V_{IN}, V_{OUT}(AC)	CH1 input CH2 output	The output level at the CH opposite with the input CH		−51	−45	dB
		CH2 →CH1	C_{TBA}	S2, S7, S8, S9, S10, S11, S12	↓	Test 12 equivalent to OSC in G_{DUAL2}		↓	CH2 input CH1 output					

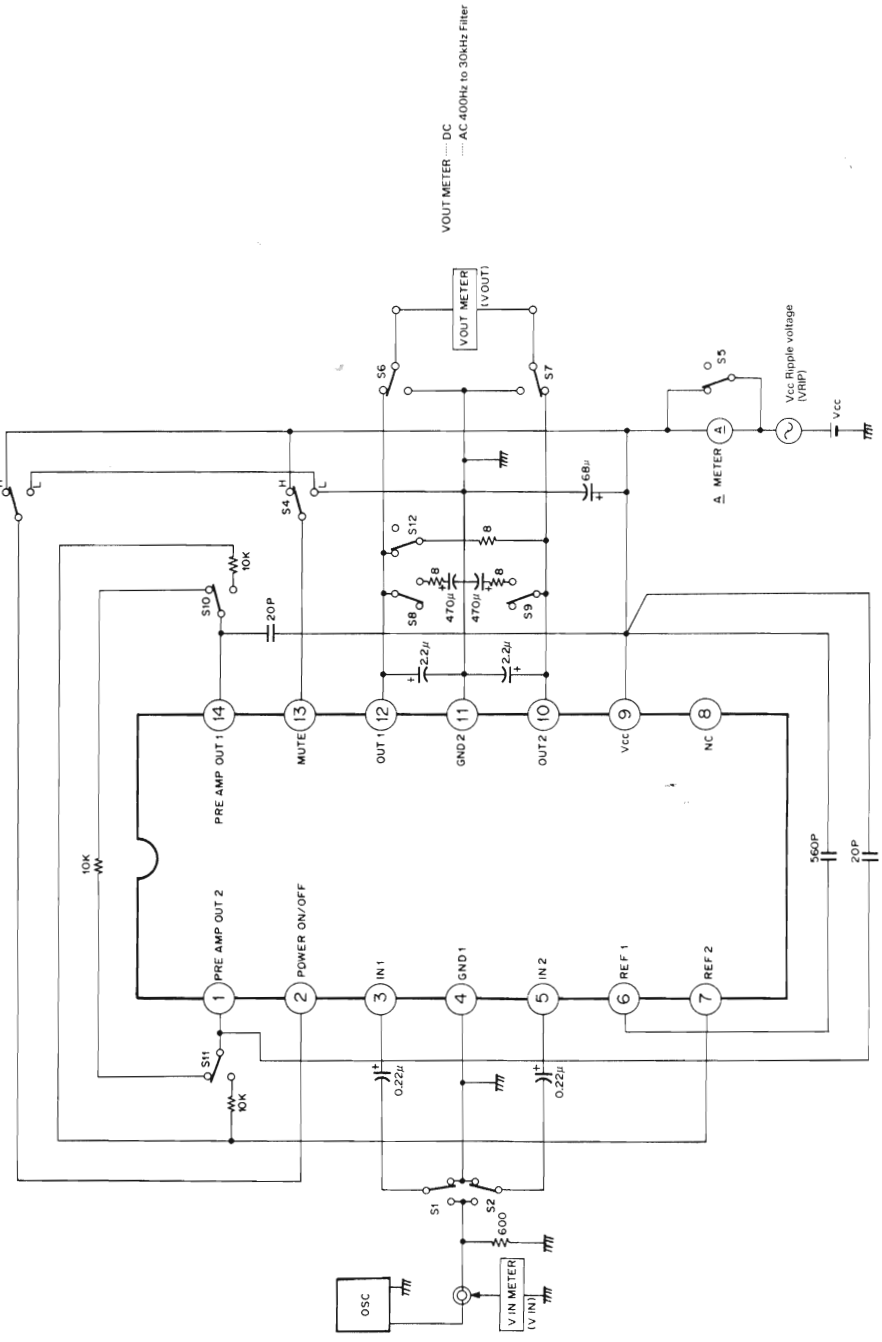
◦ Both signal input V_{IN} and ripple input V_{RIP} are 1 kHz.

◦ dBm (600 Ω) 0 dBm: 774.6mVrms

◦ BPF is set to 400 Hz to 30 kHz for AC measurement.

SONY

Electrical Characteristics Test Circuit



Description of Operation

The CX20172 incorporates two buffer amplifiers in the preceding stage and two current input amplifiers in the succeeding stage. Selection between the BTL amplifier and DUAL amplifier is made by altering the method of attaching external components as shown in the Application Circuit.

1. BTL mode (see the BTL mode Application Circuit)
   - Items 1 to 11 in the Electrical Characteristics are the characteristics for the BTL mode.
   - Input through either IN1 or IN2 results in a reverse-phase output at the output side of the input channel and in the same-phase output at the other, to enable BTL driving of the load between OUT1 and OUT2.
   - Ground the unused input pins via a coupling capacitor which is the same one used for the input pin.
   - Gain setting can be altered by changing values of external resistors connected between Pre Amplifier out 1 and 2. Gain decreases as a resistor value between Pin 1 and Pin 14 increases. Reducing a resistor value to increase the gain results in larger output offset and current consumption. I/O characteristics, distortion factor and maximum output change according to resistor values. Specify a set value, therefore, in view of input level, output level, distortion and power consumption.
   - The value of a phase-compensation capacitor can be altered considerably according to patterns on mounting substrate.

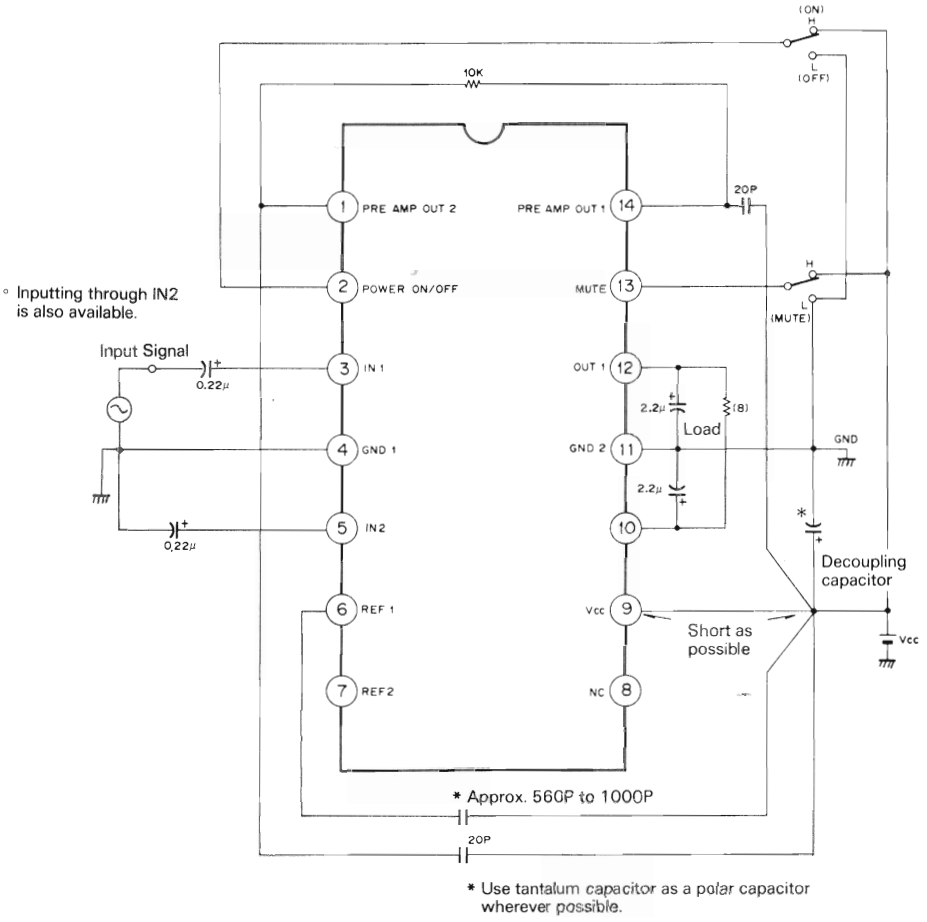
2. Dual mode (see the Dual mode Application Circuit)
   - Items 12 to 16 in the Electrical Characteristics are the characteristics for the Dual mode.
   - Simultaneous input through IN1 and IN2 results in reverse-phase outputs at both output pins to enable DUAL driving.
   - Gain setting can be altered by changing values of external resistors connected between Pre Amplifier out 1 and 2 and REF2, similarly to the BTL mode. Gain decreases as resistor value increases. I/O characteristics, distortion factor and maximum output change according to resistor values. The same consideration as in the BTL mode is, therefore, required. Current consumption has, however, less dependency on the gain than in BTL.
   - The value of a phase-compensation capacitor can be altered considerably according to patterns on mounting substrate.

3. Common functions

3.1 REF block
   - Circuit block to generate reference voltage.
     REF1 (Pin 6) is an output from the block (high impedance). This is reduced in its impedance through the buffer amplifier to generate REF2 (Pin 7).

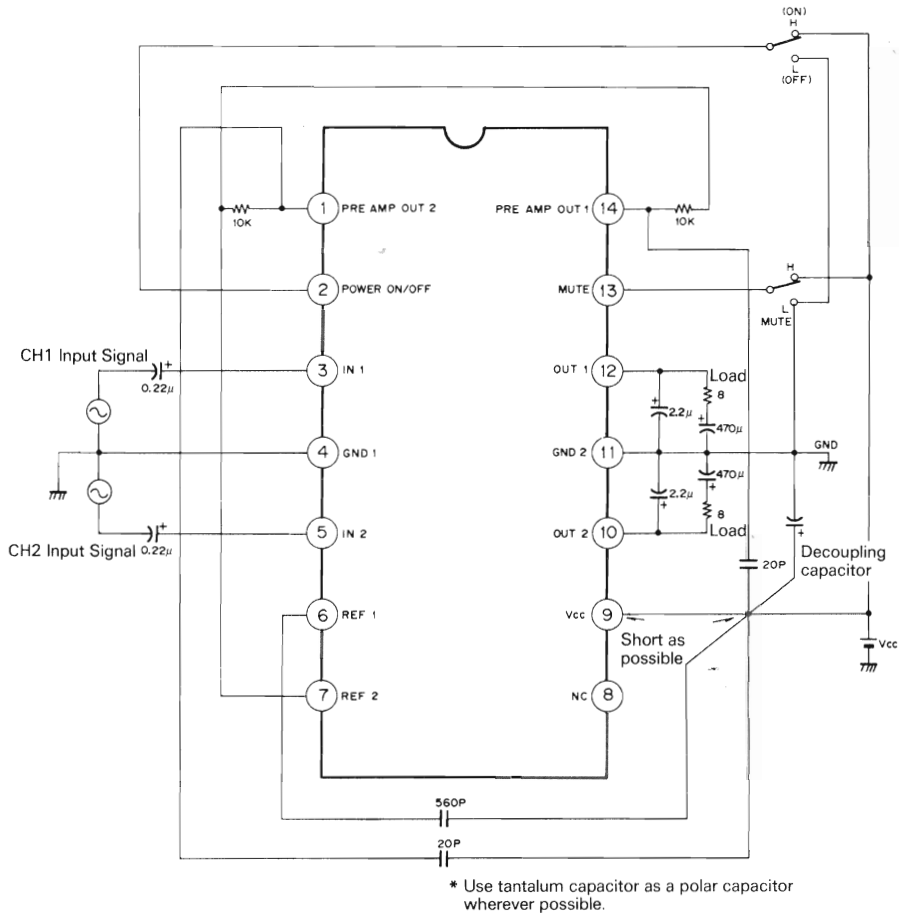
3.2 Mute, Power ON/OFF block
   - Grounding the Mute pin (Pin 13) results in the interrupt of the signal route to generate DC voltage of approx. 700 to 765 mV at both output sides of channel (CH).
   - Grounding the Power ON/OFF pin (Pin 2) results in the OFF state of the REF block and the output is grounded.

BTL Mode Application Circuit



Note) Place a decoupling capacitor between Vcc and GND as close as possible to Vcc and GND2. Assuming this point as the point of power supply or grounding, place (*)-marked components as close as possible.
Values of the decoupling capacitor can be altered according to the pattern layouts.

Dual Mode Application Circuit



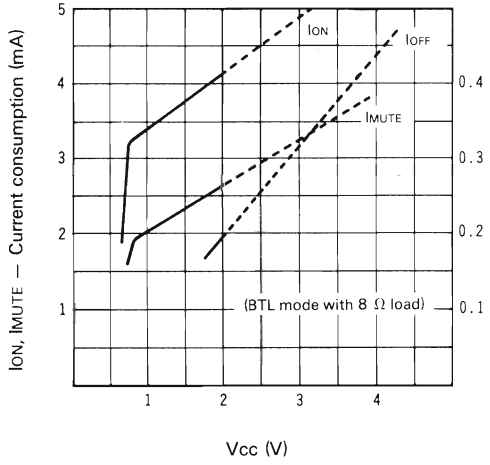
* Use tantalum capacitor as a polar capacitor wherever possible.

Note) Notes for the above are almost same as in BTL.

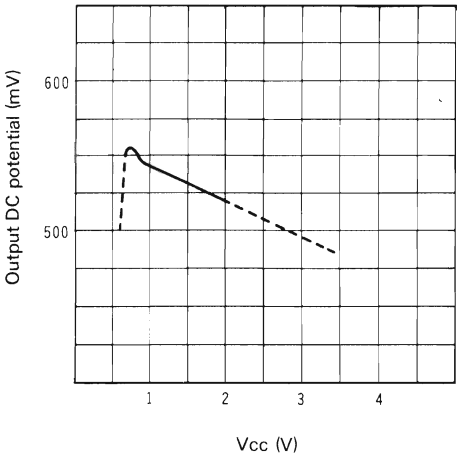
Standard Characteristics

- See "Electrical Characteristics Test Circuit " for the test circuit.
- A resistor between Pin 1 and Pin 14 to determine the gain is of 10 kΩ, unless otherwise specified.
- Measuring temperature is 25°C, unless otherwise specified.

Current consumption ION, IMUTE, IOFF — Vcc

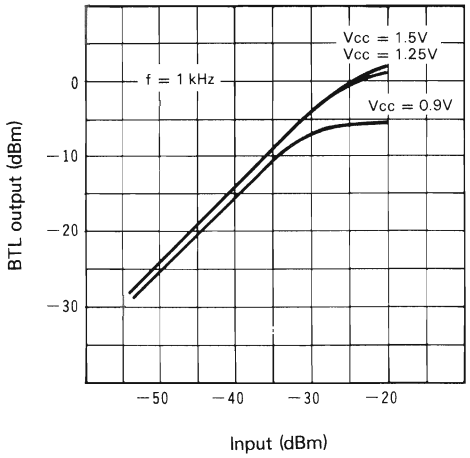


Output DC electric potential — Vcc

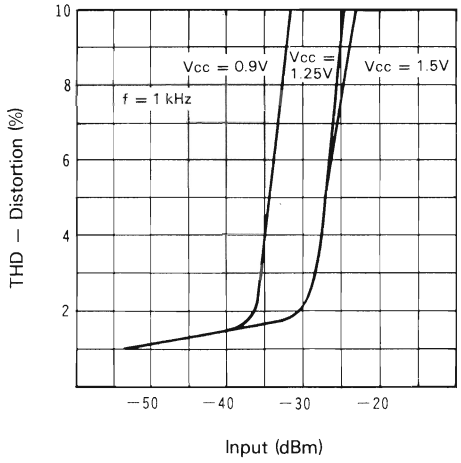


ION and IOFF are measured conforming to the methods in the measurement 1 and 3.
IMUTE represents the current consumption with S4 and S5 ON.

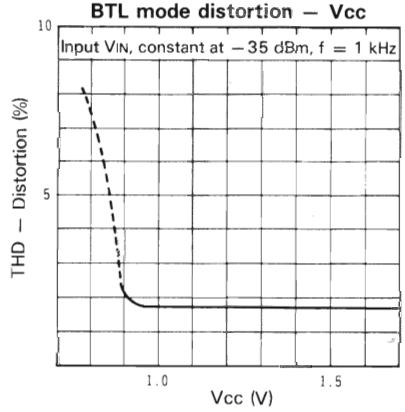
BTL Mode, I/O characteristics (Vcc Parameter)



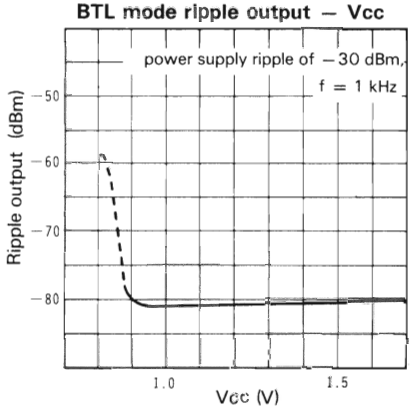
BTL Mode distortion — input level (Vcc Parameter)



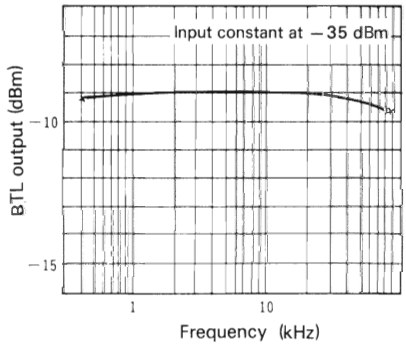
BTL mode distortion — Vcc



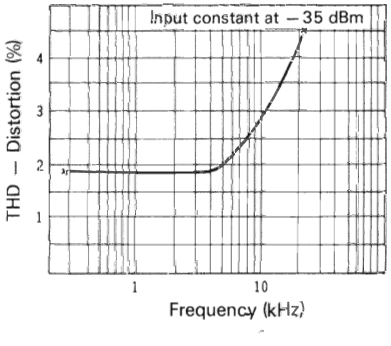
BTL mode ripple output — Vcc



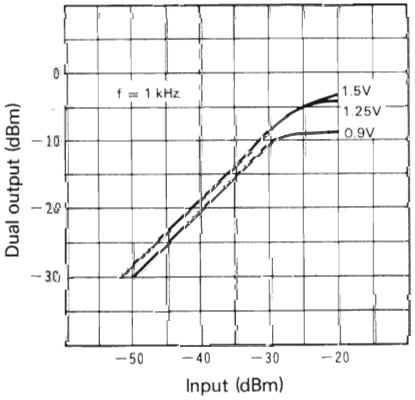
BTL mode output frequency characteristics



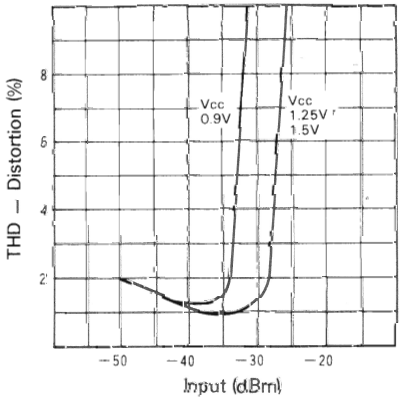
BTL mode distortion frequency characteristics



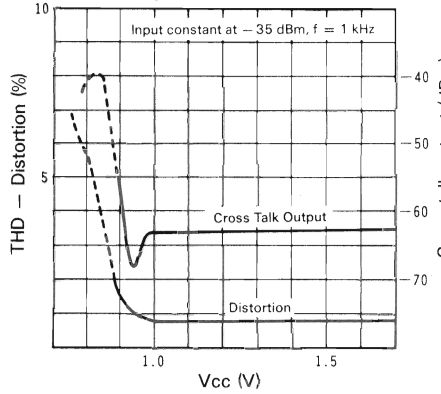
Dual mode I/O characteristics (Vcc Parameter)



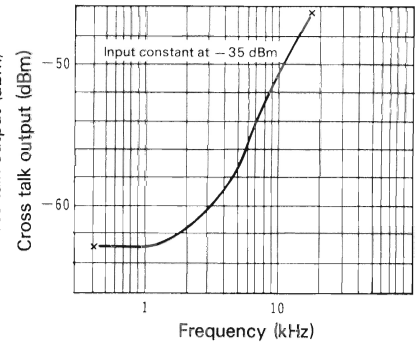
Dual mode distortion — input level (Vcc Parameter)



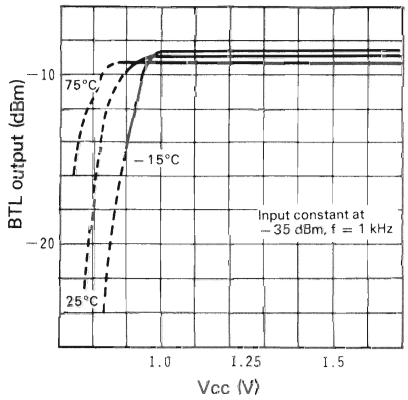
Dual mode distortion — Vcc, Cross talk Vcc 1→2



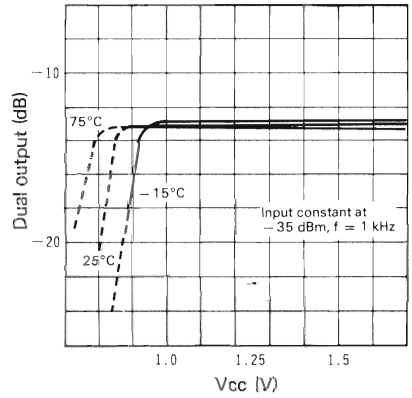
Dual mode cross talk output frequency characteristics



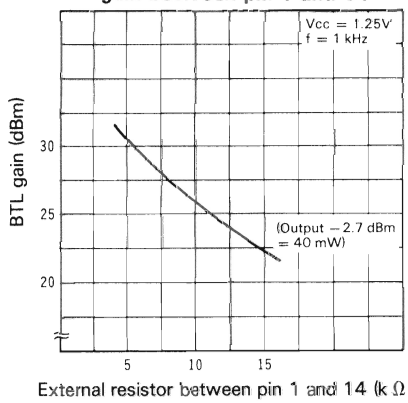
BTL Mode output level — Vcc (Temperature characteristics)



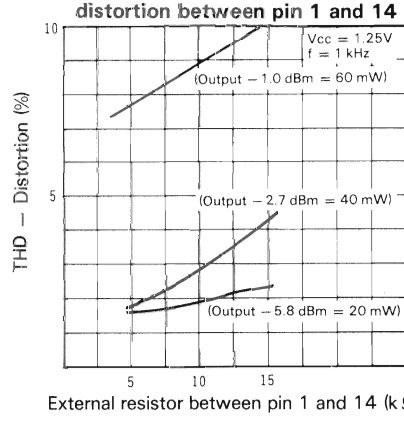
Dual mode output level — Vcc (Temperature characteristics)



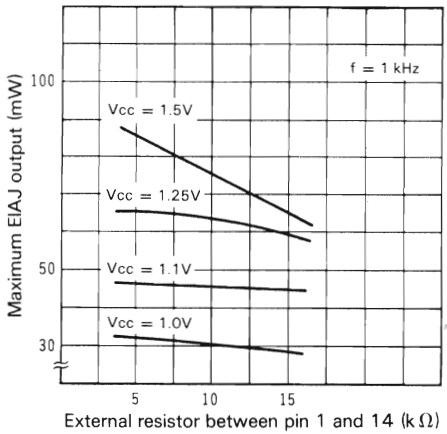
BTL mode external resistance — gain between pin 1 and 14



BTL mode external resistance — distortion between pin 1 and 14



BTL mode external resistance — maximum output between pin 1 and 14



SONY CXA1034P

Stereo Headphone Amplifier

Preliminary

Description

CXA1034P is an IC for stereo headphone player and comprises pre-amplifiers, D.C volume controls, and headphone drivers.

Features

- Wide range of power supply voltage.
- Small number of peripheral components.
- Built-in DC volume controls.

Structure

Silicon Monolithic IC

Absolute Maximum Ratings (Ta=25°C)

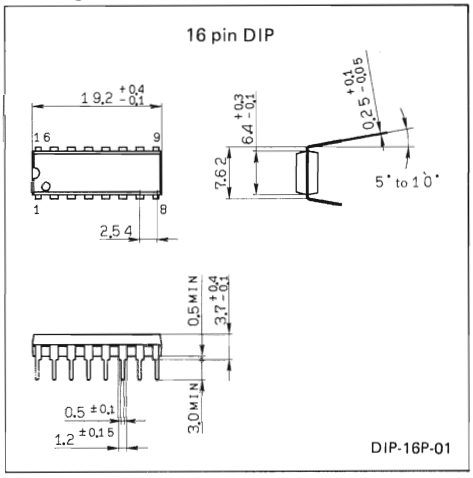
• Supply voltage	V_{CC}	10	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	730	mW

Recommended Operating Condition

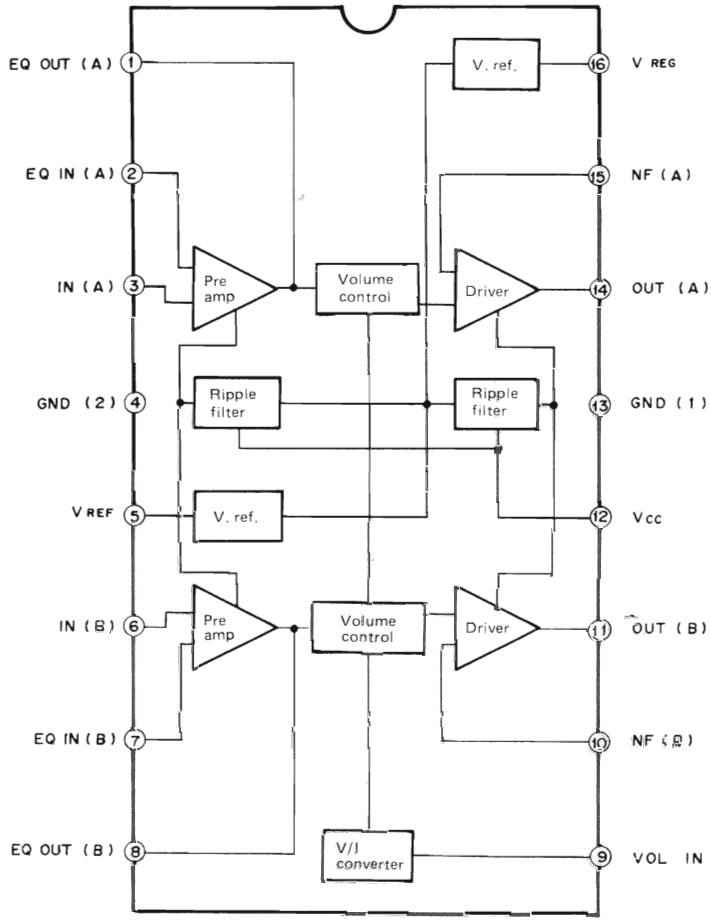
• Supply voltage	V_{CC}	1.8 to 7.5	V

Package Outline

Unit: mm

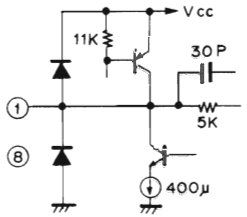
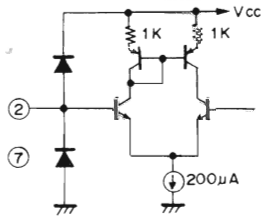
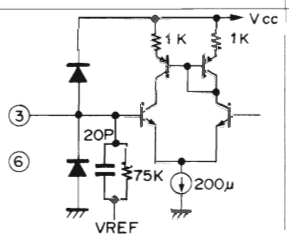
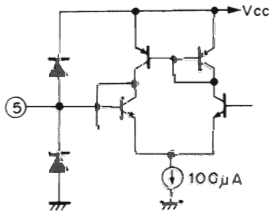
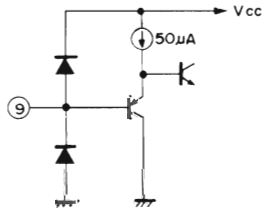


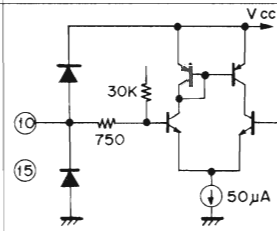
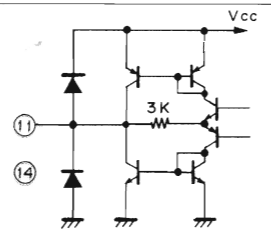
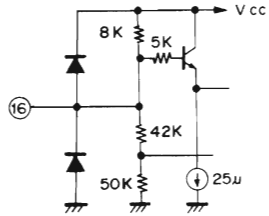
Block Diagram (Top View)



Pin Description

(Vcc=3.0V, no signal)

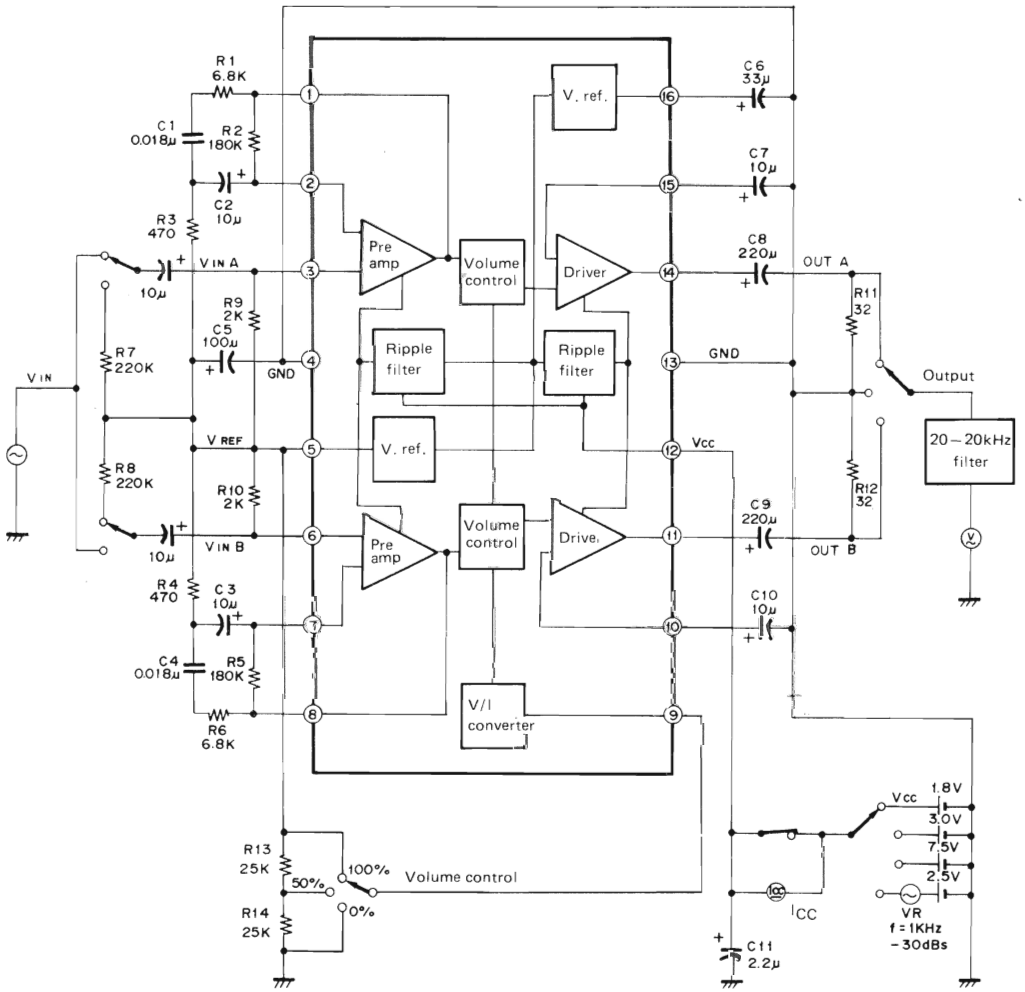
No.	Symbol	Voltage (Typ.)	Equivalent circuit	Description
1 8	EQ OUT (A) EQ OUT (B)	1.6V		Output of preamplifier Output of equalizer circuit
2 7	EQ IN (A) EQ IN (B)	1.5V		Input of equalizer circuit
3 6	IN (A) IN (B)	1.5V		Input of preamplifier
4 13	GND (2) GND (1)	0V		GND (1): GND of pre-amplifier GND (2): GND of driver
5	V_{REF}	1.5V		Reference voltage
6	V_{OL} IN	1.5V		Input of control voltage for volume control

No.	Symbol	Voltage (Typ.)	Equivalent circuit	Description
10 15	NF (B) NF (A)	1.4V		Time constants for filter
11 14	OUT (A) OUT (B)	1.4V		Output of headphone driver
12	V_{CC}	3.0V		Power supply
16	V_{REG}	2.75V		Filter of power supply

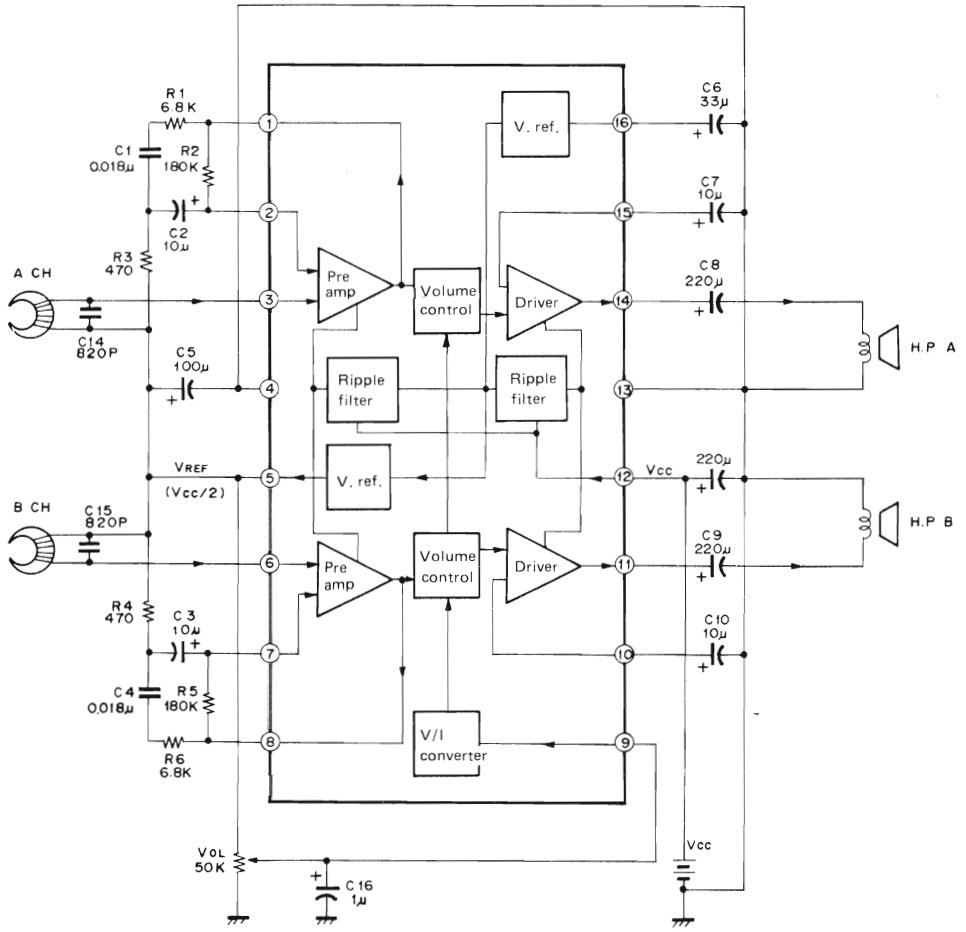
Electrical Characteristics (Ta=25°C, V_{CC}=3V, fo=1 kHz, Volume max. unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current	I_{CC}	No signal	8	11	14	mA
Voltage Gain 1	GV1	V_{IN}=−75dBm	62	65	68	dB
Voltage Gain 2	GV2	V_{IN}=−75dBm Volume 50%	52	55	58	dB
Channel Balance 1	ΔGV1	GV1 (B)/GV1 (A)	−1.5	0	1.5	dB
Channel Balance 2	ΔGV2	GV2 (B)/GV2 (A)	−1.5	0	1.5	dB
Maximum Attenuation	V_{MIN}	V_{IN}=−65dBm	67	75	−	dB
Maximum Power	P_{OMAX}	R_L=32Ω THD=10%	25	30	−	mW
Distortion 1	THD1	V_{IN}=−70dBm	−	0.7	1.2	%
Distortion 2	THD2	V_{IN}−=60dBm Volume 50%	−	0.5	1.0	%
Noise Level	V_{NO}	Rg=2kΩ	−	−55	−50	dBm
Ripple Level	V_R	V_{CC}=2.5V ΔV_R=−30dBm		−55	−50	dBm
Crosstalk	V_{CT1}	V_{IN}=−65dBm Rg=2kΩ		−60	−55	dBm

Test Circuit

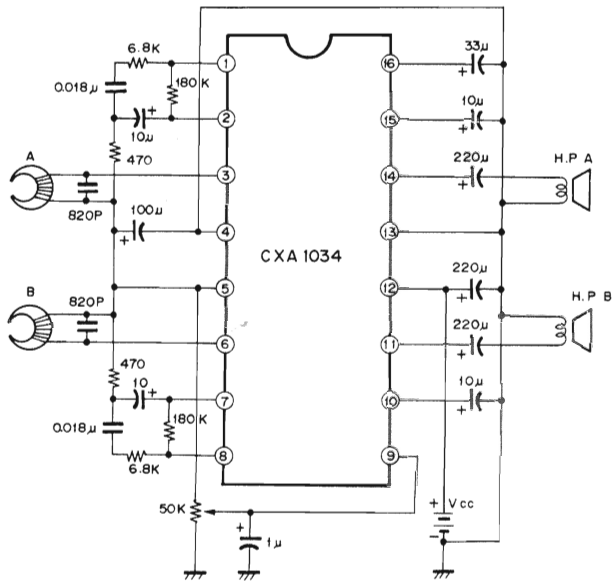


Application Circuit

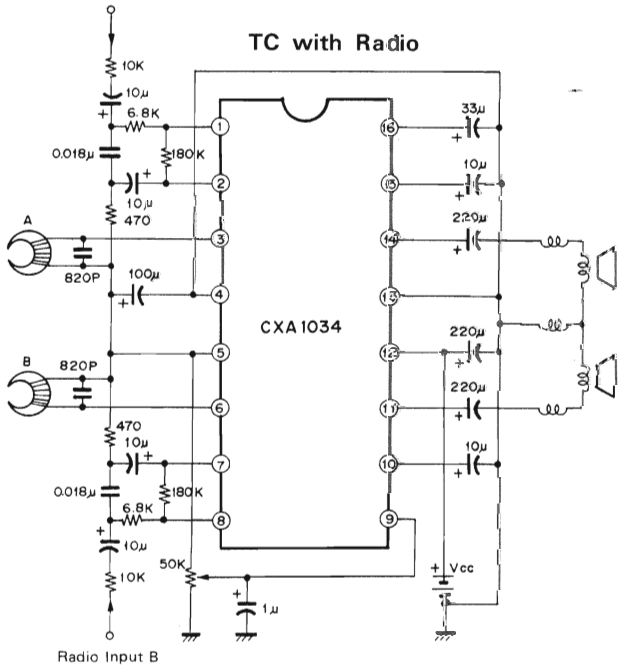


Input the signal from the playback head to input pins 3 and 6 and obtain approximately 30 dB (1 kHz) of signal amplification with the preamplifier stage and the NAB equalization characteristics with the low band compensation circuit. It controls the sound volume control circuit by receiving the DC control voltage from pin 9 and converting the voltage into current. The headphone driver circuit has an approximately 30 dB of signal amplification and a sufficient driving capability. Since V_{REF} pin 5 becomes floating with approximately $V_{CC}/2$, so the operation range can be taken widely (1.8V to 7.5V). C16 is used for absorbing volume sliding noise.

Headphone Stereo

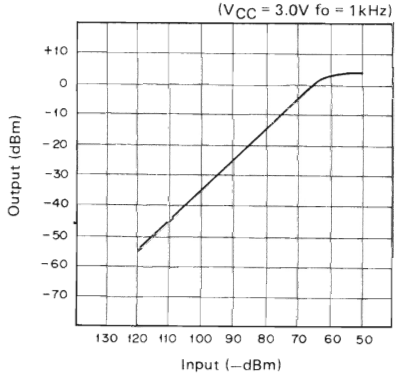


TC with Radio



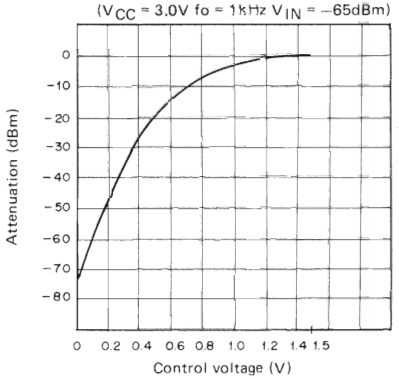
Output vs. Input

(V_{CC} = 3.0V fo = 1kHz)



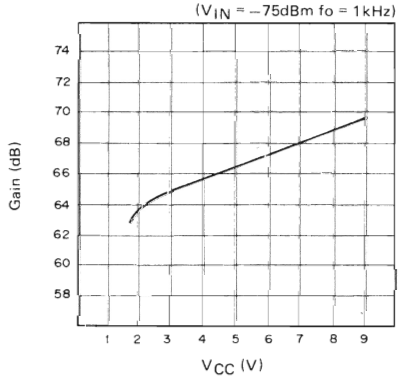
Attenuation vs. Control voltage

(V_{CC} = 3.0V fo = 1kHz V_{IN} = –65dBm)



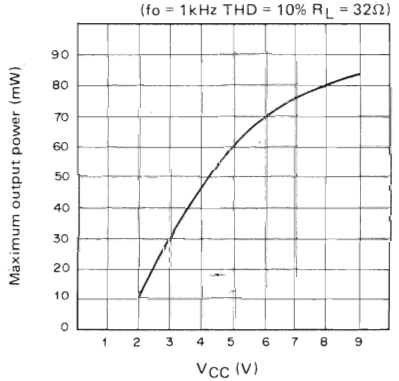
Gain vs. Vcc

(V_{IN} = –75dBm fo = 1kHz)



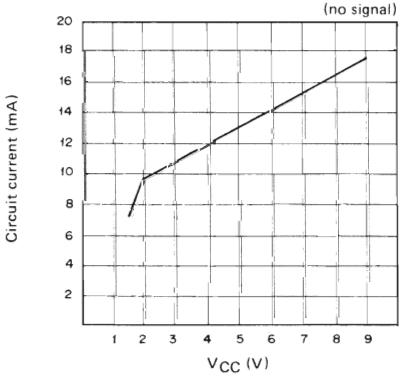
Maximum output power vs. Vcc

(fo = 1kHz THD = 10% R_L = 32Ω)



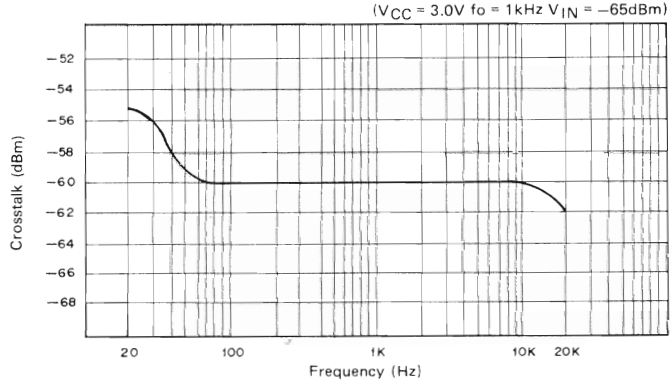
Circuit current

(no signal)



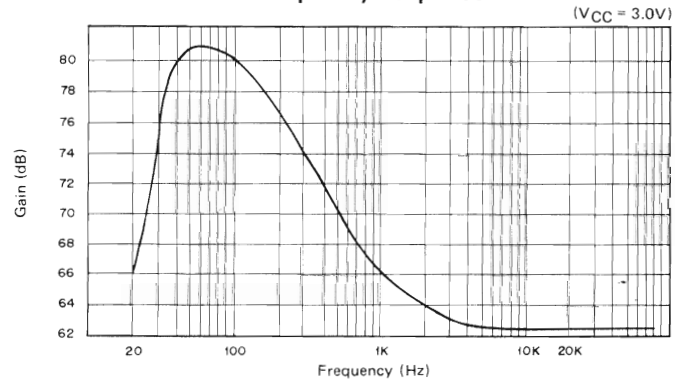
Channel to channel crosstalk

(V_{CC} = 3.0V fo = 1kHz V_{IN} = −65dBm)



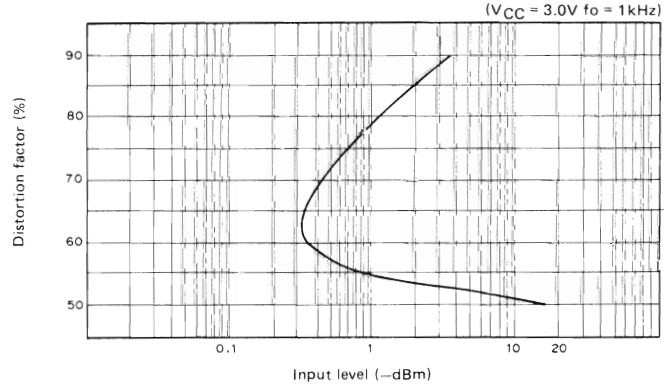
Frequency response

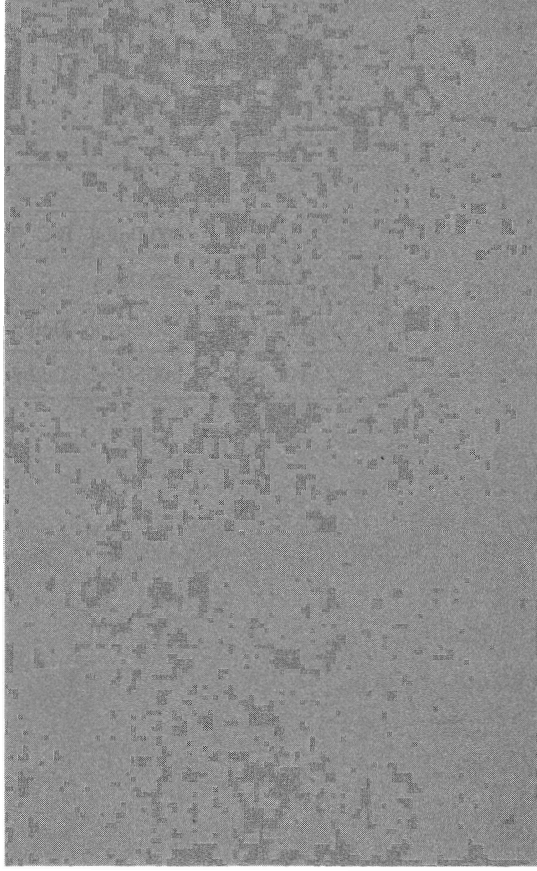
(V_{CC} = 3.0V)



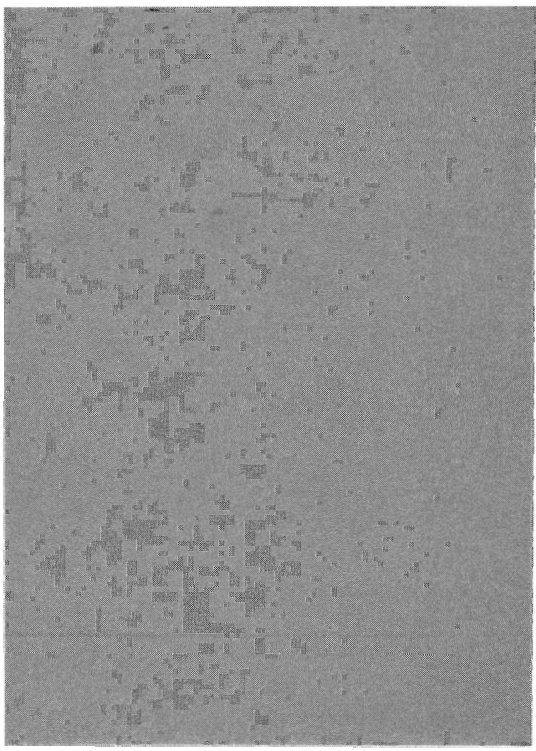
Distortion factor vs. Input level

(V_{CC} = 3.0V fo = 1kHz)





Dolby System



2) Dolby System

Type	Function	Page
CX20187 CXA1097Q	□□ Dolby B-C Type Noise Reduction System	109
CX20188 CXA1098Q	□□ Dolby B-C Type Noise Reduction System	125
CXA1057M	□□ Stereo Dolby B Type Noise Reduction	147
CXA1058M	□□ Stereo Dolby B Type Noise Reduction	156

SONY CX20187/CXA1097Q

Dolby* B-C Type Noise Reduction System

Description

The CX20187/CXA1097Q are integrated circuits designed for use in Dolby B and C type noise reduction systems. These devices offer complete stereo Dolby B and C type noise reduction processors with just one IC and a few external components.

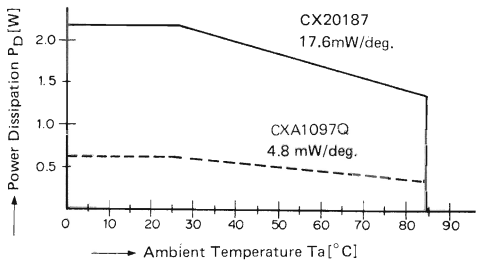
Features

- Dual channel processors integrated in one chip
- Minimum number of external components
- Programmable line output level
- Multiplex filter buffers included
- Low supply current (14 mA typ.)
- Wide supply voltage range (8 to 16V)

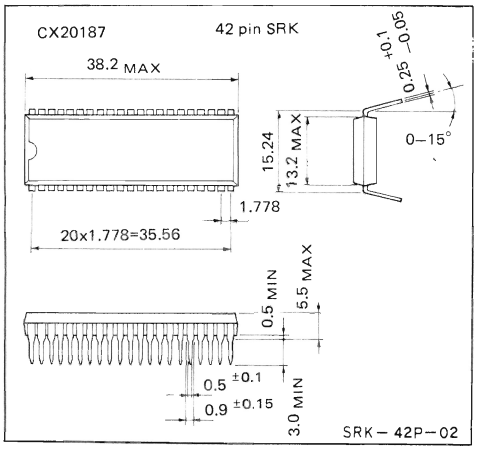
Absolute Maximum Ratings (Ta = 25°C)

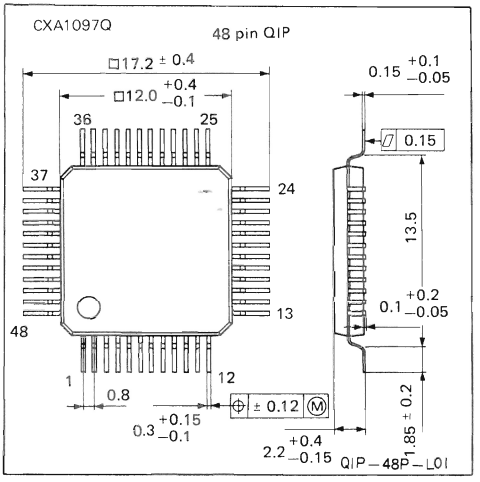
• Supply Voltage	V_{CC} — V_{EE}	17	V
• Operating Temperature	Topr.	−30 to +85	°C
• Storage Temperature	Tstg.	−55 to +150	°C
• Allowable Power Dissipation	P_D CX20187	2200	mW
	CXA1097Q	600	mW

Power Dissipations are indicated in the following Derating Curves.



Package Outline Unit: mm

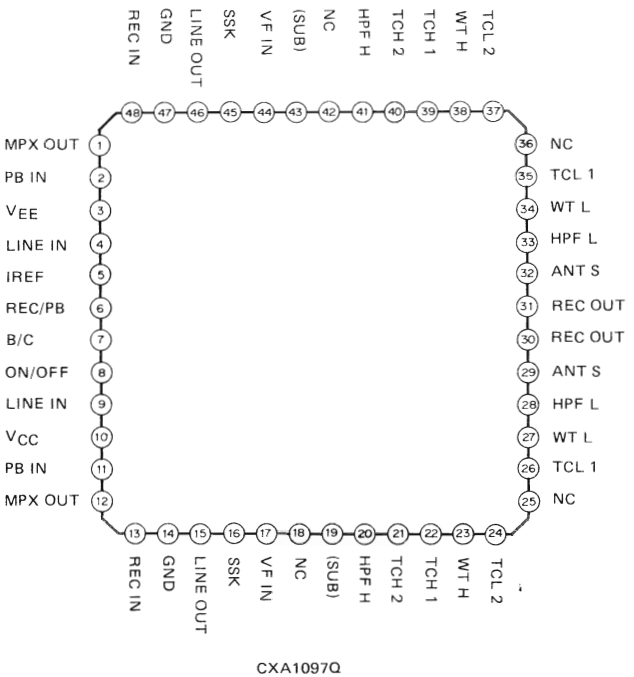




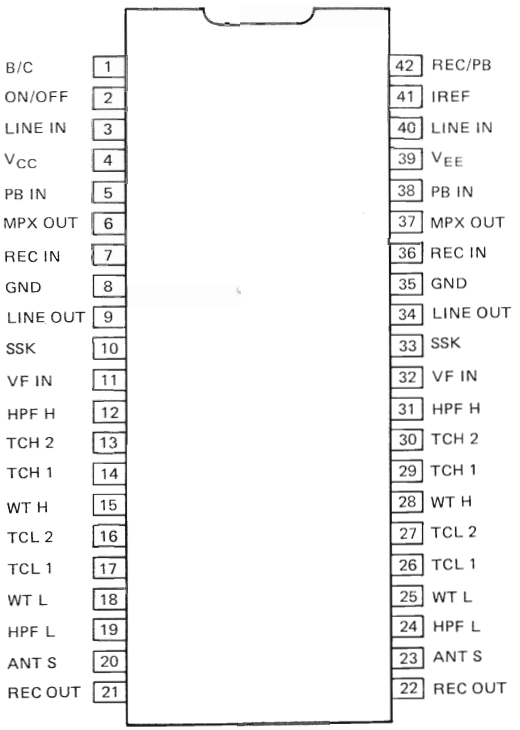
* These ICs are available only to the licensees of Dolby Laboratories Licensing Corporation from whom licensing and application information may be obtained.

* "Dolby" and double D symbol are trade marks of Dolby Laboratories Licensing Corporation.

Pin Configuration



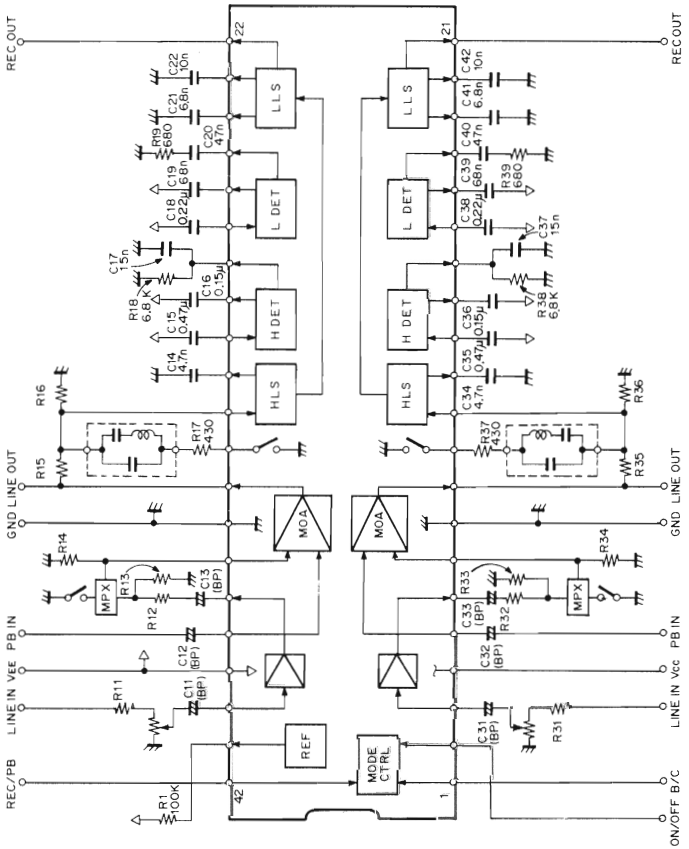
CXA1097Q



CX20187

SONY

Schematic Diagram (CX20187)



Note) CXA1097Q refer to Pin Configuration

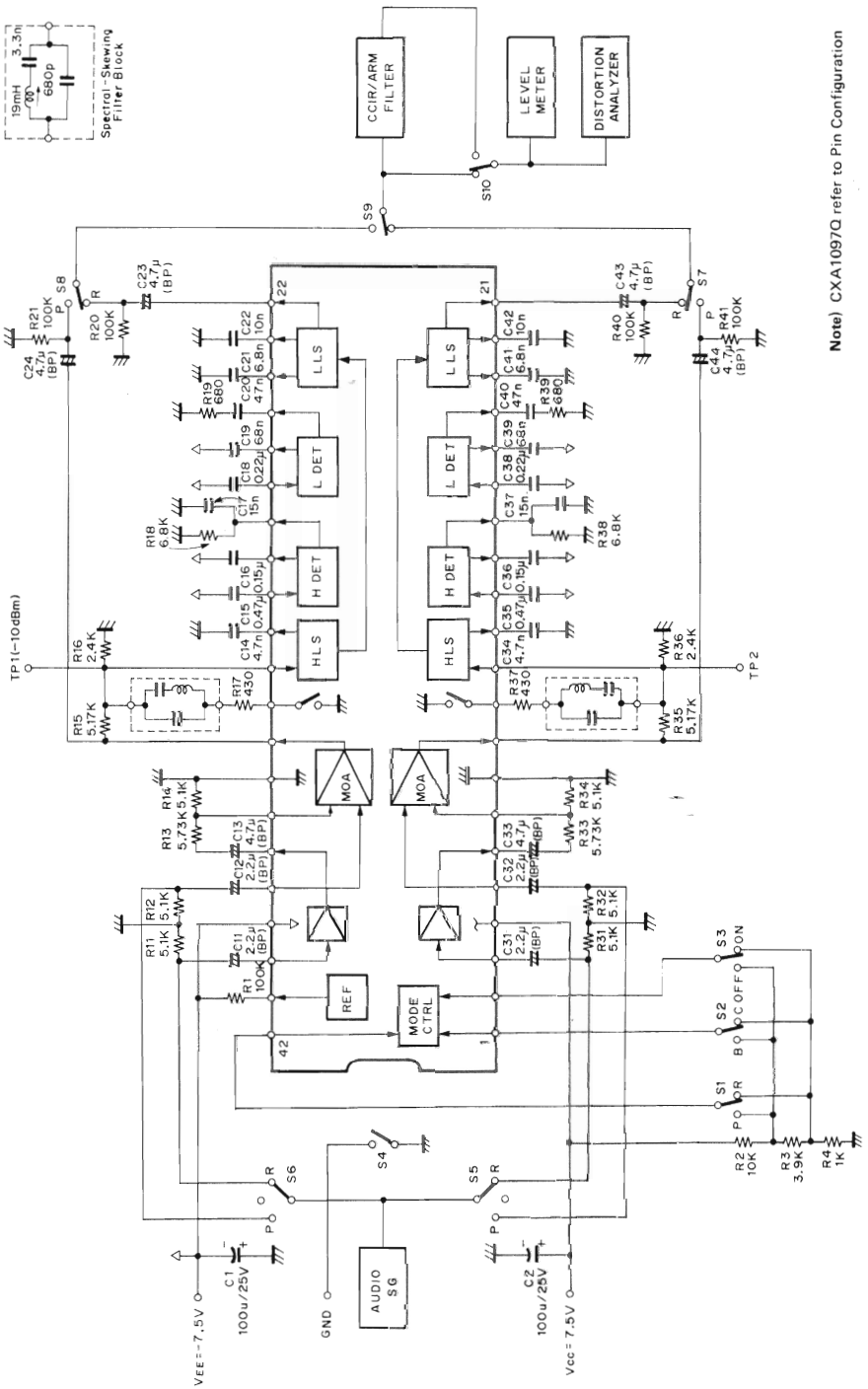
Electrical Characteristics

Ta=25°C, V_{CC}=7.5V, V_{EE}=−7.5V, unless otherwise specified.
Dolby Level: −10 dBm = 245 mVrms at Rec Out.

Characteristics	Symbol	Test Conditions *1				Min.	Typ.	Max.	unit
		R/P	NR	f(Hz)	Other conditions				
Operating Voltage	Vopr	—	—	—	Split	±4	—	±8	V
					Single	8	—	16	
Supply Current	Icc	R	OFF	—	No signal *2	10.0	14.0	18.0	mA
Encode Characteristics (Boost)									
B type (1)	B-R-1	R	B	500	−25 dB	1.7	2.9	4.1	dB
(2)	B-R-2	R	B	2k	−25 dB	5.8	7.0	8.2	dB
(3)	B-R-3	R	B	5k	−25 dB	4.2	5.4	6.6	dB
(4)	B-R-4	R	B	10k	−40 dB	9.7	10.4	11.6	dB
(5)	B-R-5	R	B	10k	0 dB	−0.8	0.4	1.6	dB
C type (1)	C-R-1	R	C	500	−60 dB	14.7	16.2	17.7	dB
(2)	C-R-2	R	C	500	−25 dB	7.7	9.2	10.7	dB
(3)	C-R-3	R	C	2k	−60 dB	19.7	20.7	22.2	dB
(4)	C-R-4	R	C	2k	−25 dB	5.9	7.4	8.9	dB
(5)	C-R-5	R	C	5k	−25 dB	4.0	5.5	7.0	dB
(6)	C-R-6	R	C	10k	0 dB	−5.0	−3.5	−2.0	dB
Frequency Response	F-R	R	OFF	20k	refer to 1kHz	−0.5	0.0	0.5	dB
Signal Handling *3	Vomax	R	OFF	1k	(Rec Out) T.H.D = 1%	13.0	15.5	—	dB
Total Harmonic Distortion									
NR OFF	T.H.D (OFF)	R	OFF	1k	+10 dB	—	0.12	0.30	%
C type	T.H.D (C)	R	C	1k	0 dB	—	0.05	0.15	%
MPX Amp Gain	GMPX	R	—	1k	LINE IN-MPX OUT	—	12.0	—	dB
MOA Gain	GMOA	R	—	1k	REC IN-LINE OUT	—	20.0	—	dB
Decode Gain	GPB	P	—	1k	PB IN-REC OUT	—	22.0	—	dB
Input impedance									
LINE IN	ZLINE	R	—	—		—	70	—	kΩ
REC IN	ZREC	R	—	—		—	50	—	kΩ
PB IN	ZPB	P	—	—		—	50	—	kΩ
C type Encode S/N Ratio (CCIR)	SN (CCIR)	R	C	—	Rg=5 kΩ	60	64	—	dB
Crosstalk									
REC-PB	CT-(1)	P	OFF	1k	0 dB	—	−93	—	dB
PB-REC	CT-(2)	R	OFF	1k	0 dB	—	−95	—	dB
Channel to Channel									
REC	CT-(3)	R	OFF	1k	0 dB	—	−85	—	dB
PB	CT-(4)	P	OFF	1k	0 dB	—	−84	—	dB
REC OUT Offset Voltage (C-OFF)	Voff	R	C	—		−40	—	40	mV
Control Voltage									
"H" Level	V-CH	—	—	—		2.5	—	—	V
"L" Level	V-CL	—	—	—		—	—	0.5	V

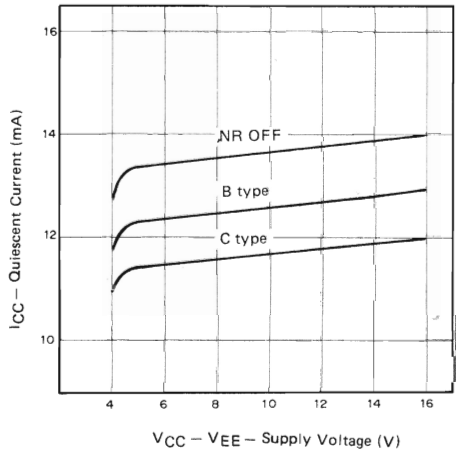
Note) *1 0 dB = Dolby Level at Rec Out
*2 Single Supply Operation
*3 The reference level of Line Output is 0 dBm (775 mVrms)

External Components and Test Circuit (CX20187)

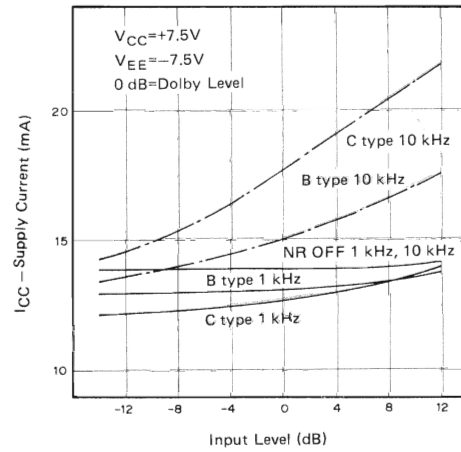


Note) CXA1097Q refer to Pin Configuration

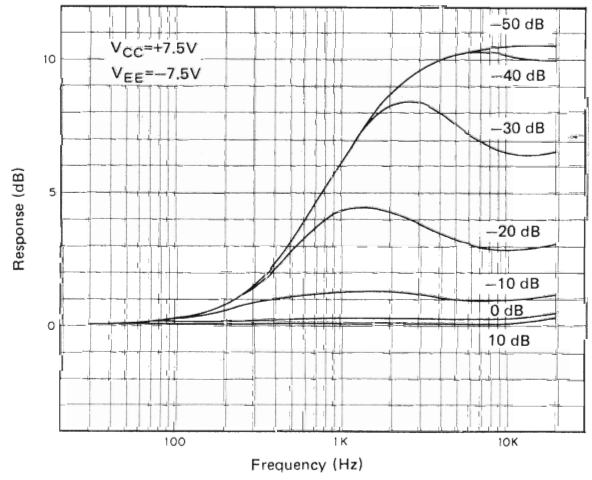
Quiescent Current vs. Supply Voltage



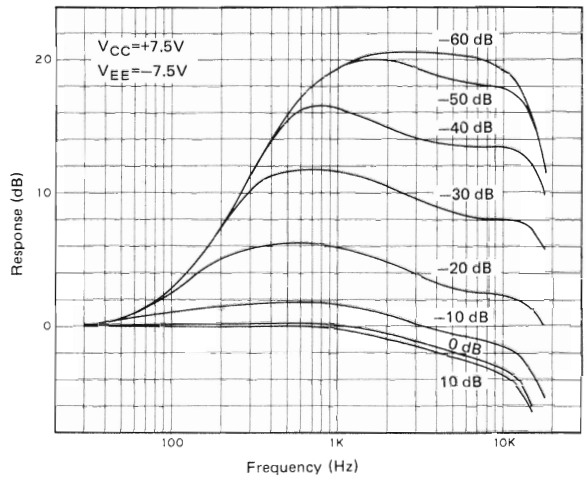
Supply Current vs. Input Level



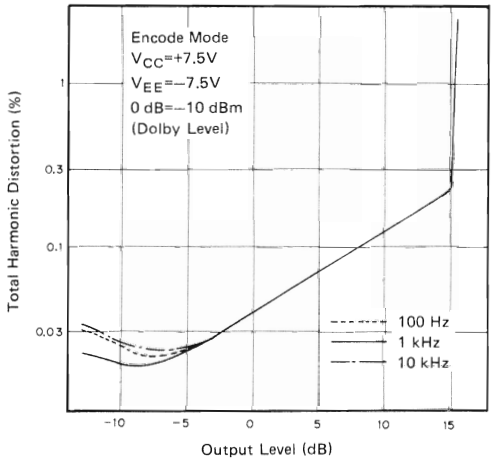
B type Encode Characteristics



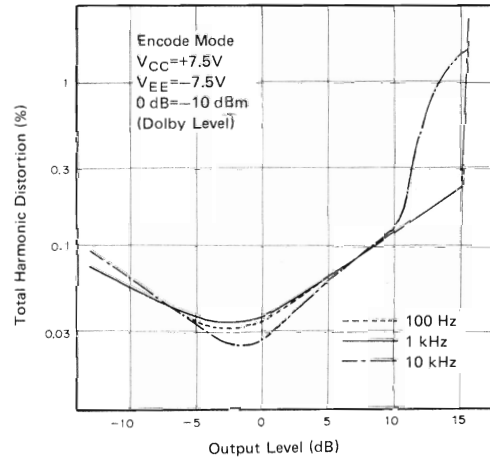
C type Encode Characteristics



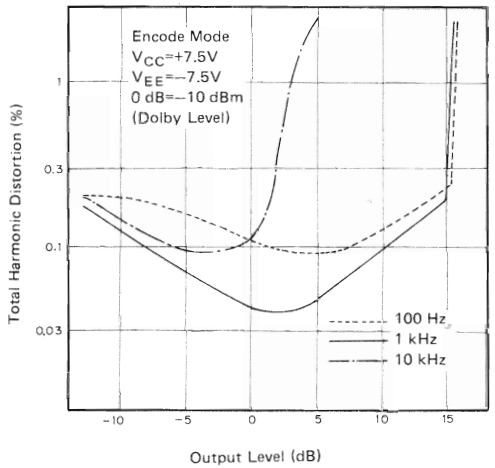
NR OFF Total Harmonic Distortion



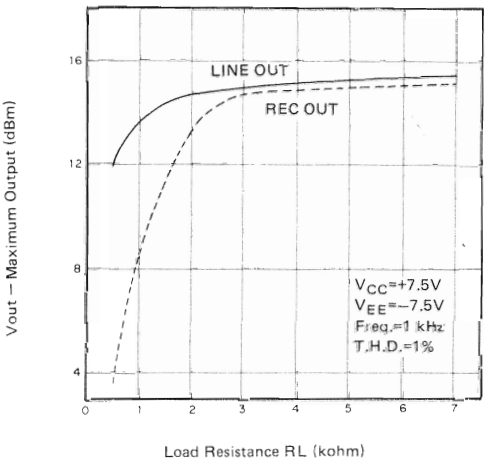
B type Total Harmonic Distortion



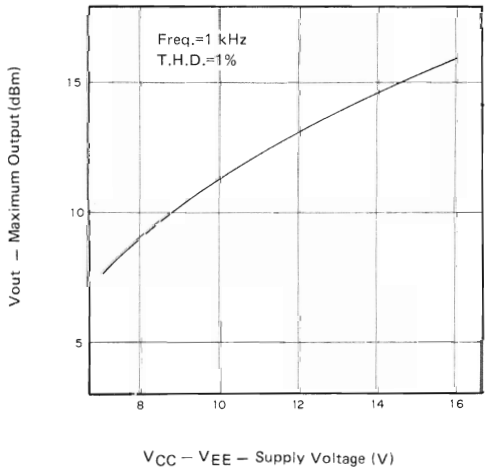
C type Total Harmonic Distortion



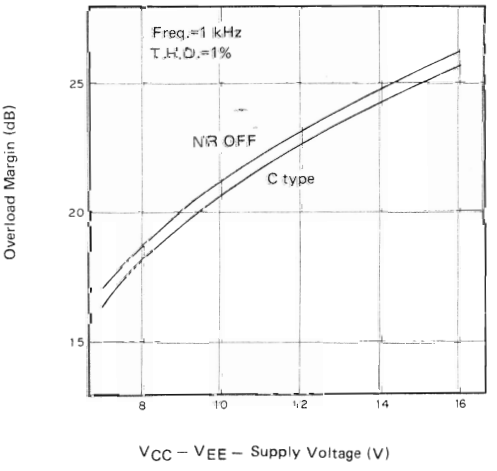
Drive Capability



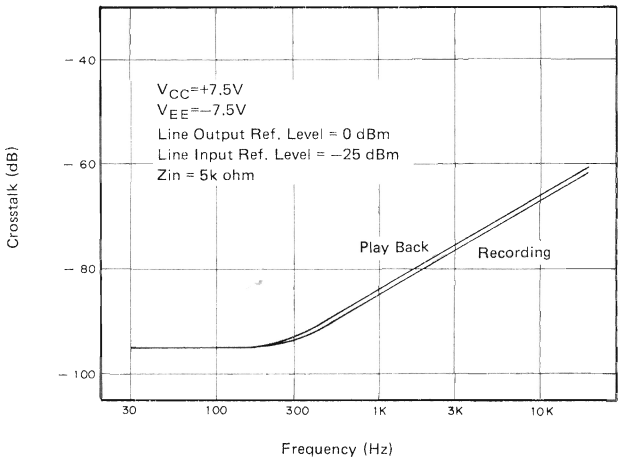
Line Output Overload Margin



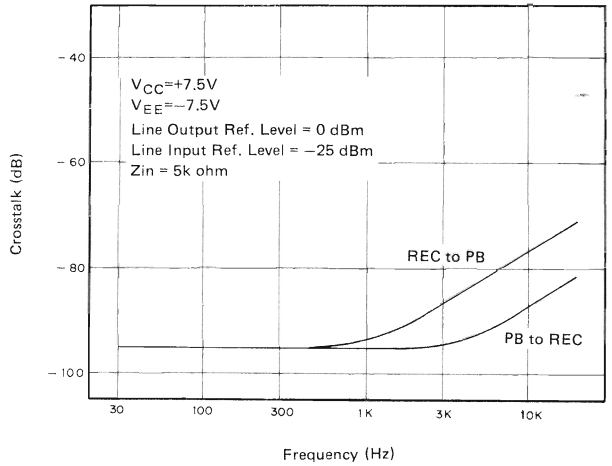
Recording Output Overload Margin



Channel to Channel Crosstalk



Recording and Play Back Crosstalk



Application Notes

1) Power Supply

The CX20187/CXA1097Q are designed to operate on either single supply or split supply. For single supply applications these devices generate the internal signal grounds of half the supply voltage. The range of the supply voltage is

(a) Single supply operation : +8 to +16 V
(b) Split supply operation : ±4 to ±8 V

The current consumption is roughly independent of supply voltage.
A useful feature of this device is the provision for programmable line output level, which will permit an optimum overload margin for various supply conditions. The overload margin therefore depends on both of the supply voltage and the line output reference level. Table a-1 shows the maximum line output reference levels to satisfy overload margins of 12 dB and 15 dB. Dolby Laboratories specifies 12 dB of minimum overload margin.

2) Operation Mode Control

The CX20187/CXA1097Q provide fully electronic switching circuits. The functions are controlled by DC voltages of the three control terminals of REC/PB, B type/C type and NR ON/OFF. The switching truth tables are shown in Table a-2. The switching levels, which are compatible with most commonly used logic gates, are as follows

(a) Single supply operation
$V_{CC}/2+2.5V \leqq VH \leqq V_{CC}$
$V_{CC}/2+0.5V \geqq VL \geqq GND$
(b) Split supply operation
$2.5V \leqq VH \leqq V_{CC}$
$0.5V \geqq VL \geqq V_{EE}$

Supply Voltage	Overload Margin	
	12 dB	15 dB
8V (±4V)	−3.0 dBm	−6.0 dBm
10V (±5V)	−0.7 dBm	−3.7 dBm
12V (±6V)	1.1 dBm	−1.9 dBm
15V (±7.5V)	3.3 dBm	0.3 dBm

Table a-1 Maximum Line Output Reference Levels

It is desirable to provide a CR circuit at REC/PB terminal with time constant from 100 mSec to 1 Sec, which will reduce switching clicks effectively.

3) Reference Levels

Characteristics of the Dolby noise reduction processors are defined with reference to the Dolby level. This particular level in these devices is −10 dBm (245 mVrms), and is measured at the Test Point (VF IN) or the recording output (REC OUT). Signal levels at other terminals, reffered to Dolby level at the Test Point, are as follows

Recording output : −10 dBm (245 mVrms) (fixed)
Play back input : −32 dBm (20 mVrms) (fixed)
Line output : variable
Line input : variable

REC/PB	"VH"	"VL"
Function	PB (Decode)	REC (Encode)

ON/OFF / B/C	"VH"	"VL"
"VH"	NR OFF	B type
"VL"	NR OFF	C type

Table a-2 Switching Truth Tables

The reference level of the line output (LINE OUT) is determined by an attenuation factor of the spectral skewing circuit. In Fig. a-1, an attenuation factor Hssk is defined as

Hssk = 20 · Log (1+R15/R16) (dB)

Spectral Skewing Circuit using Discrete (L=22 mH)

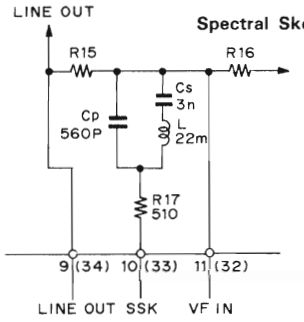


Fig. a-1

R15	R16	Reference Level	Supply Voltage
5.6k	2.7k	−0.2 dBm (750 mV)	≧ 11.0V (±5.5V)
4.3k	3.3k	−2.8 dBm (560 mV)	≧ 9.0V (±4.5V)
3.3k	4.3k	−5.1 dBm (430 mV)	≧ 8.0V (±4.0V)

Spectral Skewing Circuit using Filter Block

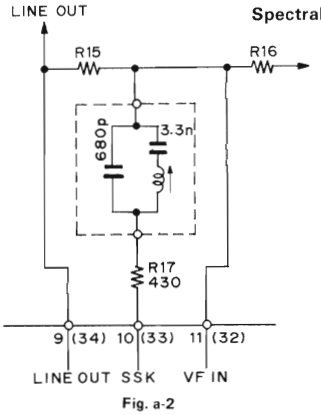


Fig. a-2

R15	R16	Reference Level	Supply Voltage
5.1k	2.4k	−0.1 dBm (765 mV)	≧ 11.0V (±5.5V)
3.9k	2.7k	−2.2 dBm (600 mV)	≧ 9.0V (±4.5V)
3.3k	3.3k	−4.0 dBm (490 mV)	≧ 8.0V (±4.0V)

Thus the line output reference level becomes

Line output reference level = Hssk−10 (dBm)

The parallel combination of R15 and R16 has to maintain a constant value to keep the accurate spectral skewing characteristics, that is 1.88 kohm for an inductor L with the inductance of 22 mH. The table in Fig. a-1 shows useful combinations of R15 and R16 for various applications.

A spectral skewing filter block, which is provided for the Dolby ICs of the CX20187/CXA1097Q and the CX20027/20028 series, will be effective for the practical applications, and will offer accurate characteristics. The application using the spectral skewing filter block and combinations of R15 and R16 are shown in the table of Fig. a-2. This filter block requires 1.64 kohm for the parallel combination of R15 and R16.

A gain from the line input (LINE IN) to the line output (LINE OUT) in the recording (encode) mode is formed by a total gain of MOA gain (REC IN → LINE OUT), MPX buffer gain and a MPX (multiplex) filter attenuation. The line input reference level can be adjusted by the MPX filter attenuation. MOA gain and MPX buffer gain are

MOA gain	(REC IN → LINE OUT)	20 dB
MPX buffer gain	(LINE IN → MPX OUT)	12 dB

In Fig. a-3 the attenuation factor MPX depends on the ratio of R12 and R13.

MPX Filter Attenuation

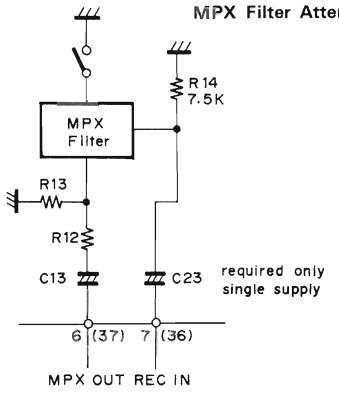


Fig. a-3

Available only for
Zin=3.3kohm, Zout=6.8kohm

R12	R13	HMPX (loss)
8.2k	5.6k	11.4 dB
6.8k	6.2k	9.9 dB
5.6k	8.2k	8.1 dB
4.7k	12.0k	6.5 dB

HMPX is

$$H_{MPX} = 20 \cdot \mathrm{Log}\,(1+R12 \cdot (1/R13 + 1/R14 + 1/Rin))\ (dB)$$

where, Rin is the input impedance of REC IN, which is typically 50 kohm. Thus the line input reference level is

Line input reference level = Line output reference level
$-32 + H_{MPX}$ (dBm)

The parallel combination of R14 and Rin (=50 kohm) should be equal to the output termination impedance of a MPX filter, and parallel combination of R12 and R13 should be equal to the input termination impedance of it. For example, combinations of R12 and R13 are shown in the table of Fig. a-3, which is available only for the MPX filter with 3.3 kohm of the input termination impedance and 6.8 kohm of the output termination impedance.

Fig. a-4 shows the level diagram of these devices. Increase of the line input sensitivity will degrade the overall noise reduction effect, which has to satisfy more than 17 dB according to the requirement of Dolby Laboratories. A recommendable line input reference level is approximately −25 dBm (44 mVrms).

Level Diagram in the Recording Mode

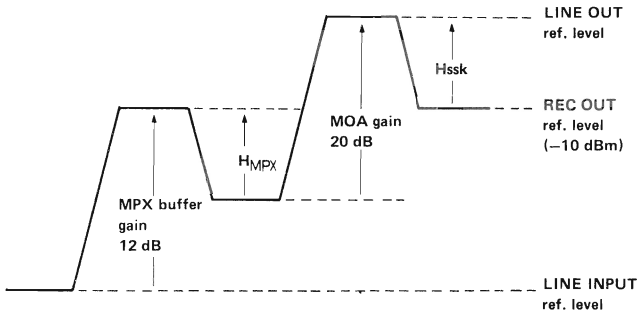


Fig. a-4

4) Application Circuits

(a) Switchable Processor with Split Supply (Fig. a-6)

Supply voltage	: ±7V typ. (±5.5 to ±8V)
Line output level	: −0.1 dBm (765 mVrms)
Recording output level	: −10.0 dBm (245 mVrms)
Line input level	: −25.6 dBm (41 mVrms)
Play back input level	: −32.0 dBm (20 mVrms)

This circuit is suitable for high grade cassette decks.

(b) Switchable Processor with Single Supply (Fig. a-7)

Supply voltage	: +12V typ. (+9 to +16V)
Line output level	: −2.2 dBm (600 mVrms)
Recording output level	: −10.0 dBm (245 mVrms)
Line input level	: −24.3 dBm (47 mVrms)
Play back input level	: −32.0 dBm (20 mVrms)

This circuit is most appropriate for general applications.

(c) Play Back Processor with AUX input (Fig. a-8)

Supply voltage	: +9V typ. (+8 to +16V)
Line output level	: −4.0 dBm (490 mVrms)
Tape input level	: −32.0 dBm (20 mVrms)
AUX input level	: −24.0 dBm (49 mVrms)

This unique application providing AUX input is suitable for car stereo players and car stereo cassette decks. AUX input will be useful for a tuner input. REC/PB switching operates as the switching of AUX/Tape. The operation in AUX input mode is independent of the switch positions of B type/C type and NR ON/OFF.

(d) Application for Dubbing Cassette Decks

The CX20187/CXA1097Q simplifies the structure of dubbing decks. Conventional dubbing decks utilize the Dolby processors commonly for two systems. Problems occur on the dubbing mode of a Dolby NR encoded tape. Listeners will be forced to monitor non-decoded sound. This device offers a simple solution, which is to utilize the recording output signal in the play back mode as shown in Fig. a-5. In the dubbing mode the processor operates as a decode (play back) mode. The monitor (line output) signal from the deck A will be decoded if necessary, however, the deck B will record directly wihtout decoding. This special application is possible because this device generates a non-decoded signal at the recording output in the decode mode even though it operates on the B type or C type NR.

Application for Dubbing Deck

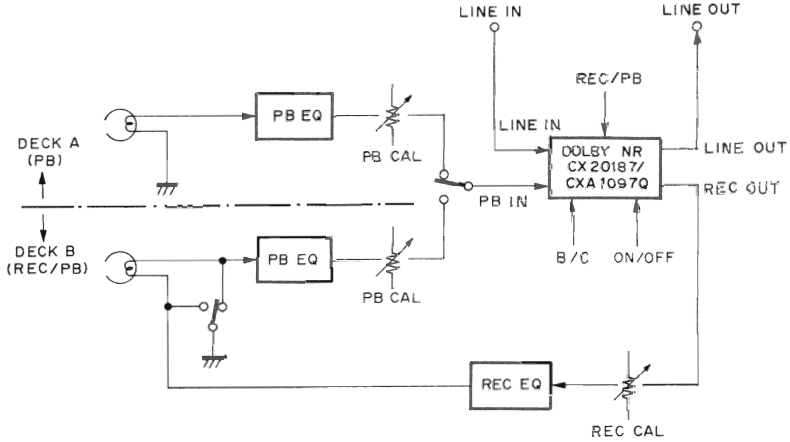


Fig. a-5

Switchable Processor with Split Supply (CX20187)

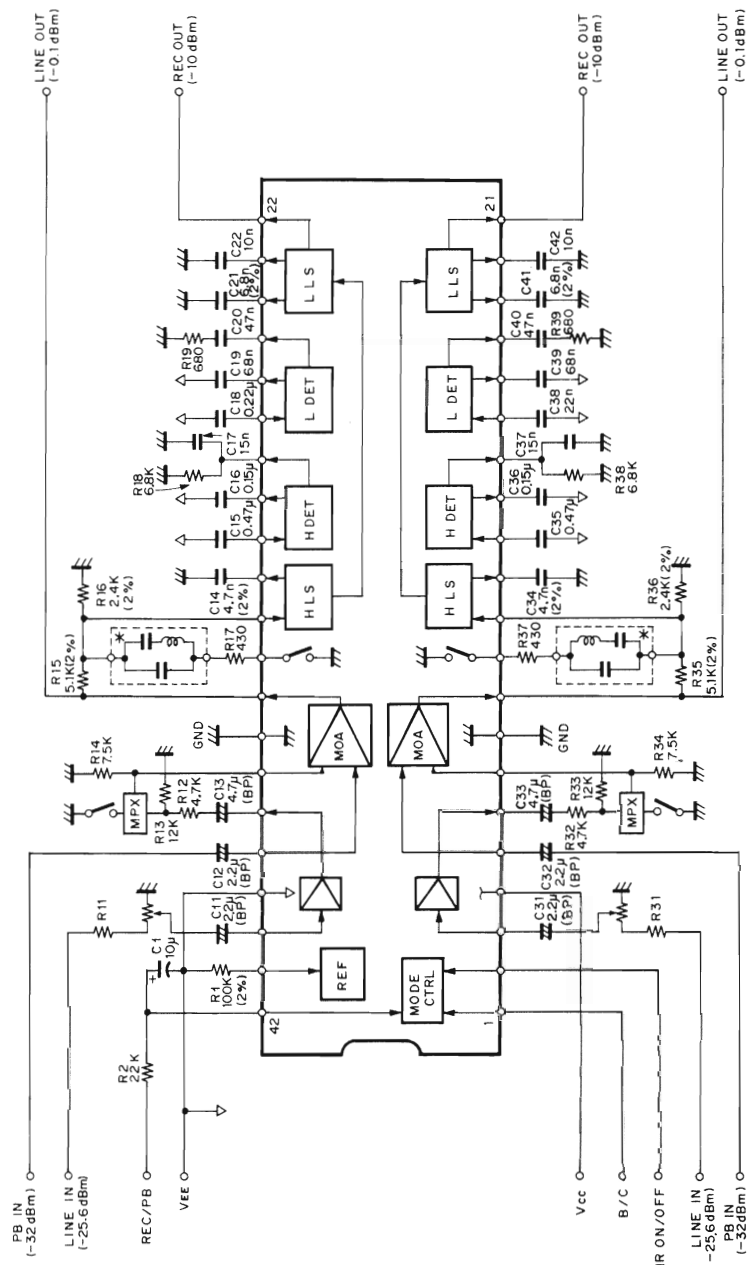


Fig. a-6

Notes) 1. Resistor tolerances are ±5% unless otherwise specified
2. Capacitor tolerances are ±5% unless otherwise specified except for coupling capacitors
3. CXA1097Q refer to Pin Configuration
* Spectral Skewing Filter Block (See Application Notes 3).)

Switchable Processor with Single Supply (CX20187)

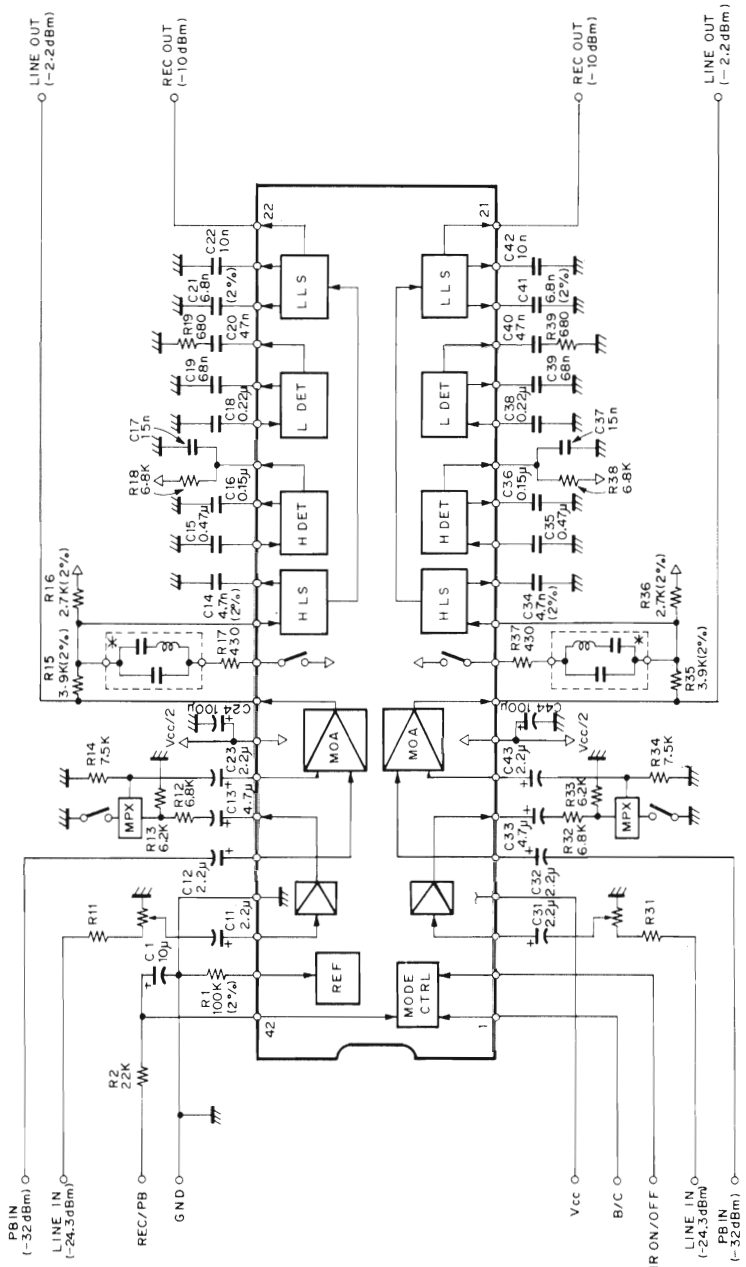


Fig. a-7

Notes)
1. Resistor tolerances are ±5% unless otherwise specified
2. Capacitor tolerances are ±5% unless otherwise specified except for coupling capacitors
3. Terminals of Vcc/2, for Ch 1 and Ch 2 should be separated in single supply
4. CXA1097Q refer to Pin Configuration
   * Spectral Skewing Filter Block (See Application Notes 3).)

Play Back Processor with AUX Input (CX20187)

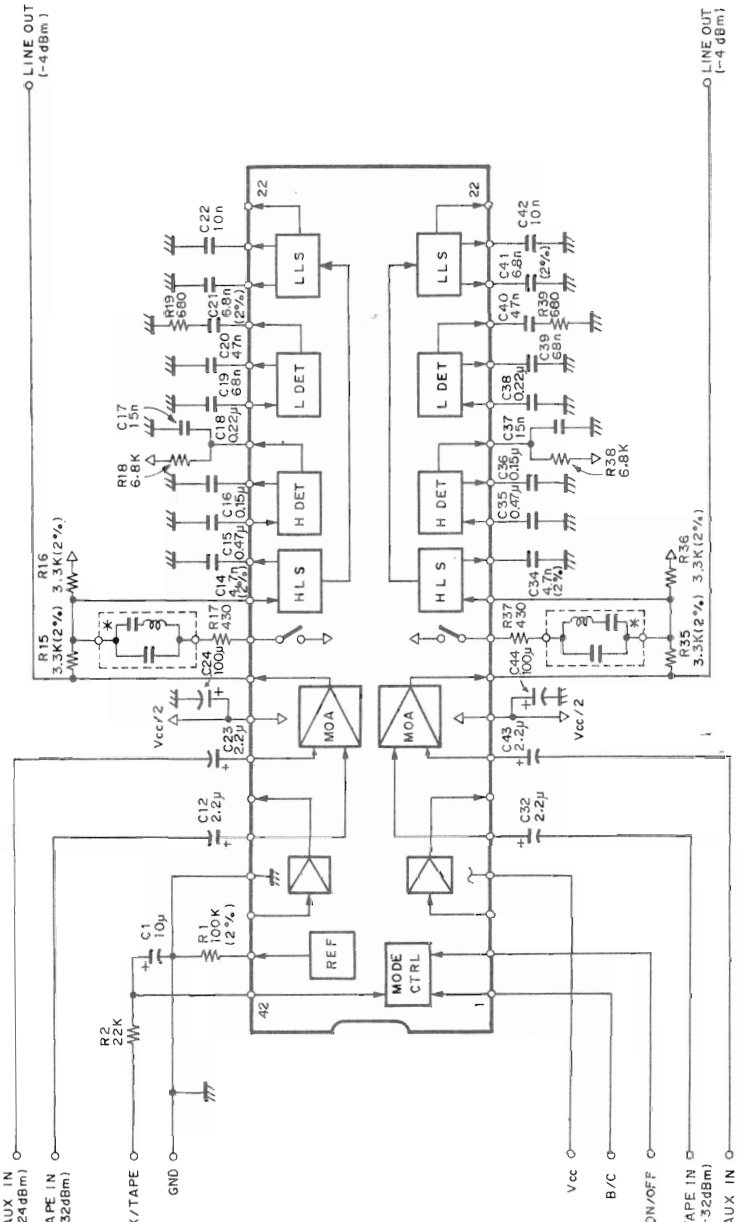


Fig. a-8

Notes) 1. Resistor tolerances are ±5% unless otherwise specified
2. Capacitor tolerances are ±5% unless otherwise specified except for coupling capacitors
3. Terminals of Vcc/2, for Ch 1 and Ch 2 should be separated in single supply
4. CXA1097Q refer to Pin Configuration
* Spectral Skewing Filter Block (See Application Notes 3.)

SONY CX20188/CXA1098Q

Dolby B-C Type Noise Reduction System

Description

The CX20188/CXA1098Q are ICs designed for use in Dolby B and C type noise reduction systems. These ICs offer complete stereo Dolby B and C type noise reduction with just one IC and a few external components. These devices provide inductorless spectral skewing circuits and excellent low distortion characteristics, and are suitable for use in high grade cassette decks and high grade automotive equipments.

Features

- Spectral skewing circuits with inductorless structure
- Very low distortion
  (0.002% typ. 1 kHz +10 dB in NR OFF)
- Dual channel processors in one chip
- Programmable input and output levels
- Low supply current (16 mA typ. in NR OFF)

Structure

Bipolar silicon monolithic IC.

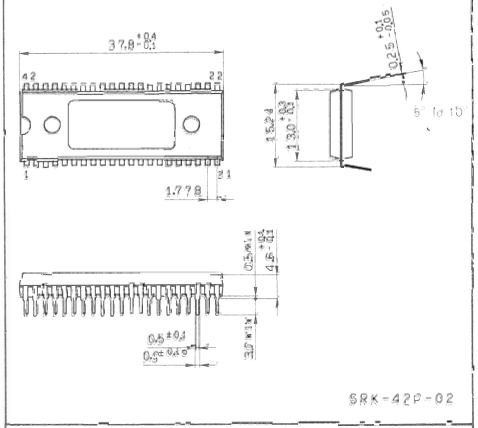
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	22	V
• Operating temperature	Topr	−30 to +85	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation			
CX20188	PD	2200	mW
CXA1098Q	PD	600	mW

Package Outline

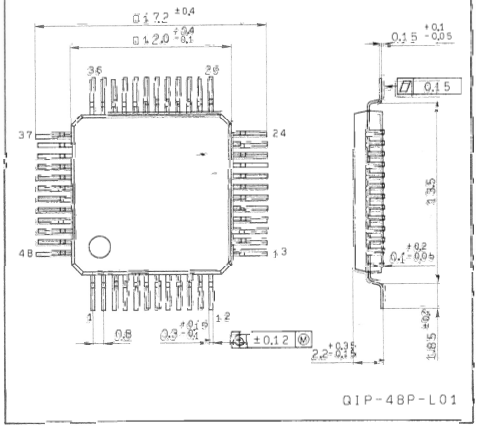
Unit: mm

CX20188 42 pin SRK



SRK-42P-02

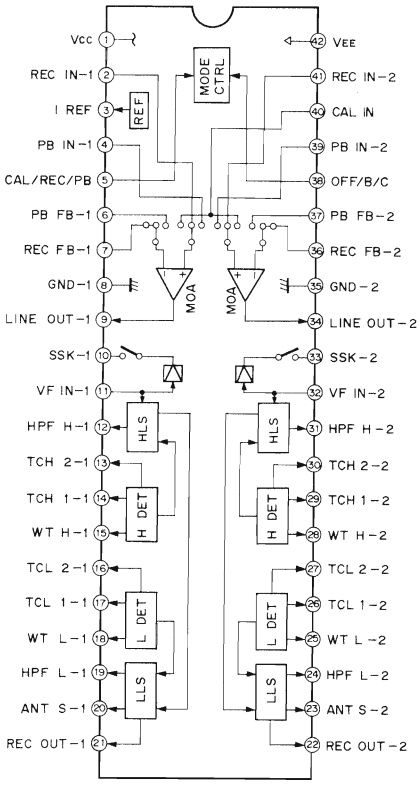
CXA1098Q 48 pin QIP



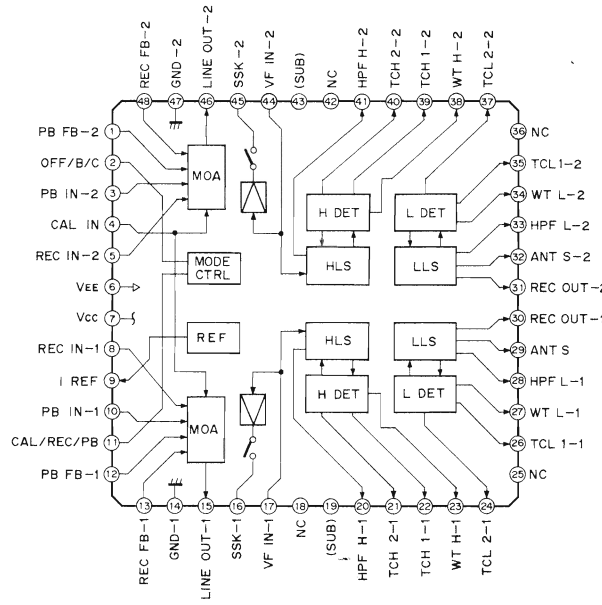
QIP-48P-L01

Note) These ICs are available only to the licensees of Dolby Laboratories Licensing Corporation from whom licensing and application information may be obtained.
"Dolby" and double D symbols are trade marks of Dolby Laboratories Licensing Corporation.

Block Diagram and Pin Configuration



CX20188

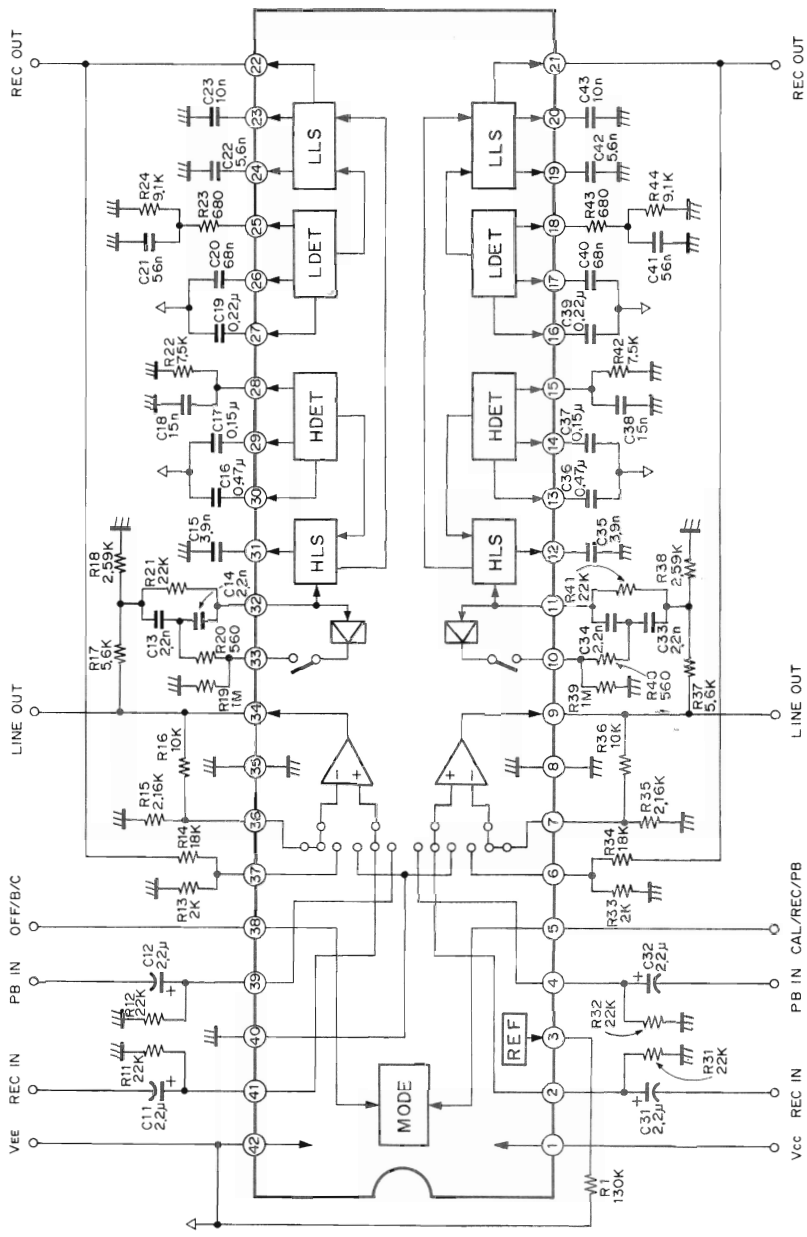


CXA1098Q

Pin Description

CX20188 No.	CXA1098Q No.	Symbol	Description
1	7	V_{CC}	Positive power supply
2, 41	5, 8	REC IN	Recording input
3	9	I REF	Reference current source
4, 39	3, 10	RB IN	Playback input
5	11	CAL/REC/PB	Calibration/recording/playback switching
6, 37	1, 12	PB FB	Playback feedback
7, 36	13, 48	REC FB	Recording feedback
8, 35	14, 47	GND	With split supply: GND, with single supply: $V_{CC}/2$
9, 34	15, 46	LINE OUT	Line output (decode output)
10, 33	16, 45	SSK	Spectral skewing switch
11, 32	17, 44	VF IN	Encode circuit input
12, 31	20, 41	HPF H	HLS high-pass filter
13, 30	21, 40	TCH 2	HLS detector time constant 2
14, 29	22, 39	TCH 1	HLS detector time constant 1
15, 28	23, 38	WT H	HLS weighting
16, 27	24, 37	TCL 2	LLS detector time constant 2
17, 26	26, 35	TCL 1	LLS detector time constant 1
18, 25	27, 34	WT L	LLS weighting
19, 24	28, 33	HPF L	LLS high-pass filter
20, 23	29, 32	ANT S	Anti-saturation
21, 22	30, 31	REC OUT	Recording output (encode output)
38	2	OFF/B/C	Dolby NR off/B-type/C-type switching
40	4	CAL IN	Calibration input
42	6	V_{EE}	With split supply: negative power supply, with single supply: GND

CX20188 Application Circuit



Note) For operation below 12V C_{20} and C_{40} should be 0.1 μF.

Electrical Characteristics Ta=25°C, V_{CC}=10V, V_{EE}=−10V unless otherwise specified.
Dolby Level: −10 dBm (=245 mVrms) at REC OUT

Characteristic	Symbol	Test Condition*1				Min.	Typ.	Max.	Unit
		R/P	NR	f(Hz)	Other Condition				
Operating voltage*2	Vopr	—	—	—	Split Single	±4.0 8.0	— —	±10.5 21.0	V V
Supply current*3	Icc	R	OFF	—	No Signal	12.0	16.0	21.0	mA
Encode characteristic (Boost)									
B-type (1)	B-R-1	R	B	500	−25dB	1.9	2.9	3.9	dB
(2)	B-R-2	R	B	2k	−25dB	6.0	7.0	8.0	dB
(3)	B-R-3	R	B	5k	−25dB	4.4	5.4	6.4	dB
(4)	B-R-4	R	B	10k	−40dB	9.7	10.4	11.4	dB
(5)	B-R-5	R	B	10k	0dB	−0.6	0.4	1.4	dB
C-type (1)	C-R-1	R	C	500	−60dB	15.0	16.2	17.4	dB
(2)	C-R-2	R	C	500	−25dB	8.0	9.2	10.4	dB
(3)	C-R-3	R	C	2k	−60dB	19.7	20.7	21.9	dB
(4)	C-R-4	R	C	2k	−25dB	6.2	7.4	8.6	dB
(5)	C-R-5	R	C	5k	−25dB	4.3	5.5	6.7	dB
(6)	C-R-6	R	C	10k	0dB	−4.7	−3.5	−2.3	dB
Frequency response	F-R	R	OFF	20k	Refer to 1kHz	−0.5	0.0	0.5	dB
Signal handling*4	Vomax	R	OFF	1k	THD=1% at REC OUT	15.0	18.0	—	dB
Total harmonic distortion									
NR OFF	THD(OFF)	R	OFF	1k	+10dB	—	0.002	0.05	%
B-type	THD(B)	R	B	1k	+10dB	—	0.02	0.05	%
C-type	THD(C)	R	C	1k	+10dB	—	0.05	0.10	%
C-type encode S/N ratio	SN(CCIR)	R	C	—	Rg=5kΩ (CCIR/ARM)	60	64	—	dB
Crosstalk									
REC-PB	CT-1	P	OFF	1k	0dB	—	−100	−70	dB
PB-REC	CT-2	R	OFF	1k	0dB	—	−97	−70	dB
REC ch to ch	CT-3	R	OFF	1k	0dB	—	−86	−65	dB
PB ch to ch	CT-4	P	OFF	1k	0dB	—	−85	−65	dB

Characteristic	Symbol	Test Condition*1				Min.	Typ.	Max.	Unit
		R/P	NR	f(Hz)	Other Condition				
REC OUT Offset Voltage (C-type-OFF)	V_{off}	R	C	—	—	−40	0	40	mV
Control Voltage									
"H" level	VC-H	—	—	—	—	3.0	—	V_{CC}	V
"M" level	VC-M	—	—	—	—	−0.7	—	0.7	V
"L" level	VC-L	—	—	—	—	V_{EE}	—	−3.0	V

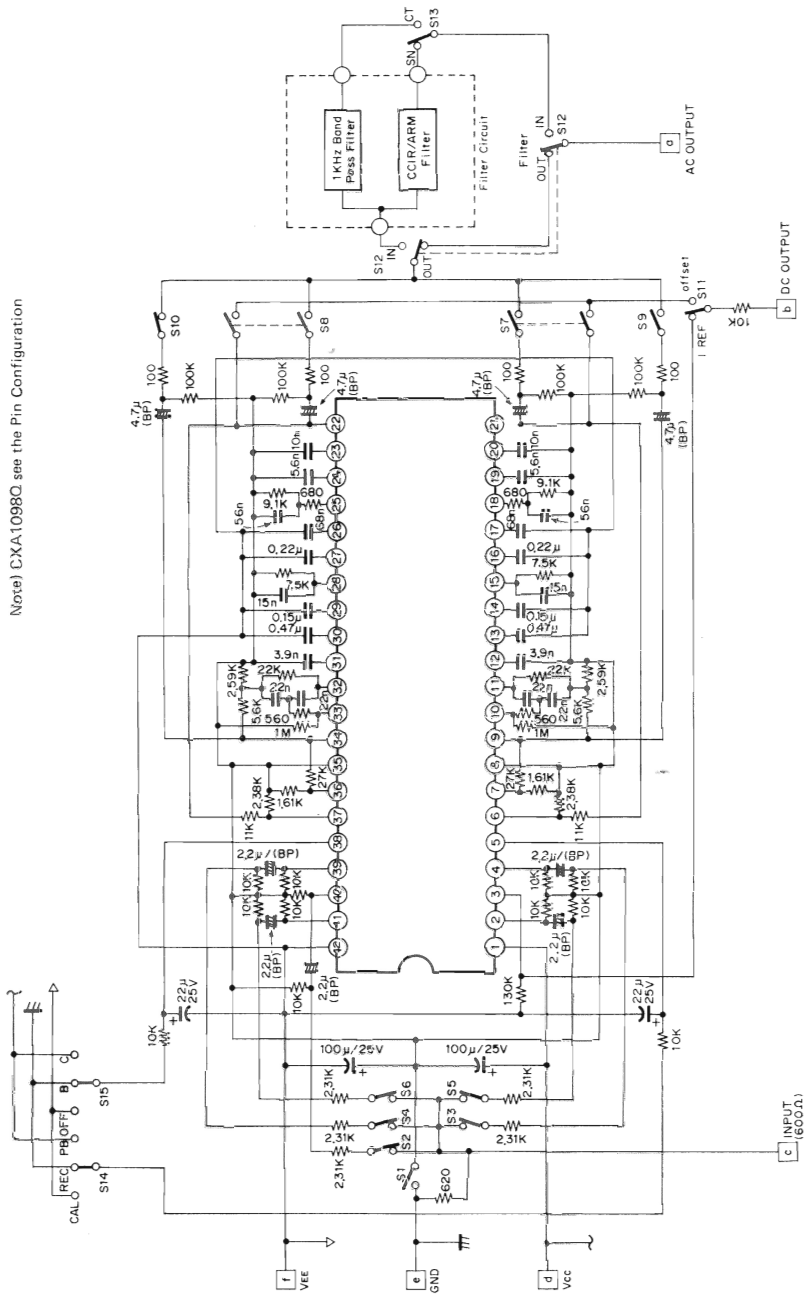
Note) *1. 0 dB means the level which provides the Dolby level at the recording output in the noise reduction off mode.

*2. Modification of the external components value should be required for low voltage condition.

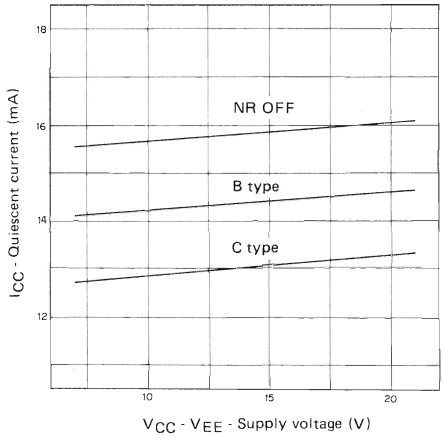
*3. Single supply operation.

*4. The reference level of the line output is 0 dBm (775 mVrms).

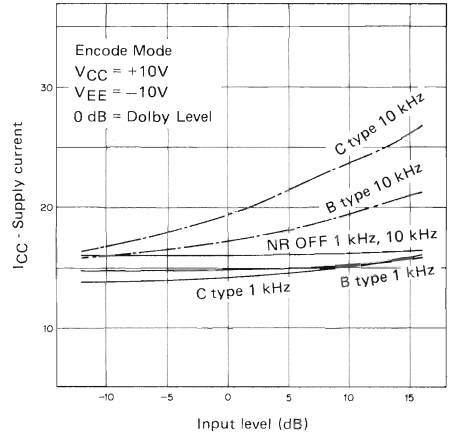
Electrical Characteristics Test Circuit



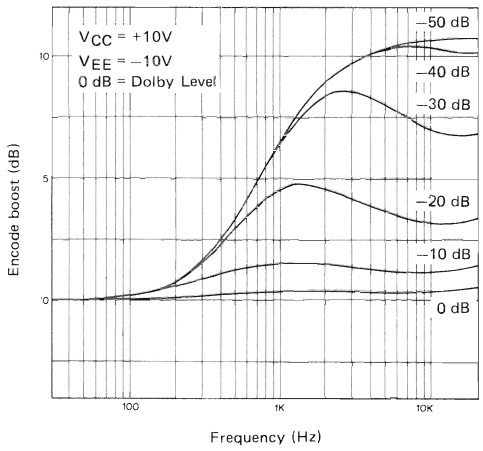
Quiescent current vs. Supply voltage



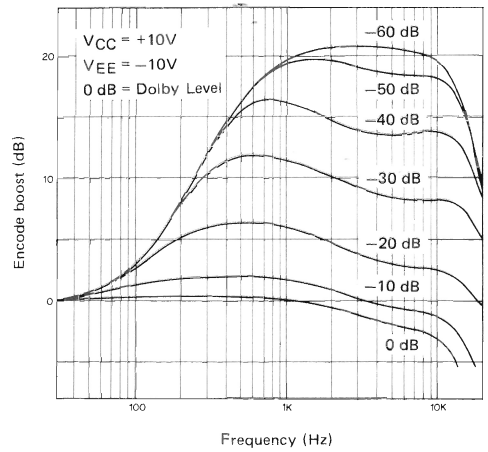
Supply current vs. Input level



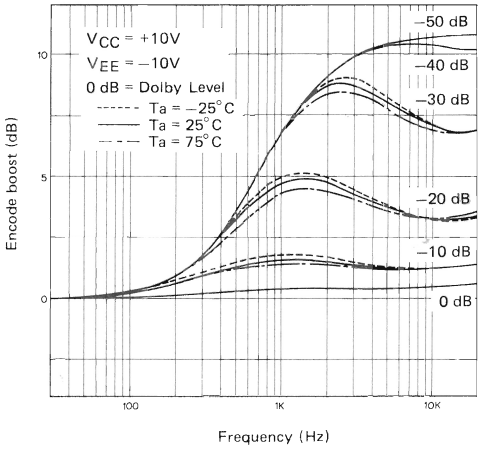
B type encode characteristics



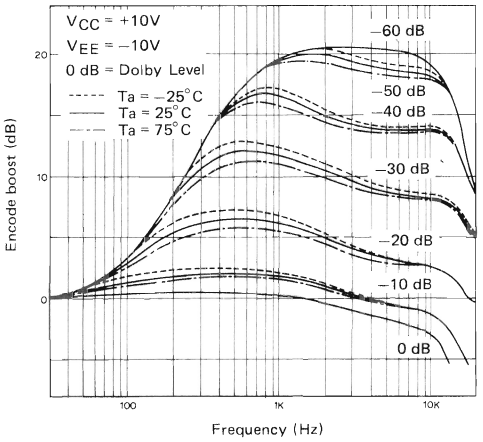
C type encode characteristics



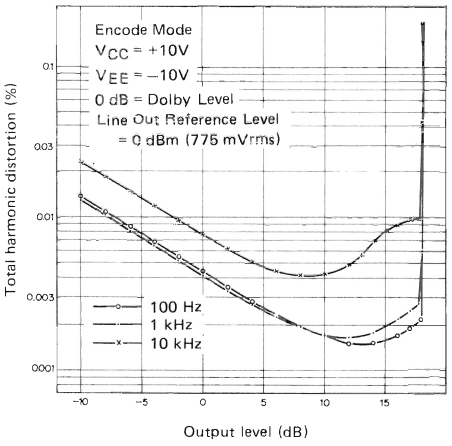
B type temperature characteristics



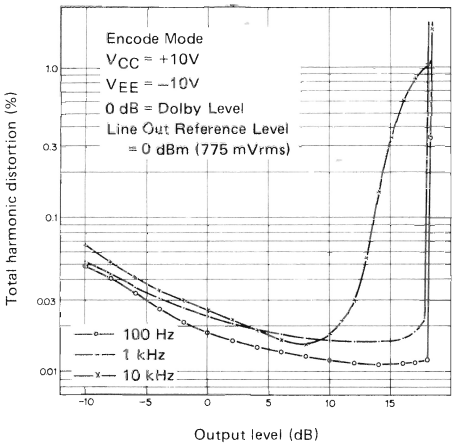
C type temperature characteristics



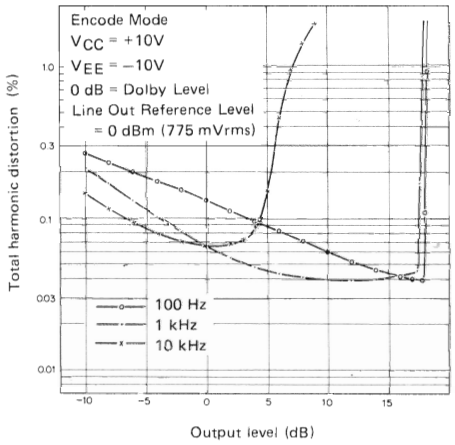
NR OFF total harmonic distortion



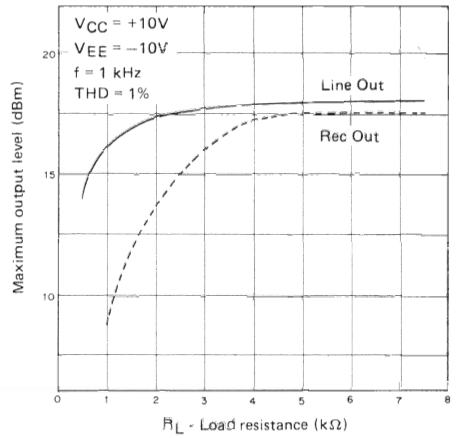
B type total harmonic distortion



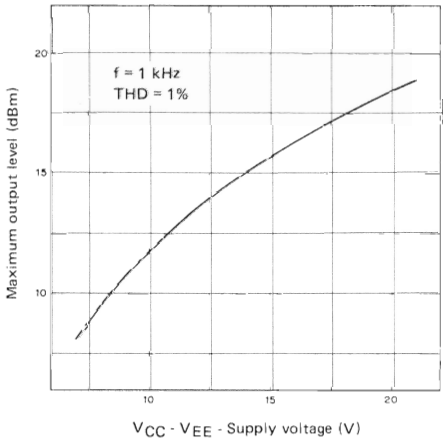
C type total harmonic distortion



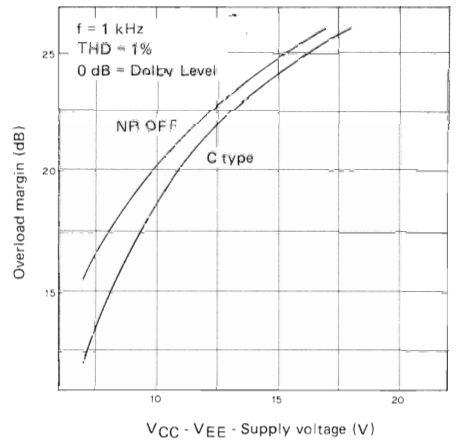
Drive capability



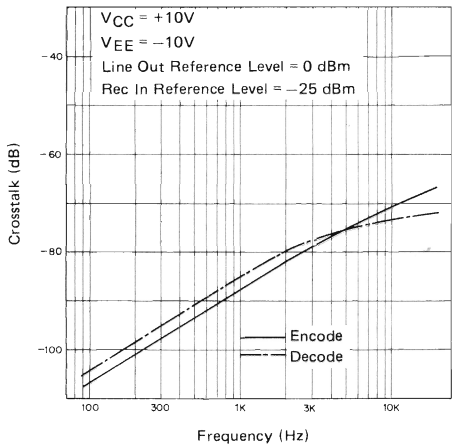
Maximum line output level



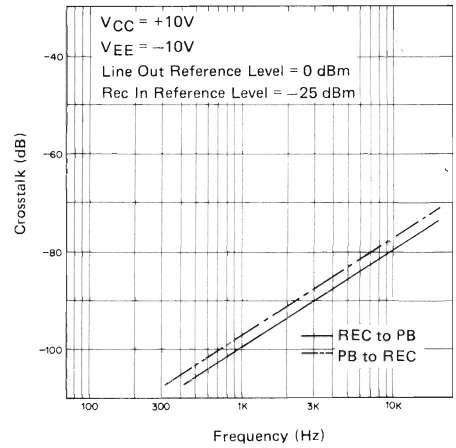
Recording output overload margin



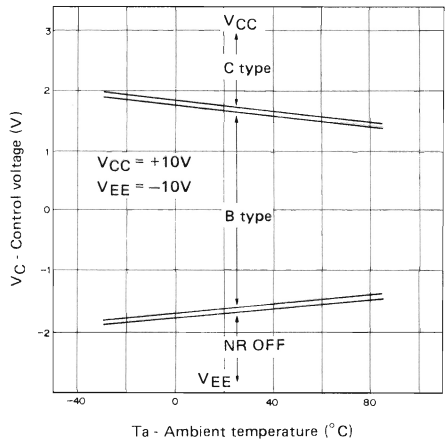
Channel to channel crosstalk



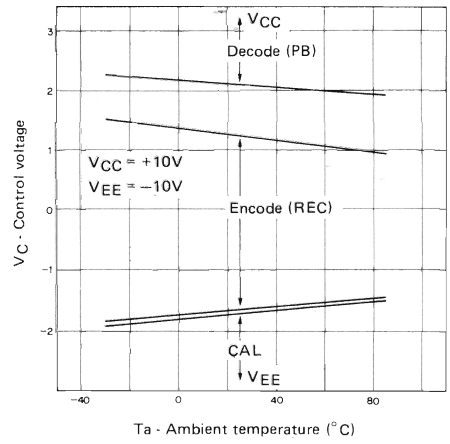
Recording and play back crosstalk



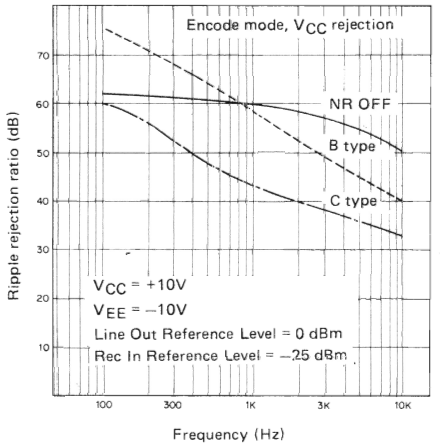
Control threshold voltage (1)



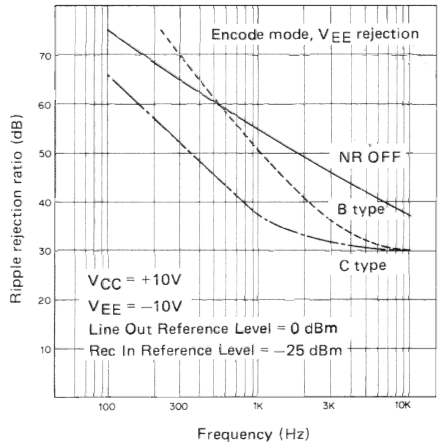
Control threshold voltage (2)



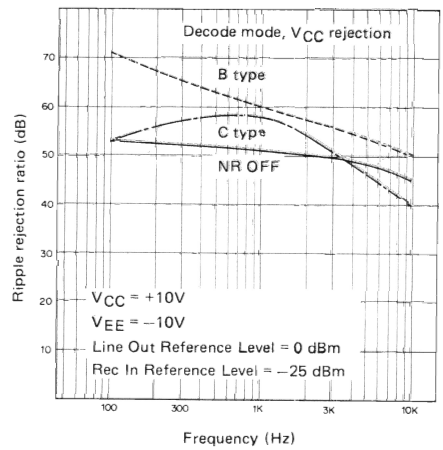
Ripple rejection ratio (1)



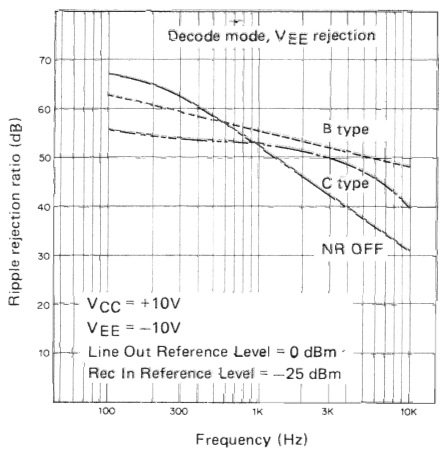
Ripple rejection ratio (2)



Ripple rejection ratio (3)



Ripple rejection ratio (4)



Notes on Application

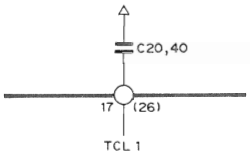
1) Power Supply

The CX20188/CXA1098Q are designed to operate on either single ended supply or split supply. The operation range of the supply voltage is

(a) Single ended supply operation: 8 to 21 V

(b) Split supply operation : ±4 to ±10.5 V

For the low supply voltage condition these devices require to change the capacitances of the low level stage detectors as shown in Fig. a-1.



High voltage condition
above +12V or ±6V supply
C20, C40=68 nF
Low voltage condition
below +12V or ±6V
C20, C40=0.1 μF

Fig. a-1

For the single ended supply operation these devices generate the signal grounds of half the supply voltage. Independent two signal grounds are provided for each channel. These pins should be connected bypass capacitors independently. External connection between the signal grounds may save the bypass capacitor, however, low frequency channel separation will degrade even though acceptable.

A usefull feature of these devices is the provision for programmable line output structure, which will permit an optimum overload margin for various supply conditions. The overload margin therefore depends on both of the supply voltage and the line output reference level. Table a-1 shows the maximum line output reference levels to satisfy overload margins of 12 dB and 15 dB. 12 dB of the overload margin is the minimum value specified by Dolby Laboratories.

Supply Voltage	Overload Margin	
	12dB	15dB
8V (±4V)	−3.0dBm (548mVrms)	−6.0dBm (388mVrms)
10V (±5V)	−0.5dBm (731mVrms)	−3.5dBm (518mVrms)
12V (±6V)	1.5dBm (921mVrms)	−1.5dBm (652mVrms)
15V (±7.5V)	3.5dBm (1.16Vrms)	0.5dBm (820mVrms)
20V (±10V)	6.0dBm (1.55Vrms)	3.0dBm (1.09Vrms)

Table a-1 Maximum line output level

2) Operation mode control

The CX20188/CXA1098Q provide fully electronic switching circuits. The functions are controlled by DC voltage of the two control pins of CAL/REC/PB and OFF/B/C. The switching truth table are shown in Table a-2. The switching levels are as follows

(a) Single ended supply operation

$V_{CC} \geqq VH \geqq V_{CC}/2+3V$

$V_{CC}/2+0.7V \geqq VM \geqq V_{CC}/2-0.7V$

$V_{CC}/2-3V \geqq VL \geqq GND$

$V_{CC}/2$ is not mathematical half of the supply voltage but the potential of the signal ground.

(b) Split supply operation

$V_{CC} \geqq VH \geqq 3V$

$0.7V \geqq VM \geqq -0.7V$

$-3V \geqq VL \geqq V_{EE}$

CAL/REC/PB	VH	VM	VL
Function	PB (Decode)	REC (Encode)	CAL

OFF/B/C	VH	VM	VL
Function	C type	B type	NR OFF

Table a-2 Switching truth table

The CAL (Calibration) mode is provided for the recording level and frequency response calibration functions of high grade cassette decks. It may also be used as an input muting function also. This mode functions as the encode mode basically, and selects CAL pin for the input pin.

It is desirable to provide CR time constant circuits at CAL/REC/PB and OFF/B/C pins with time constant from 100 msec to 1 sec, which will reduce switching clicks effectively.

3) Reference Levels

Characteristics and specifications of the Dolby noise reduction processor are defind and measured with reference to the Dolby level. This particular level in these devices is −10 dBm (245 mVrms), and is measured at the Test Point (VF IN) or the recording otuput (REC OUT). The input and output reference levels, which provide the Dolby level at the Test Point or the recording output in the NR off mode, are programmable with the external circuit.

The CX20188/CXA1098Q provide inductorless spectral skewing circuits, which are composed of a bootstrapped bridges-T circuit as shown in Fig. a-2. Resistors of R17 and R18 compose an attenuation circuit to determine the line output (LINE OUT) reference level. In Fig. a-2 the attenuation factor Hssk is defined as

$$Hssk = 20 \cdot \log (1 + R17/R18)$$

The line output reference level becomes

$$\text{Line output reference level} = Hssk - 10 \text{ [dBm]}$$

The parallel combination of R17 and R18 has to maintain a constant value to keep the specified spectral skewing characteristics. This particular resistance is 1.78 kΩ for 2.2 nF capacitance of C13 and C14. Table a-3 shows the usefull combinations of R17 and R18 for various applications. applications.

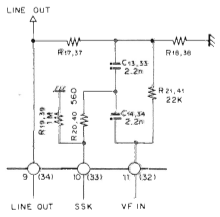


Fig. a-2

R17	R18	Line Output Reference Level	Supply Voltage
5.6kΩ	2.7kΩ	−0.2dBm (753mVrms)	≧11.0V (±5.5V)
4.3kΩ	3kΩ	−2.3dBm (596mVrms)	≧9.0V (±4.5V)
3.3kΩ	3.9kΩ	−4.7dBm (452mVrms)	≧8.0V (±4.0V)

Table a-3 Spectral skewing circuit attenuation

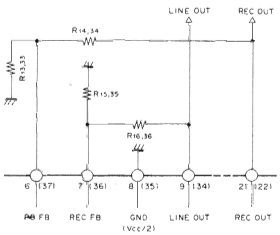


Fig. a-3

The reference level of the recording input (REC IN) and the play back input (PB IN) depend on the feedback factors of an operational amplifier MOA, which is an input switchable operational amplifier. In the recording mode the operational amplifier MOA composes the fixed gain amplifier with the feedback path of R15 and R16, and drives the encode processor. In the play back mode the output of the encode processor (REC OUT) is fed back to the inverting input (PB FB) of the operational amplifier. The transfer function of the operational amplifier therefore becomes the inverted transfer function of the encode processor, and operates as the decoder. The reference levels of the recording input (REC IN) and the play back input (PB IN) are as follows

$$\text{Recording input reference level} = \text{Line output reference level} - H_{REC} \text{ [dBm]}$$

$$\text{Play back input reference level} = -10 - H_{PB} \text{ [dBm]}$$

where, H_{REC} and H_{PB} are the feedback factors in the encode mode and decode mode respectively.

$$H_{REC} = 20 \cdot \log (1 + R16/R15)$$

$$H_{PB} = 20 \cdot \log (1 + R14/R13)$$

Increase of the recording input sensitivity will degrade the overall noise reduction effect, which has to satisfy more than 17 dB of the specified minimum value. A recommendable recording input sensitivity is approximately −25 dBm (44 mVrms). The range of the allowable play back input sensitivity will be limited by the open loop gain and the phase margin in the play back mode. A recommendable range of the play back input sensitivity it from −32 dBm (19 mVrms) to −25 dBm (44 mVrms).

4) Notes on Application

Application circuits of Fig. a-5 and Fig. a-6 show capacitors of C25, C26, C45 and C46 in the LLS and HLS weighting circuits.

We guarantee the encode error specified in the data sheet without these capacitors. However, we recommend to include the capacitors for three head cassette decks in which independent processors are provided for encode and decode processors respectively.

For example, combination of a device with positive error and a device with negative error may generates significant frequency response error, even if the devices are within specified limit. These capacitors will improve the encode error due to offset voltages of the level detectors.

(a) Encode Processor with Split Supply (Fig. a-5) will reduce the encode error.

Supply voltage : ±8Vtyp. (±6 to ±10V)
Line output level : −0.2 dBm (753 mVrms)
Recording output level : −10 dBm (245 mVrms)
Recording input level : −24.3 dBm (47 mVrms)

This circuit is suitable for three head cassette decks.

(b) Decode Processor with Split Supply (Fig. a-6)

Supply voltage : ±8Vtyp. (±6 to ±10V)
Line output level : −0.2 dBm (753 mVrms)
Play back input level : −30 dBm (25 mVrms)

This circuit is suitable for three head cassette decks.

(c) Switchable Processor with Split Supply (Fig. a-7)

Supply voltage : ±8Vtyp. (±6 to ±10V)
Line output level : −0.2 dBm (753 mVrms)
Recording output level : −10 dBm (245 mVrms)
Recording input level : −24.3 dBm (47 mVrms)
Play back input level : −30 dBm (25 mVrms)

This circuit is suitable for high grade two head cassette decks.

(d) Switchable Processor with Single Ended Supply (Fig. a-8)

Supply voltage : +14V typ. (9 to 20V)*
Line output level : −2.3 dBm (596 mVrms)
Recording output level : −10 dBm (245 mVrms)
Recording input level : −24.6 dBm (46 mVrms)
Play back input level : −30 dBm (25 mVrms)

This circuit is most appropriate for general applications.

* **Note)** Change C20 and C40 to 0.1 μF when Vcc is below +12V.

(e) Decode Processor with AUX input (Fig. a-9)

Supply voltage : +9V typ. (8 to 20V)*
Line output level : −4.7 dBm (452 mVrms)
Recording output level : −10 dBm (245 mVrms)
AUX input level : −30.2 dBm (23 mVrms)
Play back input level : −30 dBm (25 mVrms)

This unique application providing AUX input is suitable for car stereo players and car stereo cassette decks. AUX input will be usefull for a tuner input. CAL/REC/PB switching operates as the switching of AUX/Tape. The operation in the AUX input mode is independent of the switch position of OFF/B/C. When AUX input is unnecessary, C2, C11, C31, R3, R11, R31, R15, R16, R35 and R36 can be omitted. Refer to Fig. a-6.

* **Note)** Change C20 and C40 to 68 nF when Vcc is upon +12V.

(f) Application for Dubbing Cassette Decks

The CX20188/CXA1098Q simplify the structure of dubbing decks. Conventional dubbing decks utilize the Dolby processors commonly for two systems. Problems occur on the dubbing mode of a Dolby NR encoded tape. Listeners will be forced to monitor non-decoded sound. This device offers a simple solution, which is to utilize the recording output signal in the play back mode as shown in Fig. a-4. In the dubbing mode the processor operates as a decode (play back) mode. The monitor (line output) signal from the deck A will be decoded if necessary, however, the deck B will record directly without decoding. This special application is possible because this device generates a non-decoded signal at the recording output in the decode mode even though it operates on the B type or C type NR.

Application for Dubbing Deck

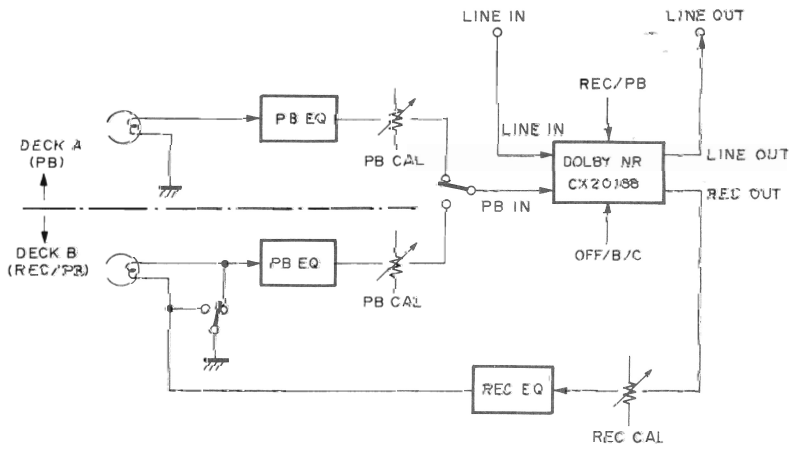
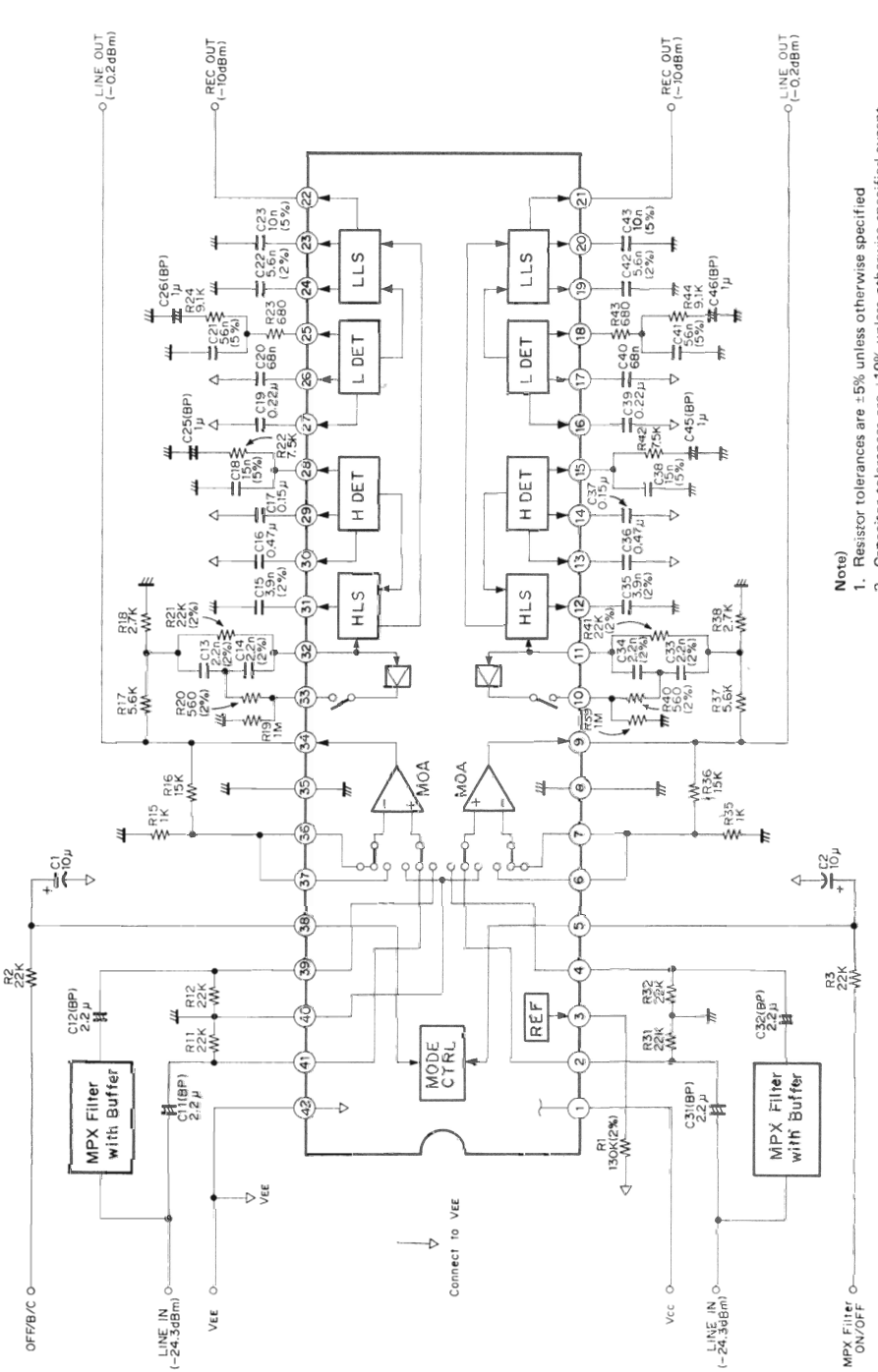


Fig. a-4

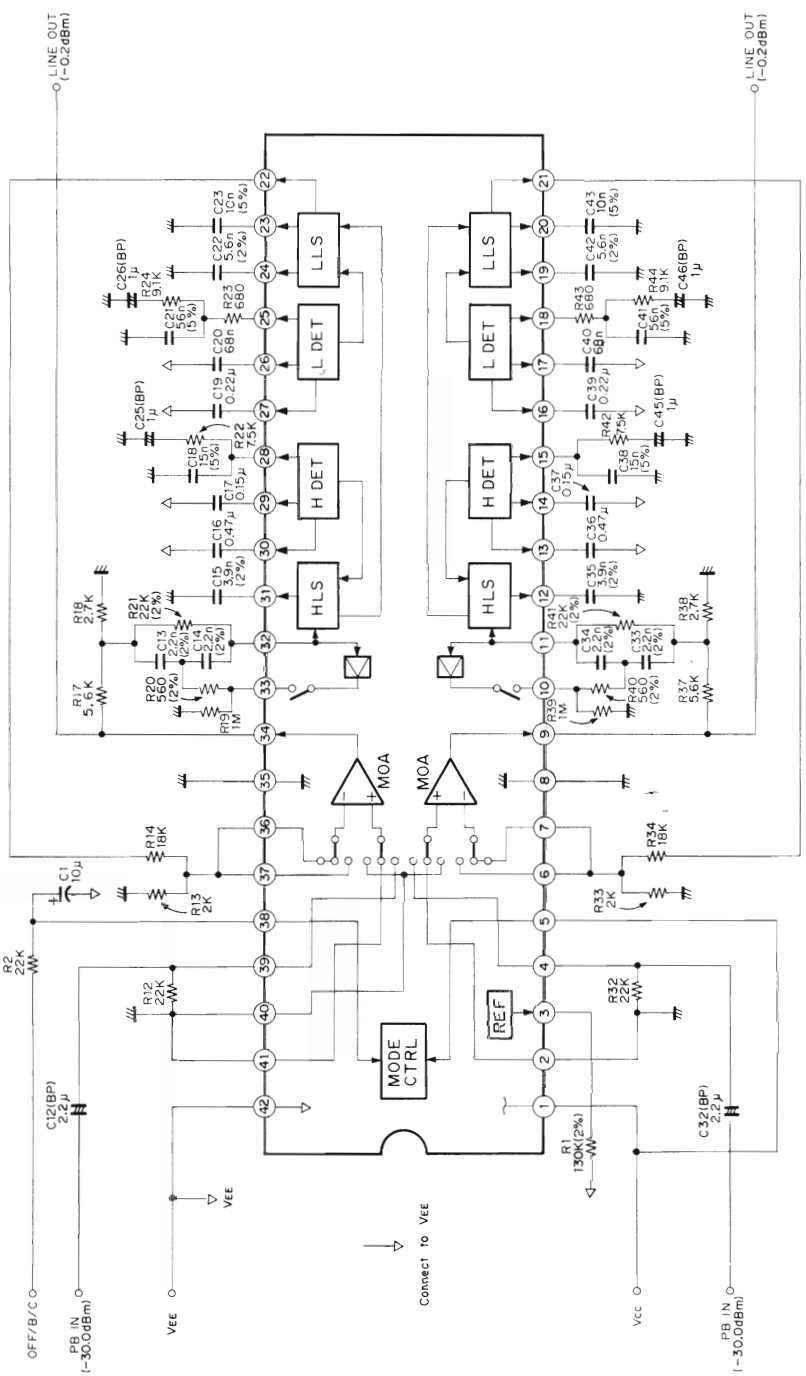
Encode Processor with Split Supply for 3 Head Cassette Deck



Note)
1. Resistor tolerances are ±5% unless otherwise specified
2. Capacitor tolerances are ±10% unless otherwise specified except for coupling capacitors
3. CXA1098Q refer to the pin configuration

Fig. a-5

Decode Processor with Split Supply for 3 Head Cassette Deck

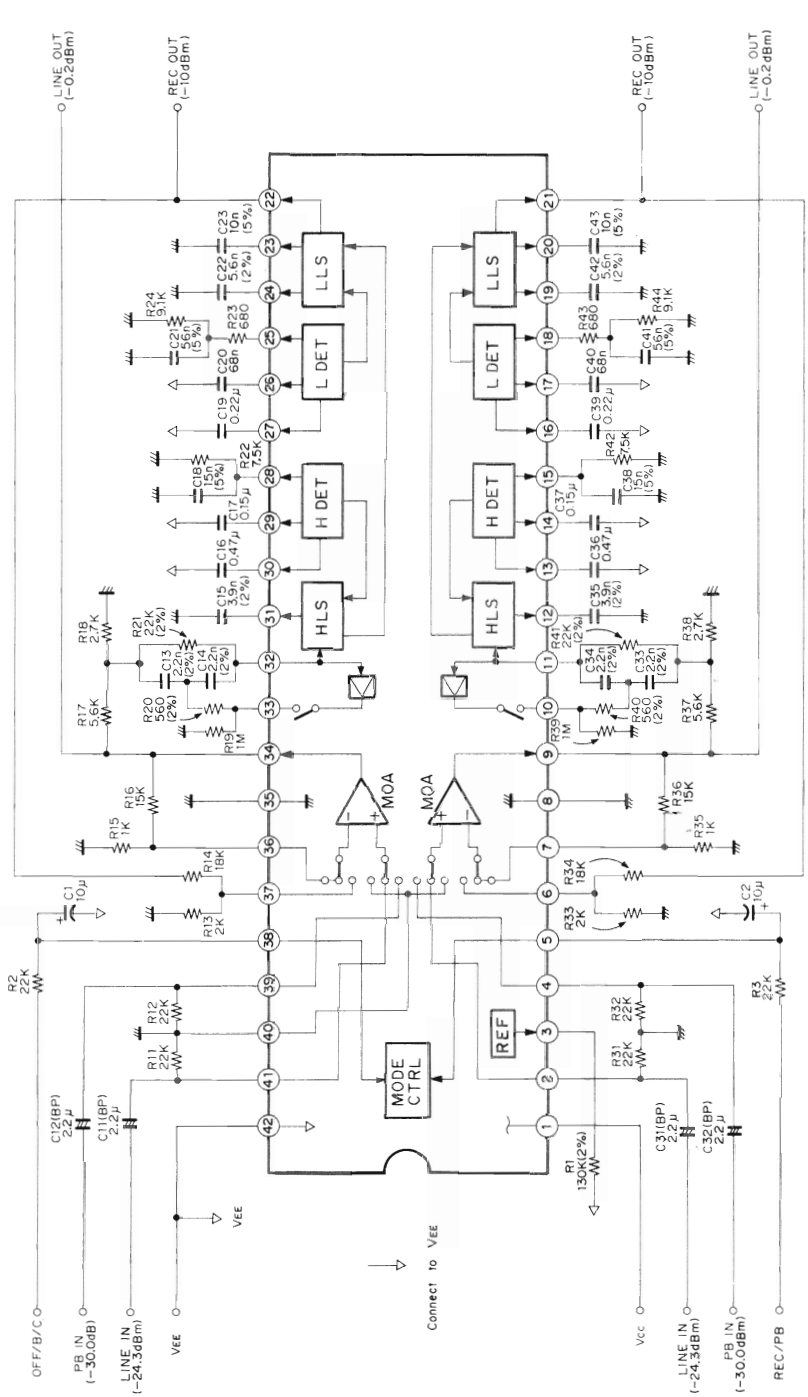


Note)

1. Resistor tolerances are ±5% unless otherwise specified
2. Capacitor tolerances are ±10% unless otherwise specified except for coupling capacitors
3. CXA1098Q refer to the pin configuration

Fig. a-6

Switchable Processor with Split Supply

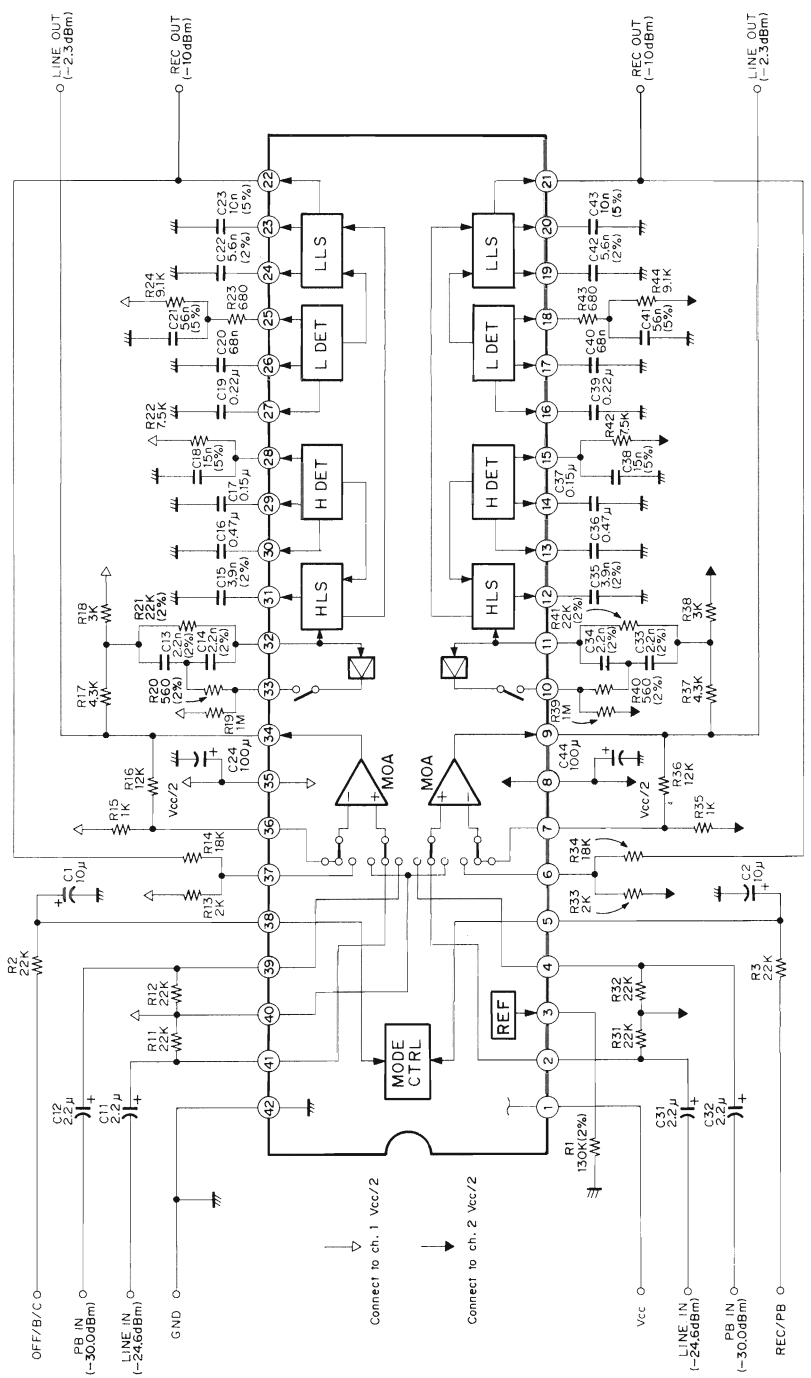


Note)

1. Resistor tolerances are ±5% unless otherwise specified
2. Capacitor tolerances are ±10% unless otherwise specified except for coupling capacitors
3. CXA1098Q refer to the pin configuration

Fig. a-7

Switchable Processor with Single Supply

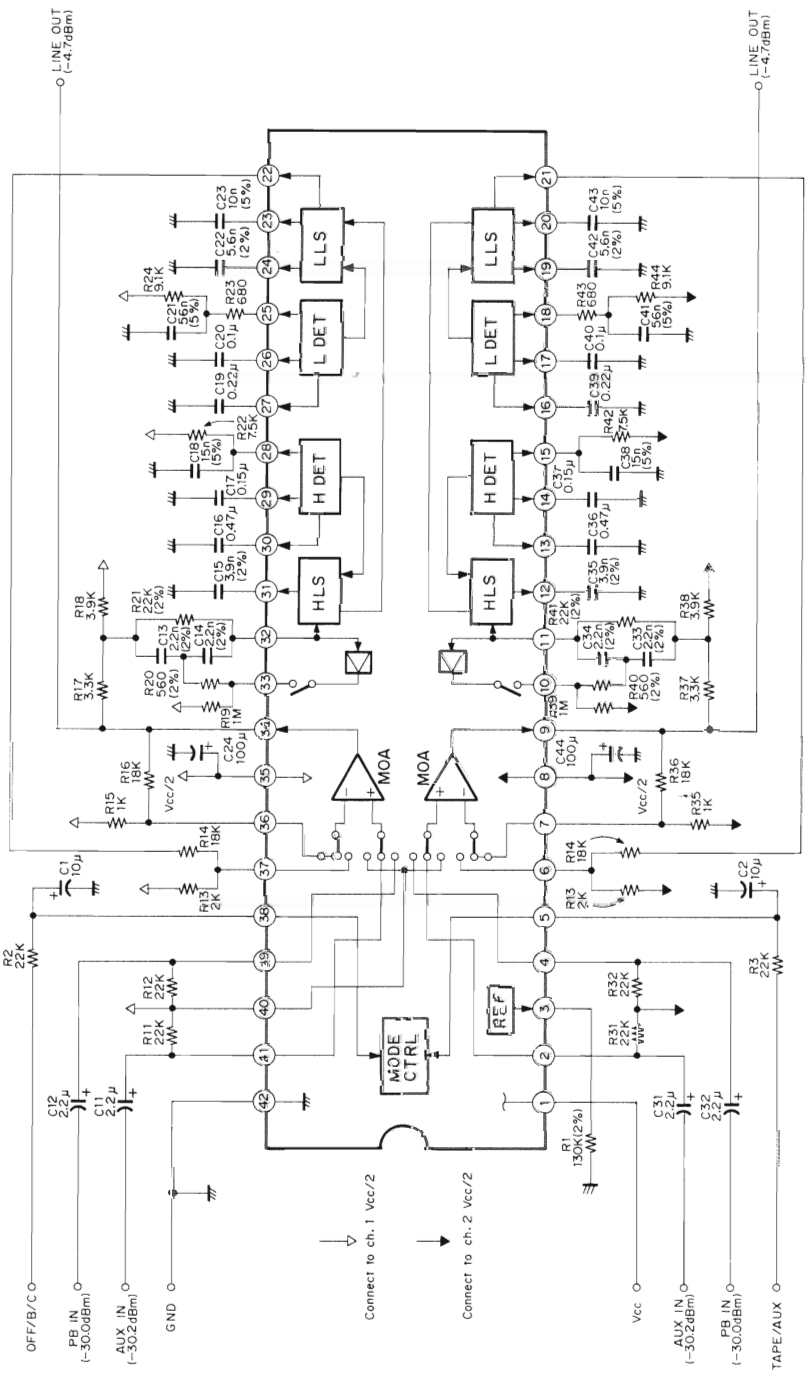


Note)

1. Resistor tolerances are ±5% unless otherwise specified
2. Capacitor tolerances are ±10% unless otherwise specified except for coupling capacitors
3. CXA1098Q refer to the pin configuration

Fig. a-8

Decode Processor with AUX Input for Car Stereo Players



Note)

1. Resistor tolerances are ±5% unless otherwise specified
2. Capacitor tolerances are ±10% unless otherwise specified except for coupling capacitors
3. CXA1098Q refer to the pin configuration

Fig. a-9

SONY **CXA1057M**

Stereo Dolby B Type Noise Reduction

Description

The CXA1057M is a low-voltage stereo Dolby B type noise reduction system IC developed for exclusive playback of headphone audio units. This IC is so structured for stereo that it can easily be mounted on PCB and well balanced L and R channel performance can be obtained.

Features

- Very low supply voltage (1.7 to 3.2V)
- Very low supply current (NR ON, No signal: 7.4 mA)
- Minimum number of external components
- Full electronic switching (NR ON/OFF)

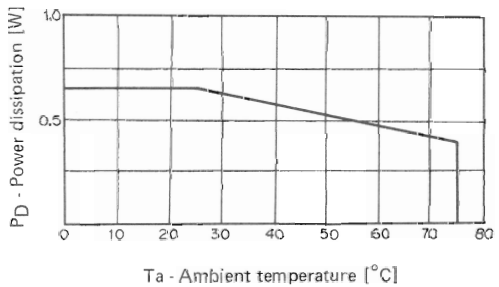
Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta=25°C)

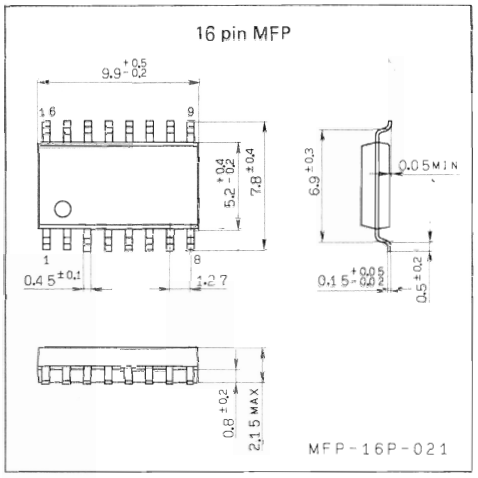
• Supply voltage	Vcc	5.0	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	658	mW

Power Consumption Derating Curve

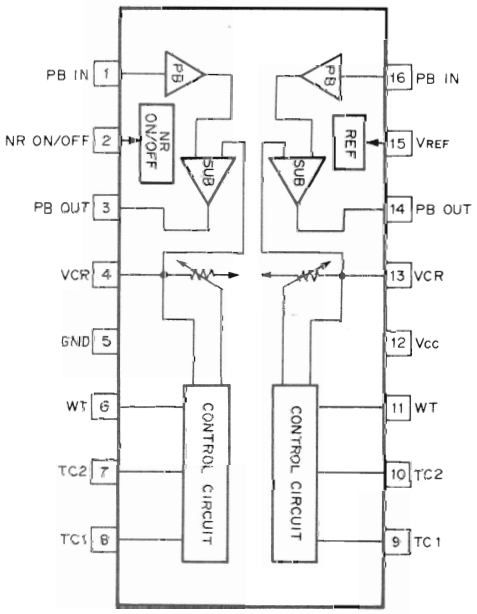


Package Outline

Unit: mm



Block Diagram (Top View)



CXA1057M

- This IC is available only to the licensees of Dolby Laboratories Corporation from whom licensing and application information may be obtained.
- "Dolby" and double D symbol are trade marks of Dolby Laboratories Licensing Corporation.

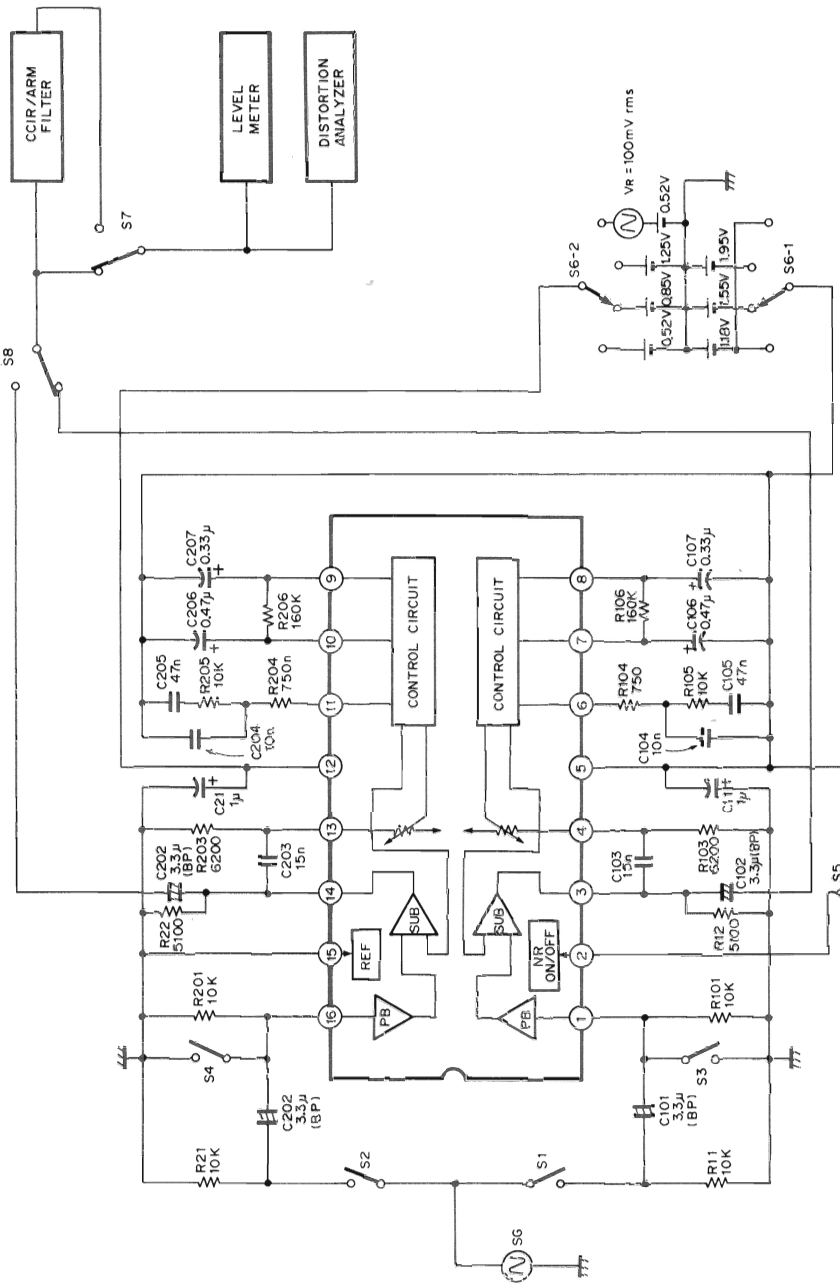
Electrical Characteristics

Ta=25°C, V_{CC}=2.4V, V_{REF}*2=1.55V, unless otherwise specified.
Dolby Level: −25 dBm=43.6 mVrms at PB OUT, f=400 Hz

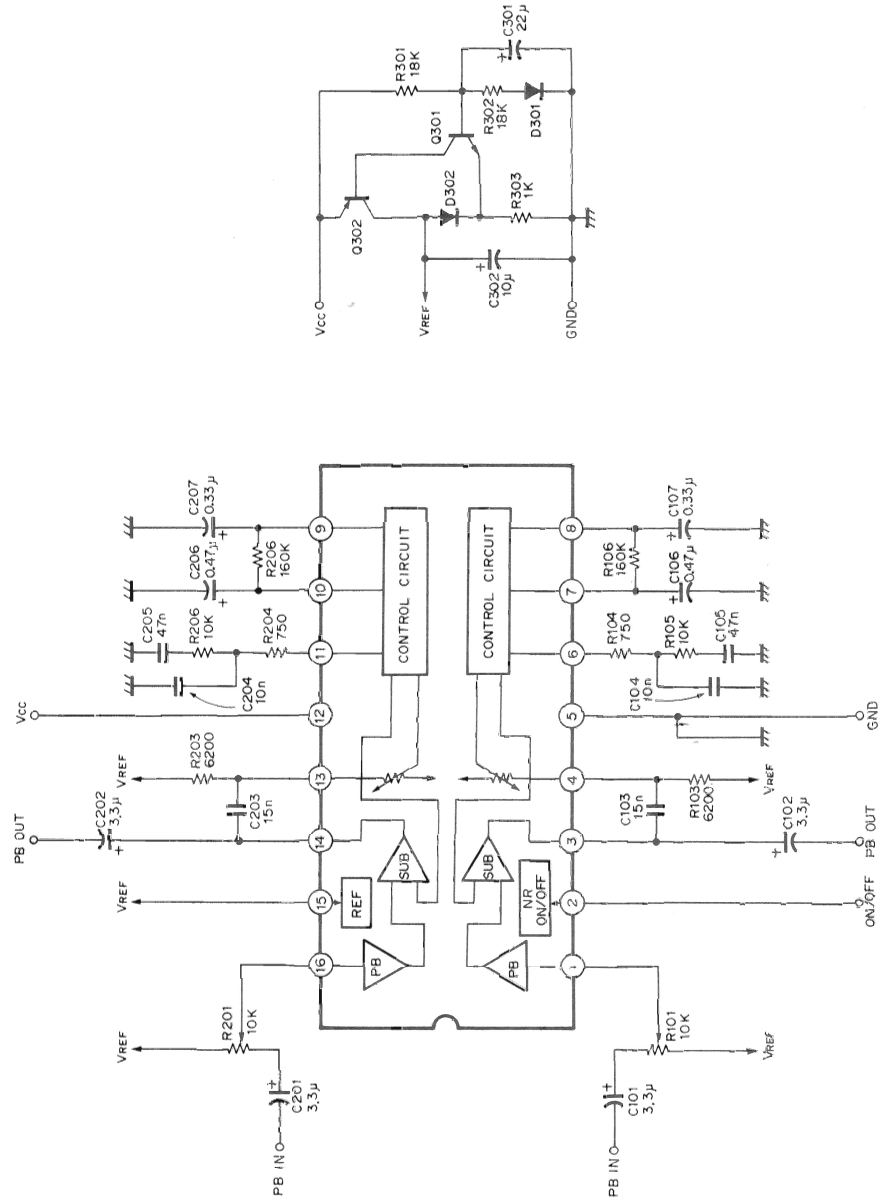
Characteristics	Symbol	Test Conditions*1				Min.	Typ.	Max.	Unit
		R/P	NR	f(Hz)	Other conditions				
Quiescent Current (1)	I_{CC}	P	OFF	—	No signal	3.3	4.8	6.3	mA
Quiescent Current (2)	I_{CC}	P	B	—	No signal	5.1	7.4	9.7	mA
Decode Cut B type (1)	B-P-1	P	B	1.4k	−20dB	3.2	4.4	5.6	dB
(2)	B-P-2	P	B	1.4k	−40dB	6.5	7.7	8.9	dB
(3)	B-P-3	P	B	5k	−20dB	2.0	3.2	4.4	dB
(4)	B-P-4	P	B	5k	−30dB	7.0	8.2	9.4	dB
(5)	B-P-5	P	B	10k	0dB	−0.8	0.4	1.6	dB
(6)	B-P-6	P	B	10k	−25dB	3.0	4.2	5.4	dB
(7)	B-P-7	P	B	10k	−40dB	9.8	10.4	11.9	dB
Frequency Characteristics	F-R	P	OFF	10k	refer to 1 kHz	−0.6	0.0	0.6	dB
Signal Handling	V_{omax}	P	B	1k	(PB OUT) V_{CC}=1.7V V_{REF}=1.18V THD=1%	12	14	—	dB
Total Harmonic Distortion NR OFF	THD (OFF)	P	OFF	1k	V_{CC}=1.7V V_{REF}=1.18V +10dB	—	0.14	0.50	%
Decode Gain	G_{PB}	P	OFF	400	PB IN—PB OUT	4.5	5.7	6.9	dB
B type S/N Ratio (CCIR)	SN (CCIR)	P	B	—	V_{CC}=3.2V V_{REF}=1.95V R_g=0Ω	70	86	—	dB
Crosstalk between Channels	CT	P	B	—	V_{CC}=1.7V V_{REF}=1.18V 0dB	—	−78	—	dB
Ripple Rejection Ratio		P	B	1k	V_{CC}=1.7V V_{REF}=1.18V V_R=100 mVrms	—	−48	−40	dB
Control Voltage "H" Level	VCH	—	—	—		1.6	—	—	V
"L" Level	VCL	—	—	—		—	—	0.35	V

*1: 0 dB=Dolby Level at PB OUT
*2: Voltage of pin 15

External Components and Test Circuit



Application Circuit



Notes on Application

1) Power supply

The CXA1057M is operated in the power supply voltage range of 1.7 to 3.2V with an overload margin of at least 12 dB.

As the power supply voltage is raised, so does the overload margin also.

The quiescent current has no strong dependability to the power supply voltage.

2) Reference voltage (V_{REF})

The CXA1057M is necessary to apply the reference voltage externally.

The relation between the supply voltage and the reference voltage is as shown in Fig. a-1.

Use of it within the oblique lined section is strongly recommended.

Furthermore, there are methods to supply the reference voltage from the basic application circuit and external circuit structure as shown in Fig. a-2, and other ICs which have the characteristics whose reference voltage characteristics lie within the oblique lined section as shown in Fig. a-1.

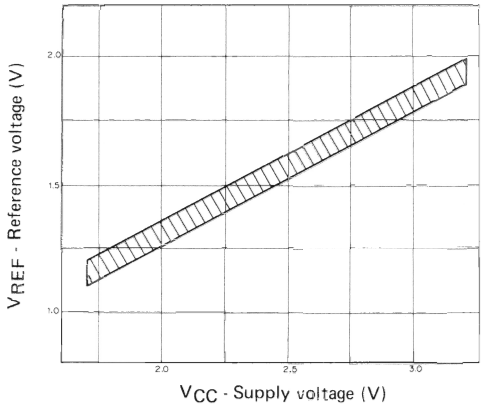


Fig. a-1. Reference voltage vs. Supply voltage

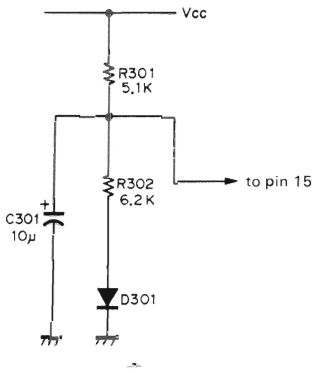


Fig. a-2. Reference voltage circuit

3) Operation mode control

All the functions of CXA1057M are controlled by the electronic switch. The switching of the operation modes is carried out by DC voltages of NR ON/OFF control pin. The operation modes and their values are shown in Table below.

NR ON/OFF	"VH"	"VL"
Condition	OFF	ON

$GND \leqq VL \leqq 0.35V$, $1.0V \leqq VH \leqq Vcc$

Table a-1. Operation modes

4) Reference level

The characteristics of the Dolby noise reduction processor is defined as the Dolby level.

This special level in the CXA1057M is −25 dBm (43.6 mVrms) at f=400 Hz, and it can be measured at the playback output pin (PB OUT) at NR OFF.

The input sensitivity of the playback output pin corresponding to the dolby level is −31 dBm (21.8 mVrms).

5) Application circuit

Decode Processor without Filter. (Fig. a-3)

It is suitable for exclusive playback of headphone audio units.

Decode Processor without Filter

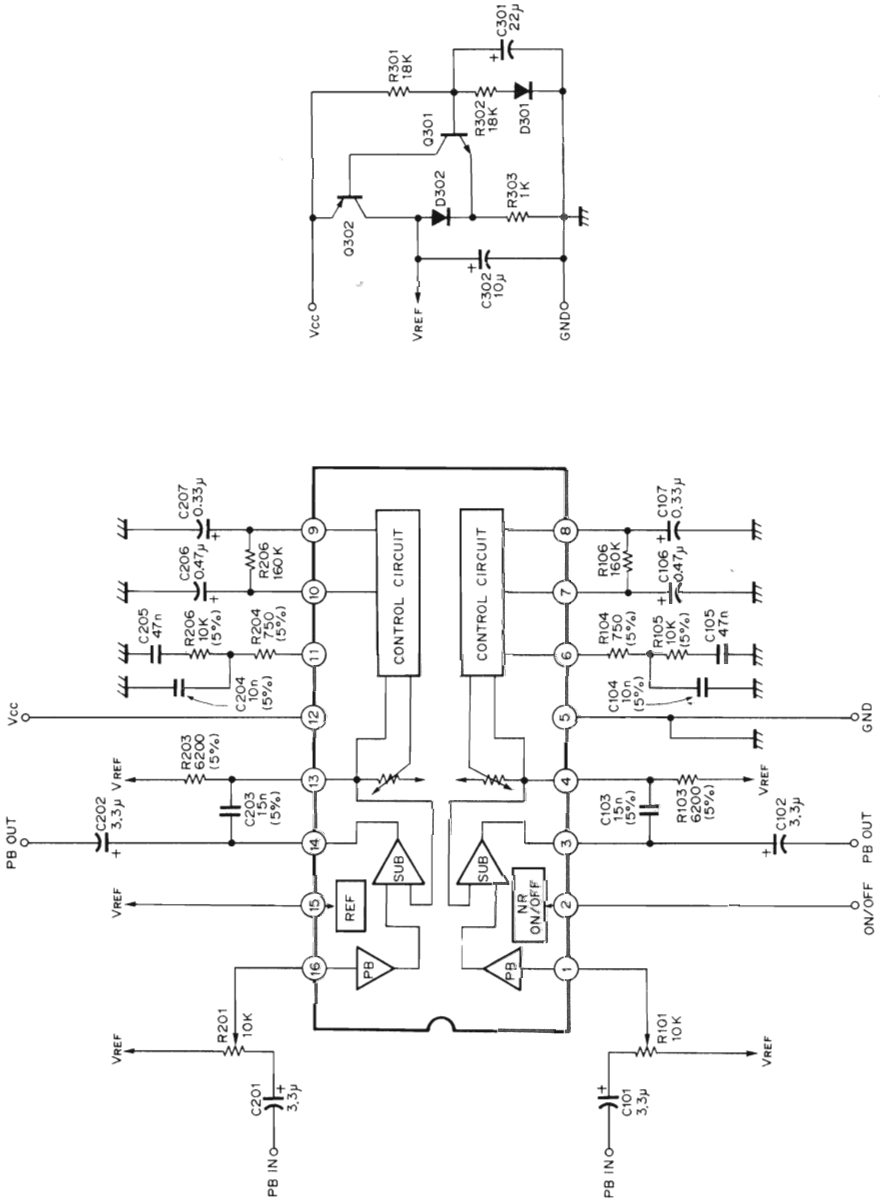
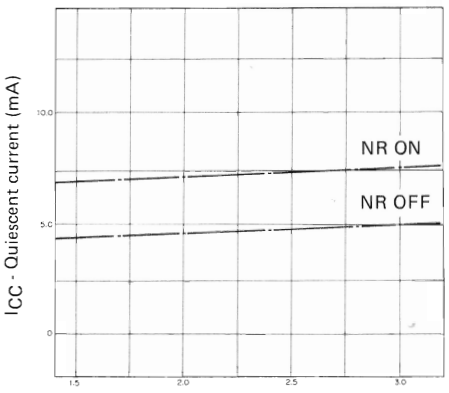
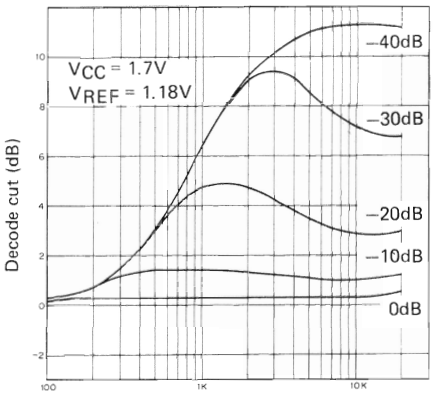


Fig. a-3.

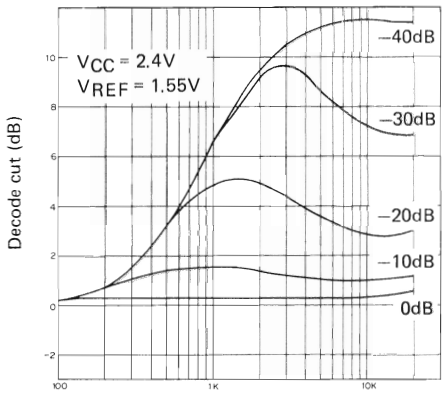
Quiescent current vs. Supply voltage



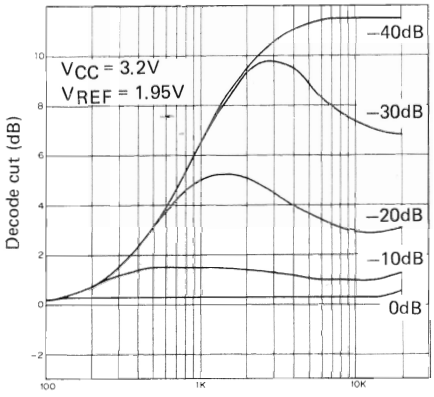
Decoding characteristics



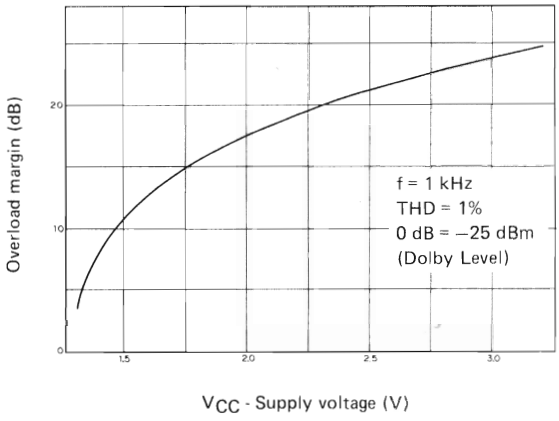
Decoding characteristics



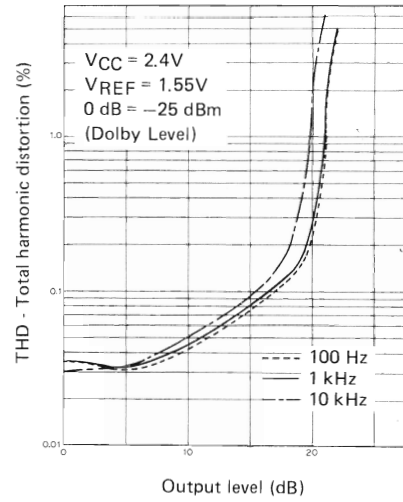
Decoding characteristics



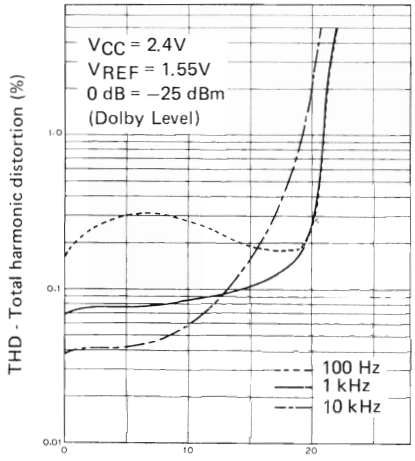
NR ON overload margin



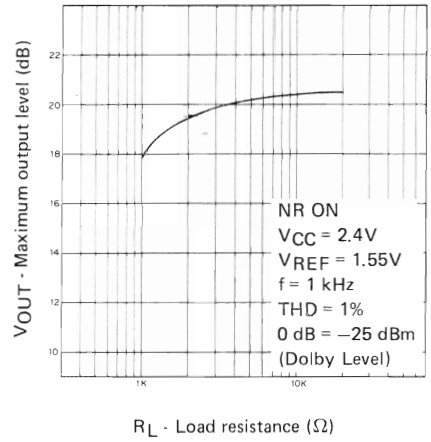
NR OFF total harmonic distortion



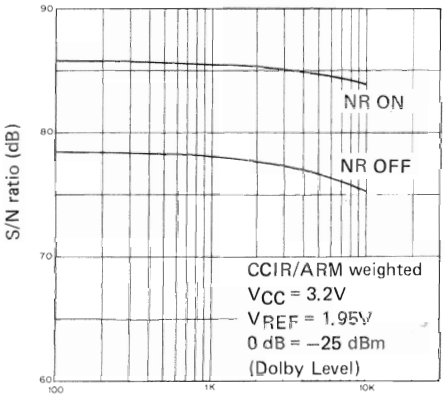
NR ON total harmonic distortion



Drive capability

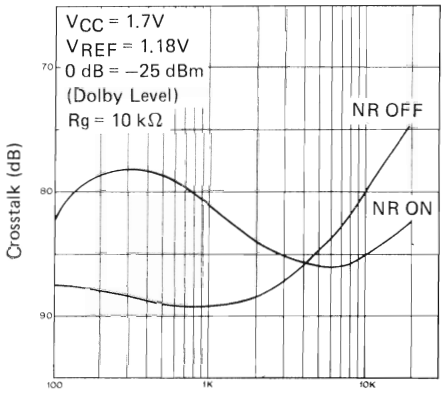


S/N ratio vs. Source impedance



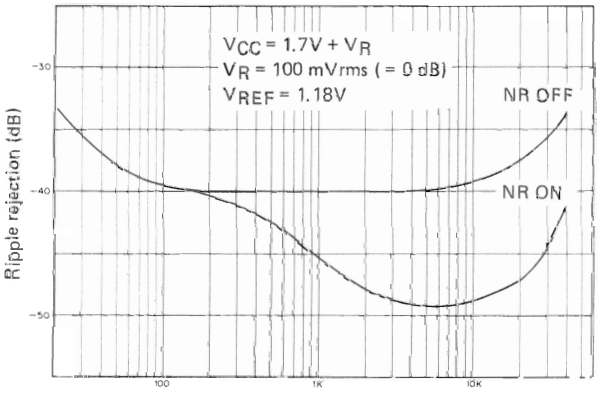
Rg - Source impedance (Ω)

Crosstalk between channels



f - Frequency (Hz)

Ripple rejection ratio vs. Frequency



f - Frequency (Hz)

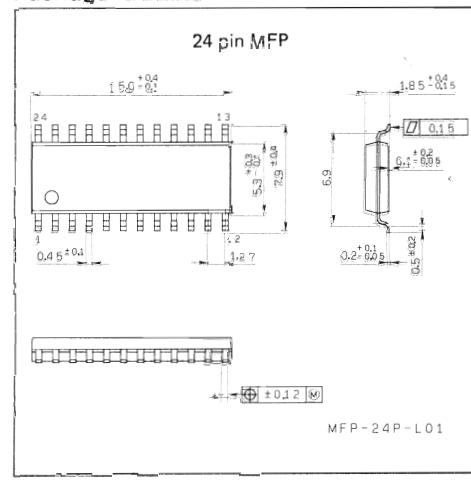
Stereo Dolby B Type Noise Reduction

Description

The CXA1058M is a low-voltage stereo Dolby B type noise reduction system IC developed for recording/playback of headphone audio units. This IC is so structured for stereo that it can easily be mounted on PCB and well balanced L and R channel performance can be obtained.

Package Outline

Unit: mm



Features

- Very low supply voltage (1.7 to 3.2V)
- Very low supply current (NR ON, No signal: 7.4 mA)
- Provides input/output pins for both REC and PB channels
- Minimum number of external components
- Full electronic switching (NR ON/OFF, REC/PB)
- Provides a mute output

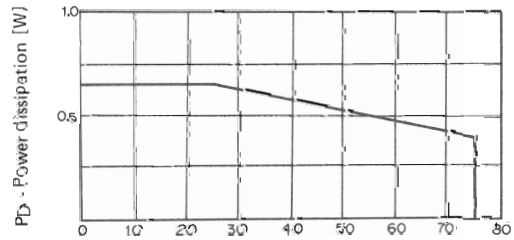
Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta=25°C)

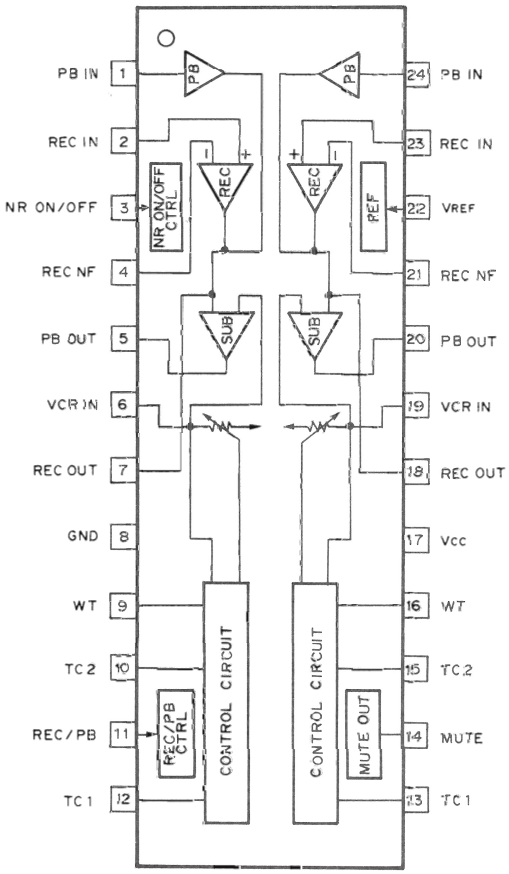
• Supply voltage	Vcc	5.0	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	Pd	656	mW

Power Consumption Derating Curve



- This IC is available only to the licensees of Dolby Laboratories Corporation from whom licensing and application information may be obtained.
- "Dolby" and double D symbol are trade marks of Dolby Laboratories Licensing Corporation.

Block Diagram and Pin Configuration (Top View)



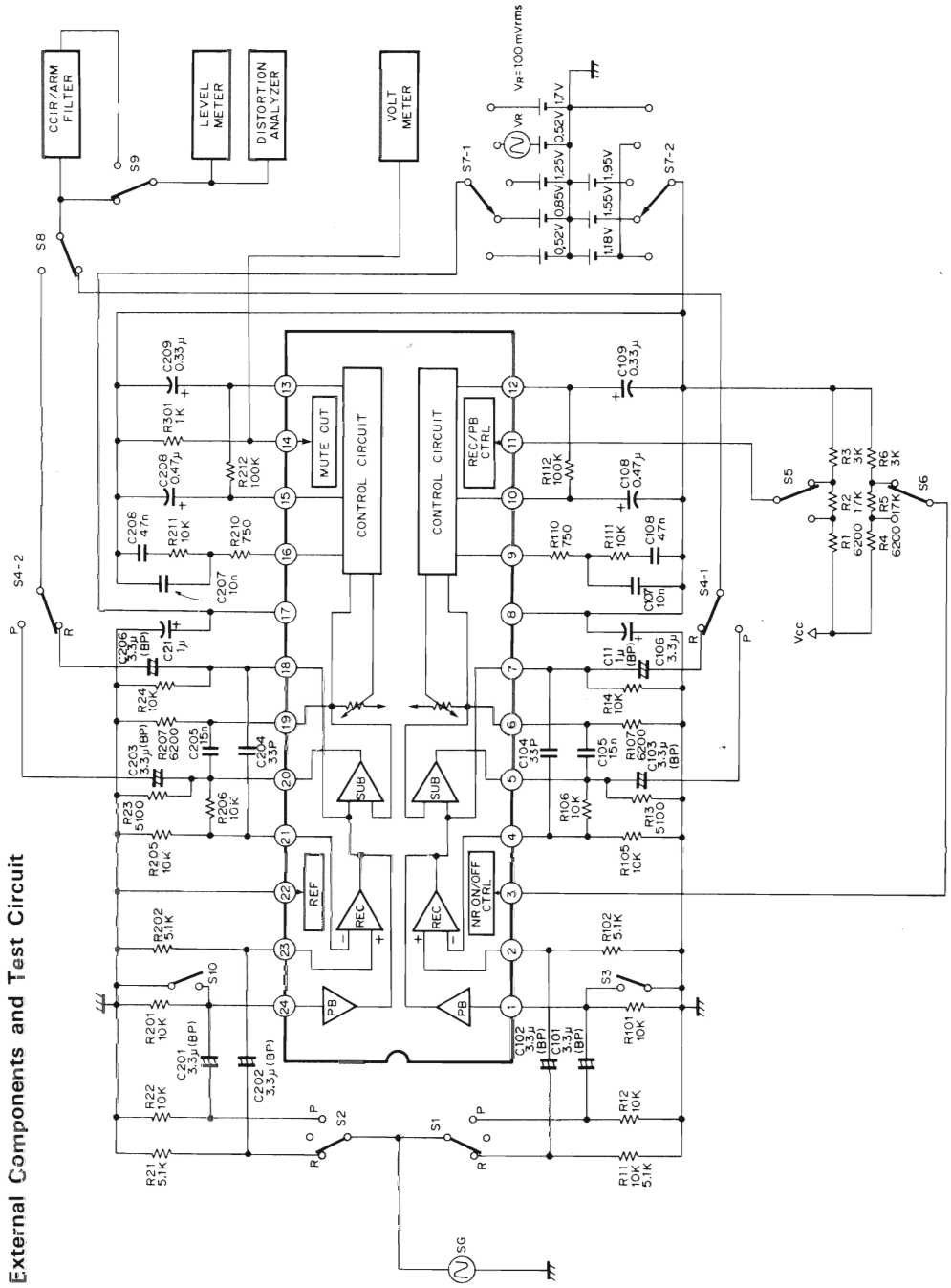
Electrical Characteristics

(Ta=25°C, Vcc=2.4V, VREF*2=1.55V, unless otherwise specified
Dolby Level: −25 dBm=43.6 mVrms at PB OUT, f=400 Hz)

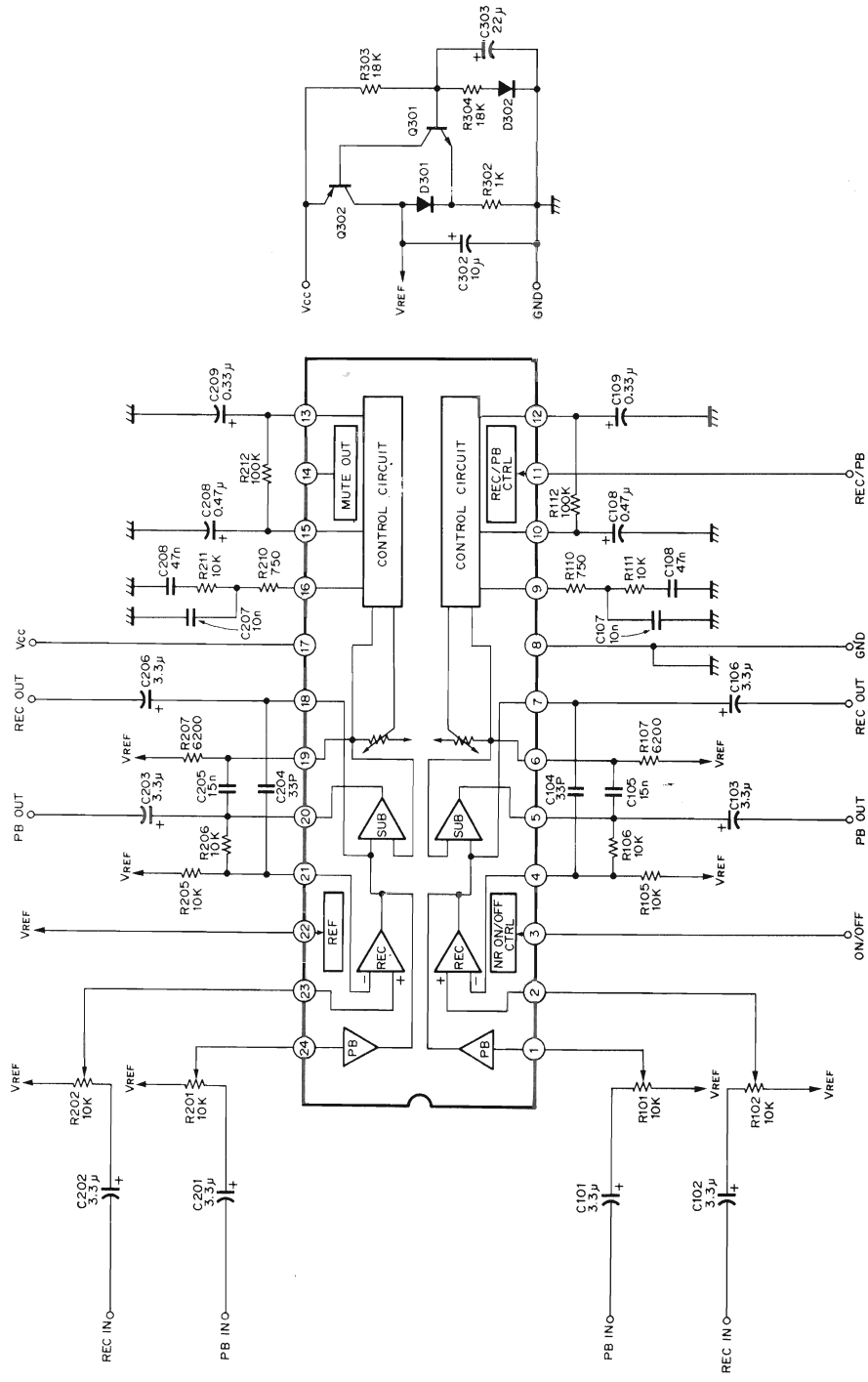
Characteristics	Symbol	Test Conditions*1				Min.	Typ.	Max.	Unit
		R/P	NR	f(Hz)	Other conditions				
Supply Current (1)	Icc	P	OFF	—	No signal	3.3	4.8	6.3	mA
Supply Current (2)	Icc	P	B	—	No signal	5.1	7.4	9.7	mA
Encode Characteristics (boost)									
B type (1)	B-R-1	R	B	1.4k	−20dB	3.2	4.4	5.6	dB
(2)	B-R-2	R	B	1.4k	−40dB	6.5	7.7	8.9	dB
(3)	B-R-3	R	B	5k	−20dB	2.0	3.2	4.4	dB
(4)	B-R-4	R	B	5k	−30dB	7.0	8.2	9.4	dB
(5)	B-R-5	R	B	10k	0dB	−0.8	0.4	1.6	dB
(6)	B-R-6	R	B	10k	−25dB	3.0	4.2	5.4	dB
(7)	B-R-7	R	B	10k	−40dB	9.8	10.4	11.9	dB
Frequency Response	F-R	P	OFF	10k	refer to 1 kHz	−0.6	0.0	0.6	dB
Overload Margin	$V_{o\ max}$	P	B	1k	(PB OUT) Vcc=1.7V VREF=1.18V THD=1%	12	14	—	dB
Total Harmonic Distortion NR OFF	THD (OFF)	P	OFF	1k	+10dB Vcc=1.7V VREF=1.18V	—	0.14	0.50	%
Decode Gain	GPB	P	—	400	PB IN—REC OUT	4.5	5.7	6.9	dB
B type					Vcc=3.2V VREF=1.95V				
S/N Ratio (CCIR)	S/N (CCIR)	R	B	—	R_g=2.5kΩ	65	68	—	dB
		P	B	—	R_g=0Ω	70	86	—	dB
Crosstalk					Vcc=1.7V VREF=1.18V				
REC-PB	CT-(1)	P	B	1k	0dB	—	−88	—	dB
PB-REC	CT-(2)	R	B	1k	0dB	—	−74	—	dB
Between Channels PB	CT-(3)	P	B	1k	0dB	—	−78	—	dB
Ripple Rejection Ratio	RRR	P	B	1k	Vcc=1.7V VREF=1.18V VR=100 mVrms	—	−48	−40	dB
Control voltage									
"H" level	V-CH	—	—	—		1.0	—	—	V
"L" level	V-CL	—	—	—		—	—	0.35	V

*1. Dolby level at 0 dB = PB OUT
*2. Voltage of pin 22

External Components and Test Circuit



Application Circuit



Notes on Application

1) Power supply

The CXA1058M is operated in the power supply voltage range of 1.7 to 3.2V with an overload margin of at least 12 dB.

As the power supply voltage is raised, so does the overload margin also.

The quiescent current has no strong dependability to the supply voltage.

2) Reference voltage (V_{REF})

The CXA1058M is necessary to apply the reference voltage externally.

The relation between the supply voltage and the reference voltage is as shown in Fig. a-1.

Use of it within the oblique lined section is strongly recommended.

Furthermore, there are methods to supply the reference voltage from the basic application circuit and external circuit structure as shown in Fig. a-2, and other ICs which have the characteristics similar to that of the CX20023 (3V REC/PB dual amplifier) manufactured by SONY, etc, whose reference voltage characteristics lie within the oblique lined section as shown in Fig. a-1.

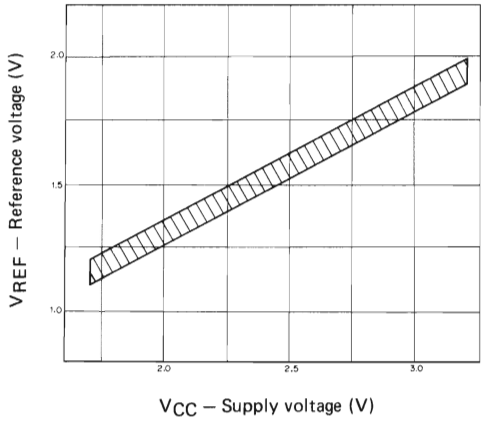


Fig. a-1. Reference voltage vs. Supply voltage

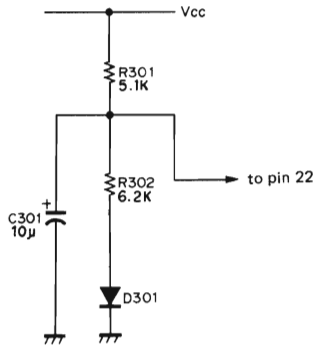


Fig. a-2. Reference voltage circuit

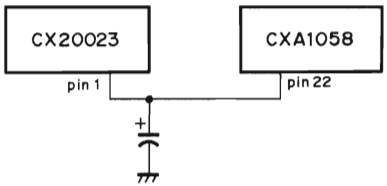


Fig. a-3. Reference voltage is supplied from CX20023

3) Operation mode control

All the functions of the CXA1058M are controlled by the electronic switch. The switching of the operation modes is carried out by DC voltages of 2 control pins; namely, REC/PB and NR ON/OFF. The operation modes and their values are shown in Table below.

Table a-1. Operation Modes

NR ON/OFF	"VH"	"VL"
Condition	OFF	ON

REC/PB	"VH"	"VL"
Condition	REC (Encode)	PB (Decode)

$GND \leqq VL \leqq 0.35V,\ 1.0V \leqq VH \leqq Vcc$

4) Reference level

The characteristics of the Dolby noise reduction processor is defined as the Dolby level.
This special level in the CXA1058M is −25 dBm (43.6 mVrms) at f=400 Hz, and it can be measured at the playback-output pin (PB OUT) at NR OFF.
The input sensitivity of the playback output pin corresponding to the dolby level is −31 dBm (21.8 mVrms) during playback and becomes as follows with variation during recording.

$$\text{(Recording Input Level) (dBm)} = \text{(Dolby Level)} - 20 \log \left(\frac{R106}{R105}+1\right)$$
$$= \text{(Dolby Level)} - 20 \log \left(\frac{R206}{R205}+1\right)$$

5) Mute output

During the duration when the power is turned ON and the reference voltage of the CXA1058M becomes to its normal state, it generates the pulse shape voltage. Mute can be applied by utilizing this voltage. The maximum current of this mute pin (pin 14) is 1 mA.

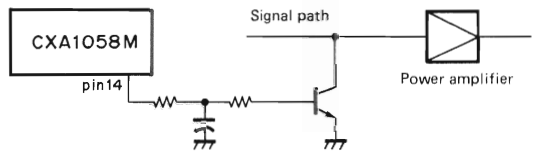


Fig. a-4. Mute

6) Application circuit

(a) Switchable Processor with Multiplex Filter (Fig. a-5)
It is suitable for the cassette recorder or compound units which is necessary to operate the processor in either the encode or decode mode.

(b) In case the CXA1058M is desired to be used for only playback, it is recommended to use the exclusive playback stereo dolby B type noise reduction system IC CXA1057M (16 pin MFP) manufactured by SONY corp.

Switchable Processor with Multiplex Filter

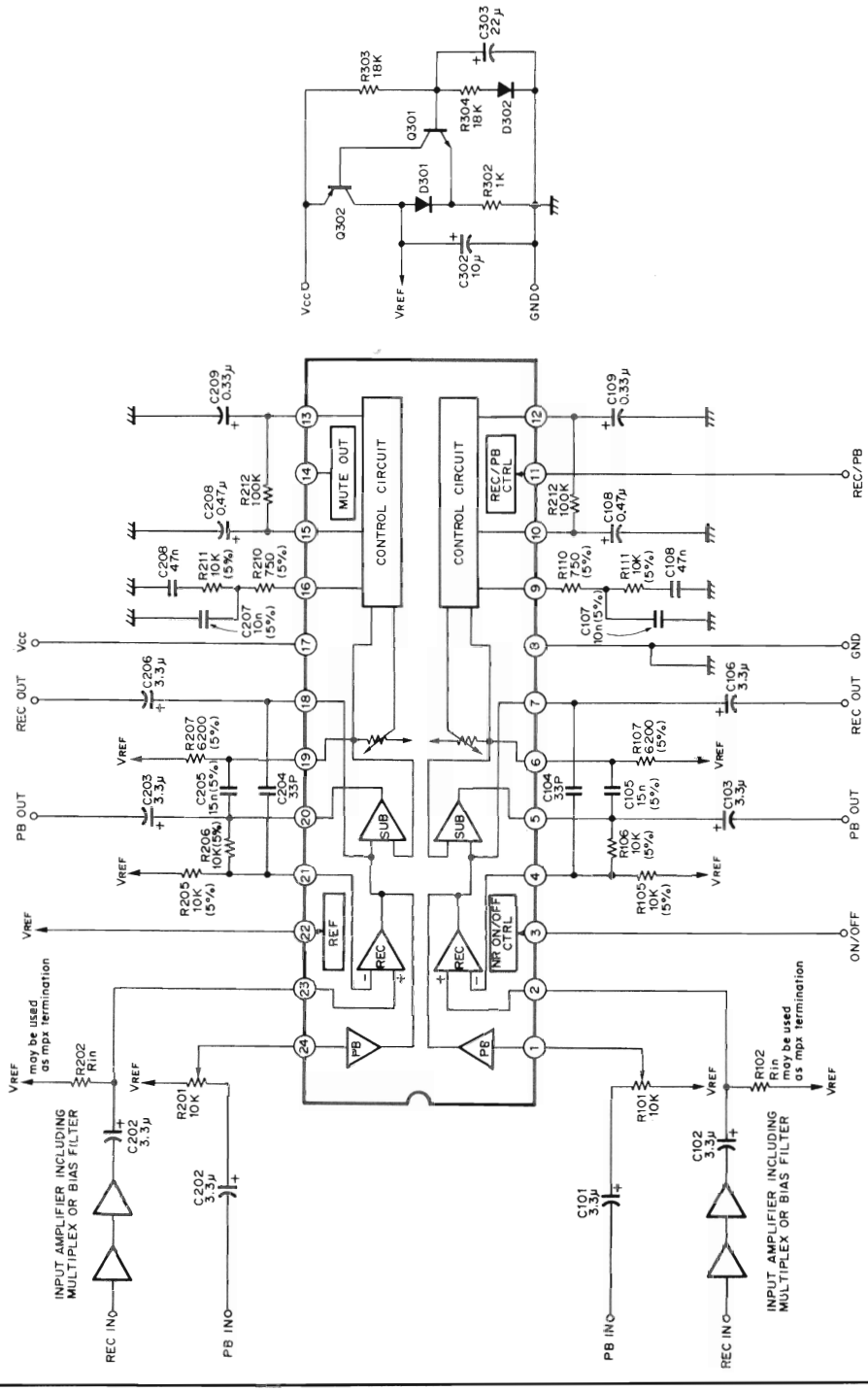
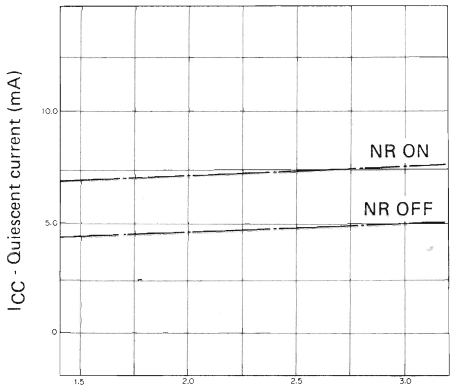
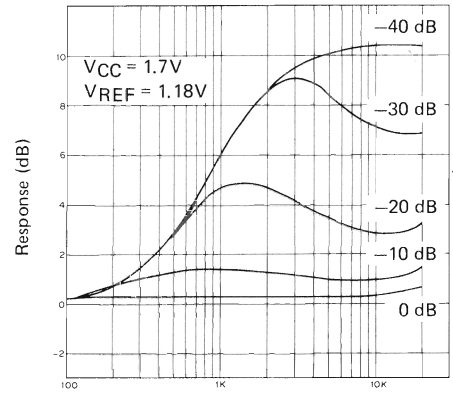


Fig. a-5.

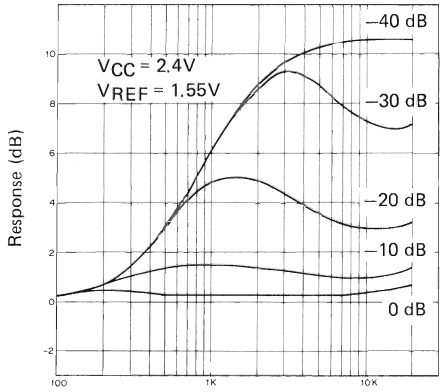
Quiescent current vs. Supply voltage during non-signal



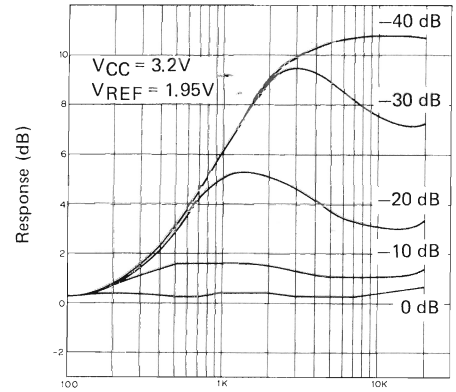
Encode characteristics



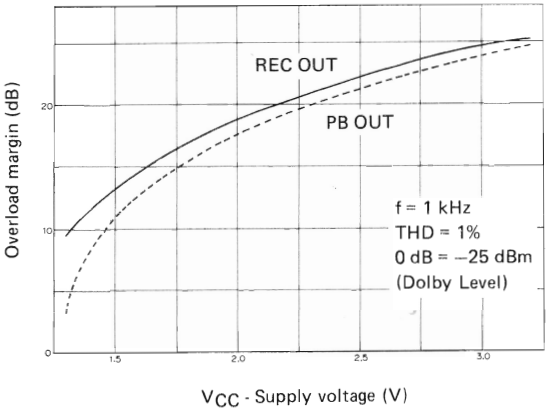
Encode characteristics



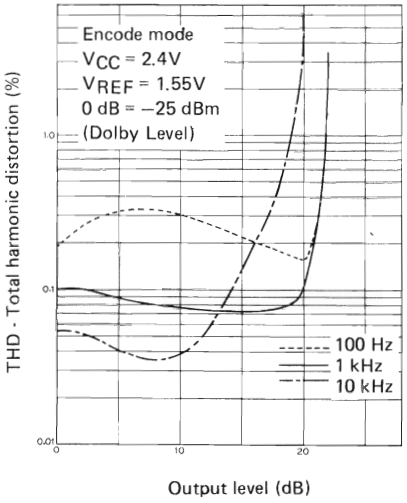
Encode characteristics



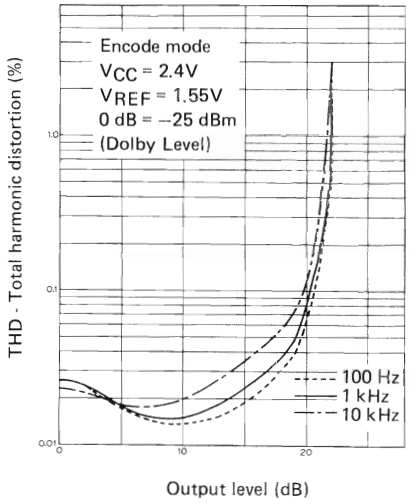
NR ON overload margin



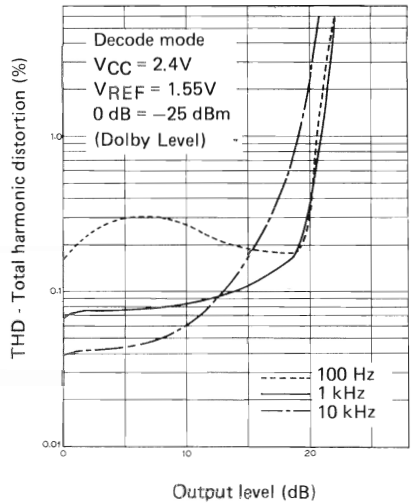
NR ON total harmonic distortion



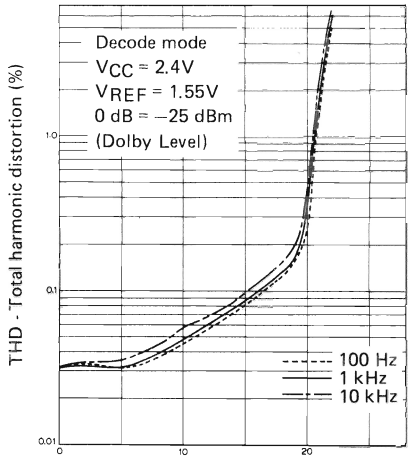
NR OFF total harmonic distortion



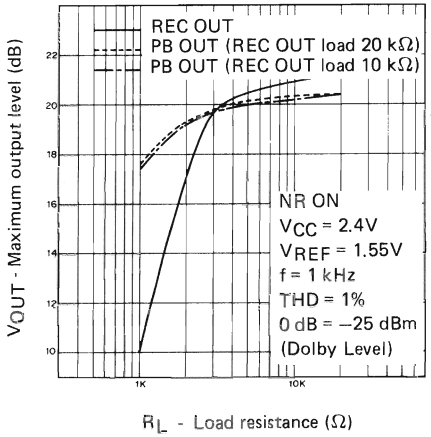
NR ON total harmonic distortion



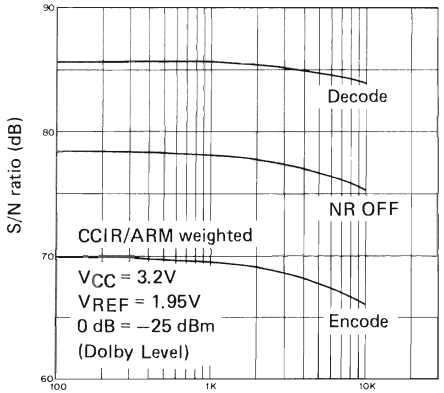
NR OFF total harmonic distortion



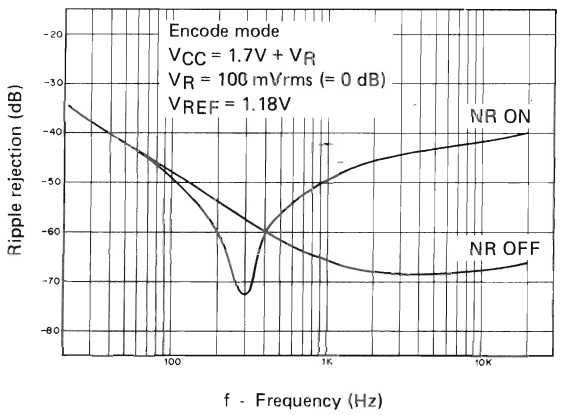
Drive capability



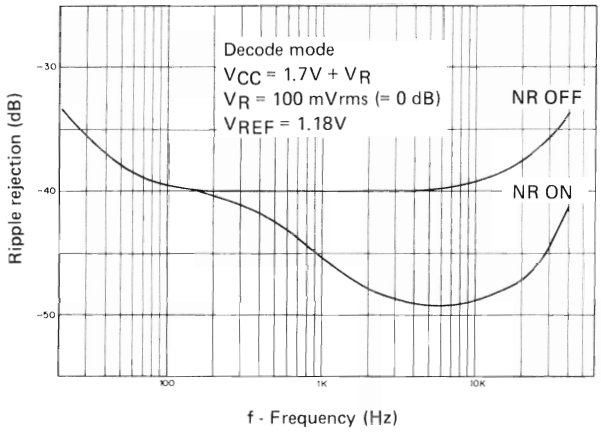
S/N ratio vs. Source impedance



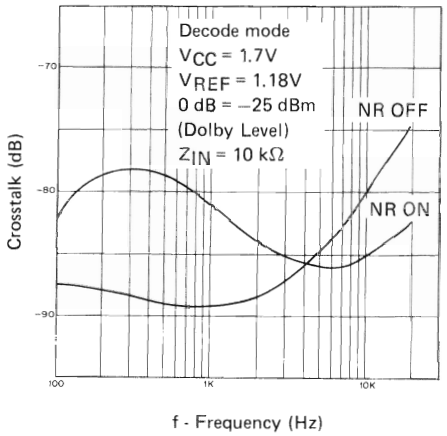
Ripple rejection ratio vs. Frequency



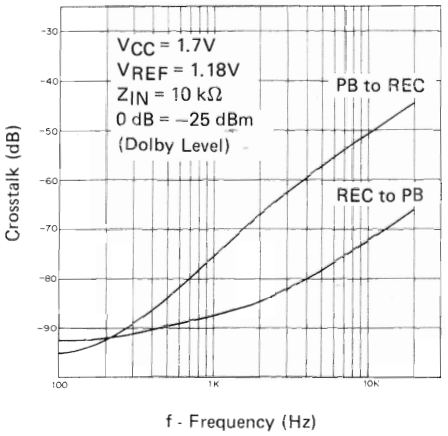
Ripple rejection ratio vs. Frequency

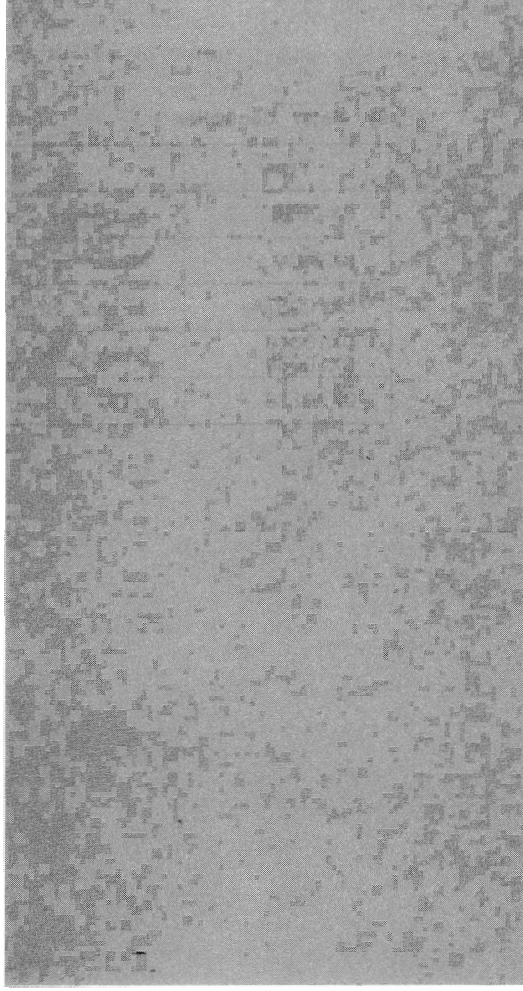


Crosstalk between channels

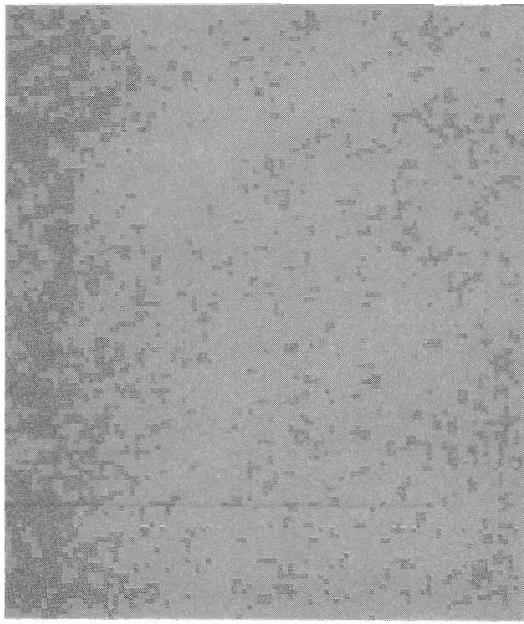


Recording and play back crosstalk





Moter Controller



3) Moter Controller

Type	Function	Page
CX-065B	Frequency Servo Controller	171
CX-891	Motor Servo Control	177
CX10031A	2-Phase Brushless Moter Control	182
CX10040 CX10060	2-Phase DC Brushless Moter Control	191
CX20123	OTM Motor Servo Control	210

SONY CX-065B

Frequency Servo Controller

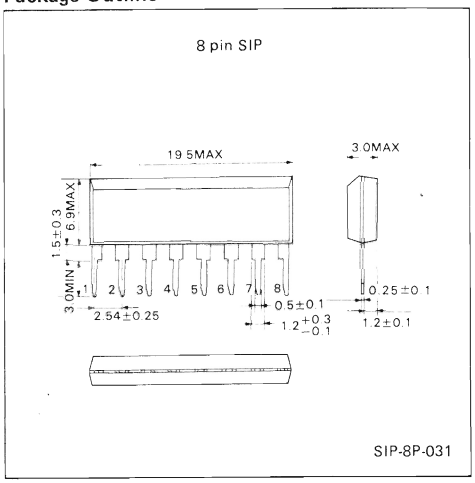
Description

The CX-065B is a frequency servo system motor control oriented monolithic integrated circuit that has been designed to suit for applications with a floppy disk drive, tape recorder, and turntable.

This integrated circuit has been configured of a waveform shaping circuit, sawtooth wave generating circuit, comparator, smoothing circuit, DC amplifier, and power supply.

Package Outline

Unit: mm



Features

- Less externally connected parts
- Resists power supply voltage fluctuations well.
- Exhibits good servo characteristics.

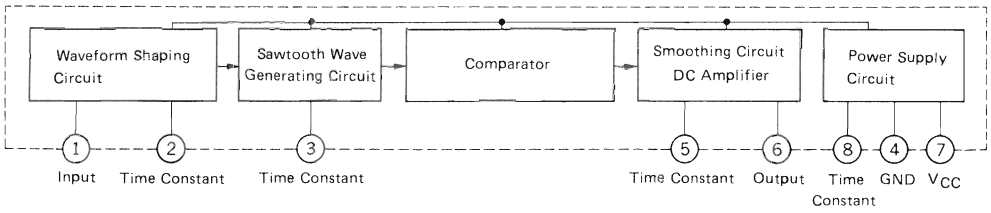
Structure

Bipolar Silicon Monolithic IC

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	17	V
• Input voltage	V_i	−2.0, 4	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−40 to +125	°C
• Allowable power dissipation	P_D	600	mW

Block Diagram

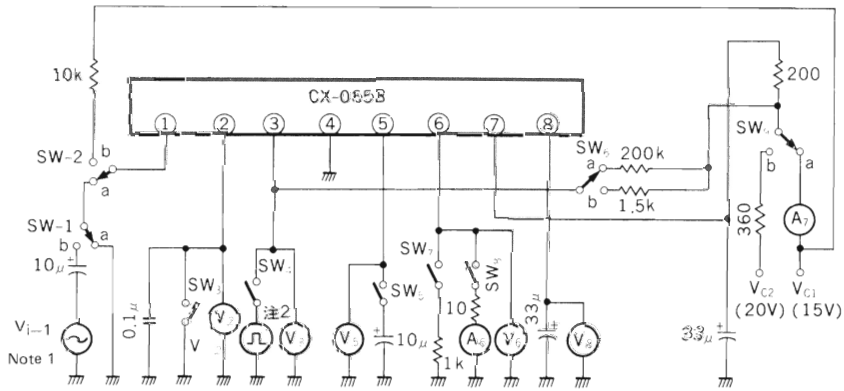


Electrical Characteristics

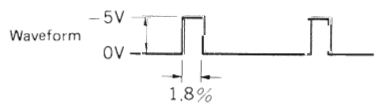
(Ta=25°C, See the Test Circuit and Conditions.)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Circuit Current	I_D	V_C=15V, 437Hz Input, Pulse Input	4.0	7.0	10.0	mA
Stabilized Voltage	V_8	V_C=15V, 437Hz Input, sin, 1Vp-p	4.55	4.80	5.00	V
Pin 5 Output Voltage	V_5	V_C=15V, No-signal Input	10.3	11.2	12.0	V
(N) Comparator Reference Voltage	V_{ref}	V_C=15V, No-signal Input	1.76	1.88	2.00	V
Pin 3 Voltage-1	V_{3-1}	V_C=15V, No-signal Input		40	70	mV
Pin 3 Voltage-2	V_{3-2}	V_C=15V, No-signal Input		1.0	5.0	mV
Gain Voltage-1	V_{g-1}	V_C=15V, Pulse input at 437Hz	2.5	2.8	3.1	V
Gain Voltage-2	V_{g-2}	V_C=20V, Pulse input at 437Hz	2.5	2.9	3.2	V
Saturation Voltage-1	V_{sat-1}	V_C=15V, No-signal Input		130	200	mV
Saturation Voltage-2	V_{sat-2}	V_C=15V, No-signal Input		140	200	mV
Output Pin Voltage	V_{out}	V_C=15V, Pulse input 437Hz	1.00	1.60	2.50	V
Maximum Output current	I_{out}	V_C=15V, Pulse input 437Hz	10	15	20	mA
Output Potential Difference	ΔV	$\Delta V=(V_{g-1})-(V_{out})$	1.00	1.30	1.60	V
Output Pulse Width	PW	V_C=15V, 437Hz Input, sin, 1Vp-p	100	150	200	μs

Electrical Characteristics Test Circuit

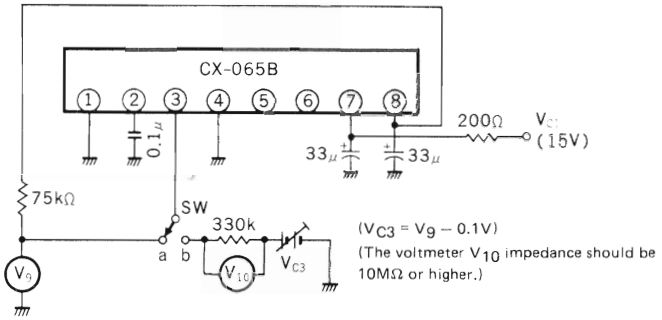


Note 1) V_{i-1} f=437Hz, Waveform: Sin, CW, Rg=600Ω, Output Level=1.0Vp-p (R_L=1.3kΩ)
2) V_{i-2} f=437Hz, Duty=1.8%, Polarity=(+), Rg_{OFF}=4.7k, Rg_{ON}=0Ω



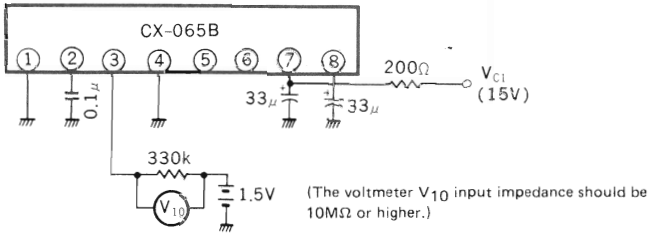
V3-1 Test Circuit

With reference to the circuit diagram below, measure voltage (V9) with SW(a), and after setting Vc3 to the reduced voltage of 100 mV, measure voltage (V10) by switching to SW(b), to make a GO/NG decision.

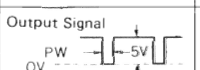


V3-2 Test Circuit

With reference to the circuit diagram below, measure voltage at (V10) to make a GO/NG decision.

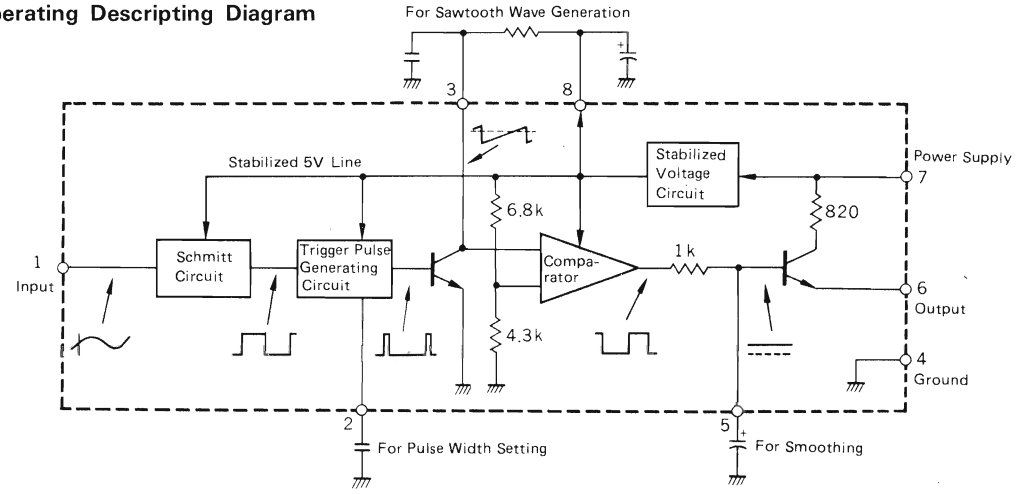


List of Test Conditions

Item	Symbol	SW Condition*									Input Signal(Note)	Test Condition	Test Point
		SW-1	SW-2	SW-3	SW-4	SW-5	SW-6	SW-7	SW-8	SW-9			
Circuit Current	I_D	a	a	OFF	ON	ON	a	OFF	OFF	a	V_{i-2}		A_7
Stabilized Voltage	V_8	b	a	OFF	OFF	OFF	a	OFF	OFF	a	V_{i-1}		V_8
Pin 5 Output Voltage	V_5	a	a	OFF	OFF	OFF	a	OFF	OFF	a	No signal		V_5
Comparator Reference Voltage	V_{ref}	a	a	OFF	OFF	OFF	a	OFF	OFF	a	No signal		V_3
Gain Voltage-1	V_{g-1}	a	a	OFF	ON	ON	a	OFF	OFF	a	V_{i-2}		V_5
Gain Voltage-2	V_{g-2}	a	a	OFF	ON	ON	a	OFF	OFF	b	V_{i-2}		V_5
Saturation Voltage-1	V_{sat-1}	b	b	ON	OFF	OFF	b	OFF	OFF	a	No Signal		V_3
Saturation Voltage-2	V_{sat-2}	a	a	OFF	OFF	OFF	a	OFF	OFF	a	No Signal		V_2
Output Pin Voltage	V_{out}	a	a	OFF	ON	ON	a	ON	OFF	a	V_{i-2}		V_6
Maximum Output current	I_{out}	a	a	OFF	ON	ON	a	OFF	ON	a	V_{i-2}		A_6
Output Potential Difference	ΔV											$V=V_{g1}-V_{out}$	
Output Pulse Width	PW	b	a	OFF	OFF	OFF	a	OFF	OFF	a	V_{i-1}	Output Signal 	V_5

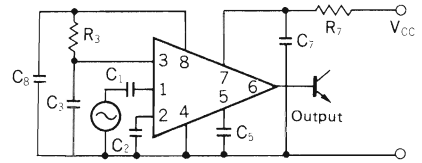
Note) * With regard to input signals V_{i-1} and V_{i-2}, refer to Notes 1 and 2 in the Test circuit.

Operating Descripting Diagram



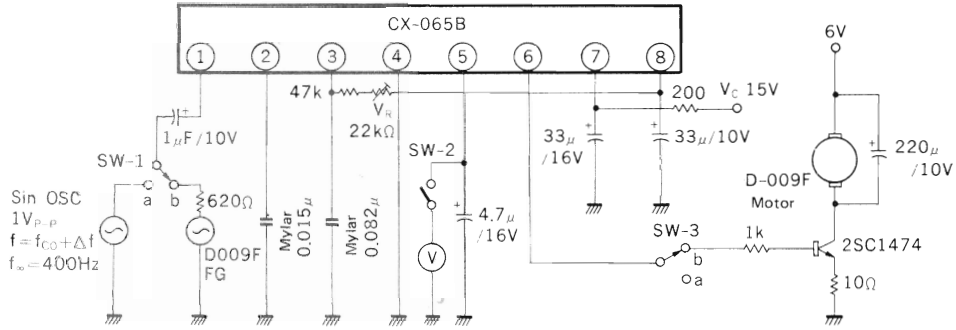
Notes on Application

Circuit



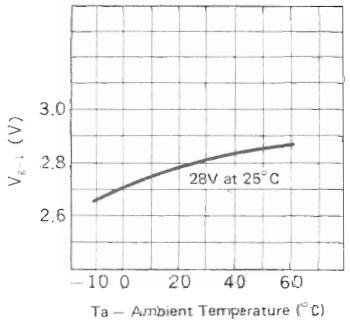
1. Although the input voltage range is from 1 Vp-p to 4.8 Vp-p, the capacitor C_1 may be omitted if the input is at 3 Vp-p or higher.
2. An appropriate output impedance of the tachogenerator is about 1 k Ω.
3. Set the sawtooth wave time constant determining R_3 at 10 kΩ≦R_3≧400 kΩ.
   The recommended sawtooth wave time constant determining R_3 range is 20 kΩ≦R_3≦200 kΩ.
4. Guidelines for selecting capacitor C_2 are $C_2=C_3/5$ with a minimum value at $C_2=C_3/10$.
5. C_8 serves parasitic oscillation preventive purposes for the power supply circuit. Under no circumstances should it be omitted.
6. When the power supply rise time is shorter than 100 ms, be sure to add R_7=200Ω on in series with the power supply for the IC protective purposes.
7. The power supply voltage applied at pin 7 may range from 6V to 17V, but when it is below 11V, the pin 8 voltage may fail to be stabilized.
8. Hold the steady output current level at pin 6 below 3 mA.
9. Hold the output current level at pin 8 within ±2 mA (where the negative value signifies an inflow). However, when not employing pin 6 , Current Range From −2 mA to +5mA is permissible.
10. C_5 should be determined in accordance with input (carrier) frequency f_o by taking transfer function H(s) and carrier ripple into consideration.
    Cut-off frequency f_c of the Frequency to Voltage (F-V) converter may be expressed as follows:
    $f_c=7.6/C_5(\mu F)$[Hz]

Application Circuit and F-V Characteristics Test Circuit

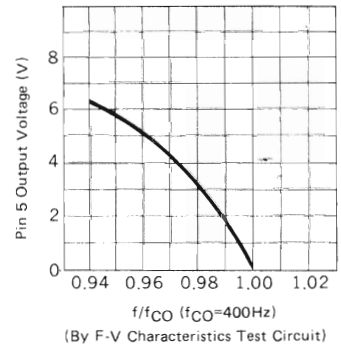


Note) ① With SW1-b, SW2-off, SW3-b: Typical Application Circuit
② With SW1-a, SW2-on, SW-a: F-V Characteristics Test Circuit, where after setting VR to provide 0V at Ⓥ against an f_{CO}=400Hz input, the frequency should be lowered and the Ⓥ measures taken.

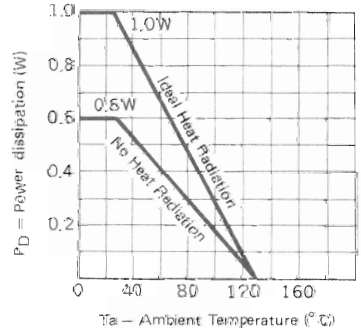
Gain Voltage-1 temperature characteristics



Frequency to Voltage characteristics



Allowable power dissipation derating curves



SONY CX-891

Motor Servo Control

Description

The CX-891 is a bipolar IC designed as a servo amplifier for motors in tape recorders. It consists of waveform shaping, sawtooth wave generator, comparator, smoothing, and DC amplification circuits.

Features

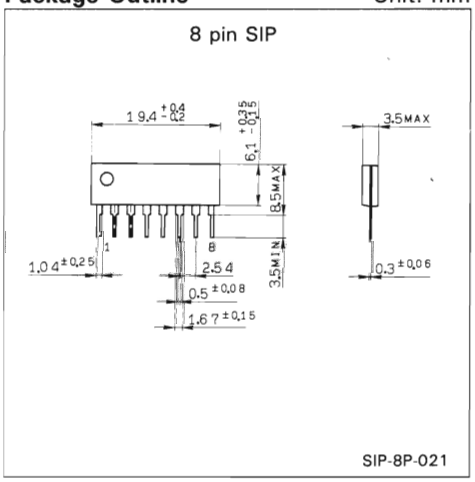
- Operates from a wide range of supply voltages (1.8 V to 14.4 V).
- Low current consumption
- Needs few peripheral parts to form a frequency amplifier.

Structure

Bipolar silicon monolithic IC

Package Outline

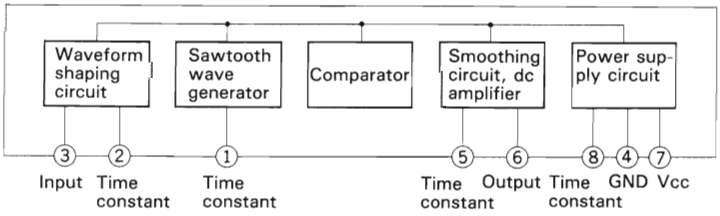
Unit: mm



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	15	V
• Input voltage (Pin 3)	VI	±10	V
• Input current (Pin 3)	II	−5	mA
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	600	mW

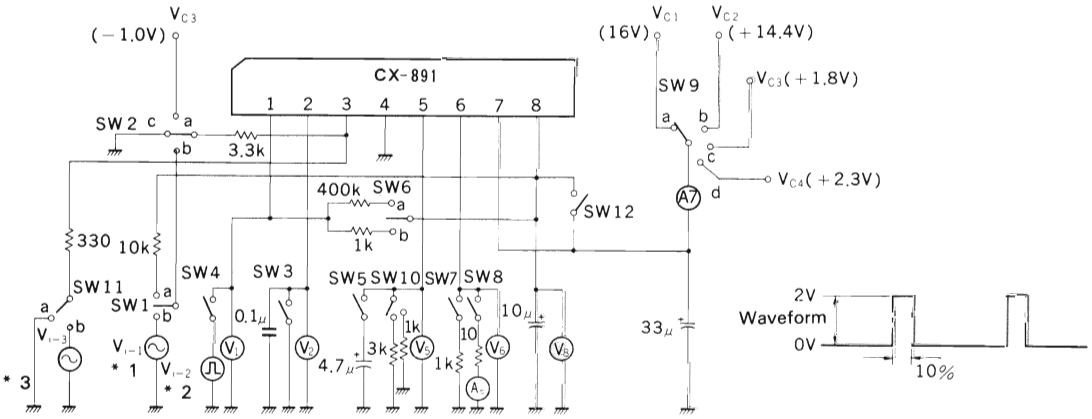
Block Diagram



Electrical Characteristics (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Circuit current	I_D	Vc = 6V, Input 400Hz, Pulse input	1.5	3.0	4.7	mA
Stabilized voltage	V_8	Vc = 6V, Input 400Hz, sine wave input	1.85	2.17	2.58	V
Comparator reference voltage	V_{ref}	Vc = 6V, No signal input	0.90	1.08	1.28	V
Gain voltage (1)	V_{g-1}	Vc = 6V, Input 400Hz, Pulse input	1.21	1.45	1.76	V
Gain voltage (2)	V_{g-2}	Vc = 14.4V, Input 400Hz, Pulse input	1.21	1.47	1.81	V
Saturation voltage (1)	V_{sat-1}	Vc = 6V, No signal input		55	110	mV
Saturation voltage (2)	V_{sat-2}	Vc = 6V, No signal input		75	132	mV
Maximum output current (2)	I_{out}	Vc = 6V, No signal input	9	15	24	mA
Output pulse width (1)	P.W-1	Vc = 6V, Input 400Hz, sine wave input	250	380	520	μs
Output voltage (1)	V_{out-1}	Vc = 6V, f = 400Hz, Pulse input	0.18	0.26	0.35	V
Voltage at Pin 1	V_1	Vc = 6V, No signal input			220	mV
Voltage at Pin 5	V_5	Vc = 15V, No signal input			110	mV
Leakage current at Pin 6	I_L	Vc = 17V, No signal input			11	μA
Voltage at Pin 2 (1)	V_{2-1}	Pin 7 and 8 interconnected, Vc = 1.8V, No signal input			220	mV
Voltage at Pin 2 (2)	V_{2-2}	Pin 7 and 8 interconnected, Vc = 2.3V, No signal input			220	mV
Output pulse width (2)	P.W-2	Pin 7 and 8 interconnected, f = 400Hz, sine wave input	270	450	671	μs
Output voltage (2)	V_{out-2}	Pin 7 and 8 interconnected, Vc = 1.8V, No signal input	0.4	0.8	1.2	V
Saturation voltage (3)	V_{sat-3}	Pin 7 and 8 interconnected, Vc = 2.3V, No signal input			132	mV

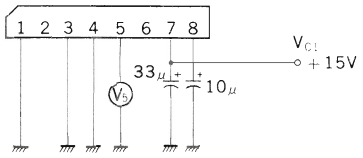
Electrical Characteristics Test Circuit



Note) * 1: V_{i-1} f = 400 Hz, sine wave, R_g = 600 Ω, output level = 1.0 V_{p-p} (R_L = 0.8 kΩ)
* 2: V_{i-2} f = 400 Hz, Du = 10%, polarity (+), $R_{g(OFF)}$ 4.7 kΩ, $R_{g(ON)}$ = 0 Ω
* 3: V_{i-3} f = 400 Hz, sine wave, R_g = 600 Ω, output level = 0.18 V_{p-p} (R_L = 0.8 kΩ)

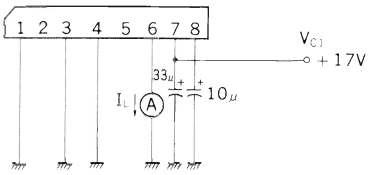
V5 Test Circuit

The voltage is measured with voltmeter (V5) as shown below.



IL Test Circuit

The current is measured with amperemeter (A) connected to Pin 6 as shown below.

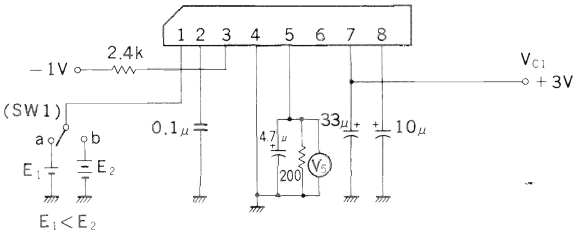


Vref Test Circuit

The voltage is measured with voltmeter (V5) as shown below.

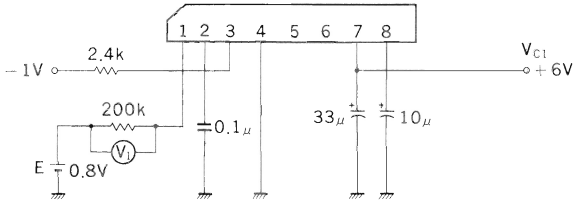
SW position	Test point	Min.	Max.	Unit
a	V5		0.1	V
b	V5	0.1		V

E1 : 0.9 V
E2 : 1.28 V



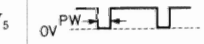
V1 Test Circuit

The voltage is measured with voltmeter V1 as shown below.

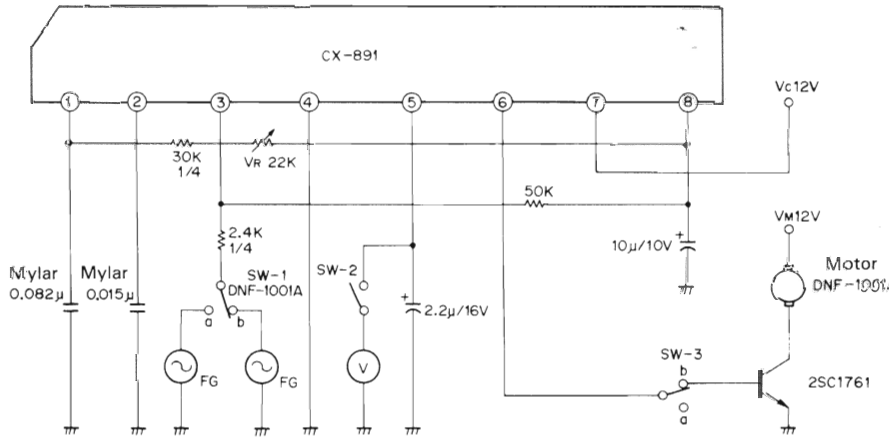


(The input impedance of voltmeter V1 must be 10 MΩ or above.)

Test Circuit

Item	Symbol	Switch Position												Input Signal (Note)	Test Point	Test Condition
		SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12			
Circuit current	I_D	–	a	OFF	ON	ON	a	OFF	OFF	a	OFF	OFF	OFF	ⓐV_{i-2} ⓐ−1V	A_7	
Stabilized voltage	V_8	b	b	↓	OFF	OFF	↓	↓	↓	↓	↓	↓	↓	ⓐV_{i-1}	V_8	
Gain voltage -1	V_{g-1}	–	a	↓	ON	ON	↓	↓	↓	↓	↓	↓	↓	ⓐV_{i-2} ⓐ−1V	V_5	
Gain voltage -2	V_{g-2}	–	↓	↓	↓	↓	↓	↓	↓	b	↓	↓	↓	ⓐV_{i-2} ⓐ−1V	V_5	
Saturation voltage -1	V_{sat-1}	a	b	ON	OFF	OFF	b	↓	↓	a	↓	↓	↓	ⓐ No signal	V_1	
Saturation voltage -2	V_{sat-2}	–	a	OFF	↓	↓	a	↓	↓	↓	↓	↓	↓	ⓐ−1V	V_2	
Ouptut pulse width (1)	P.W-1	b	b	↓	↓	↓	↓	↓	↓	↓	3k	↓	↓	ⓐV_{i-1}	V_5	
Maximum output current	I_{out}	–	a	↓	↓	↓	↓	↓	ON	↓	OFF	↓	↓	ⓐ No siganl	A_6	
Output voltage (1)	V_{out}	–	↓	↓	ON	ON	↓	ON	OFF	↓	↓	↓	↓	ⓐV_{i-2} ⓐ−1V	V_6	
Voltage at Pin 2 (1)	V_{2-1}	–	OFF	OFF	OFF	OFF	a	OFF	OFF	c	OFF	a	ON	ⓐ No signal	V_2	
Voltage at Pin 2 (2)	V_{2-2}	–	OFF	OFF	OFF	OFF	a	OFF	OFF	d	OFF	a	ON	ⓐ No signal	V_2	
Output pulse width (2)	P.W-2	–	↓	↓	↓	↓	↓	↓	↓	↓	1k	b	↓	V_{i-3}	V_5	
Output voltage (2)	V_{out-2}	a	b	↓	↓	↓	↓	↓	↓	↓	↓	OFF	↓	No signal	V_5	
Saturation voltage (2)	V_{sat-3}	↓	↓	ON	↓	↓	↓	↓	↓	↓	OFF	↓	↓	No siganl	V_1	

Application Circuit and F-V Characteristics Test Circuit

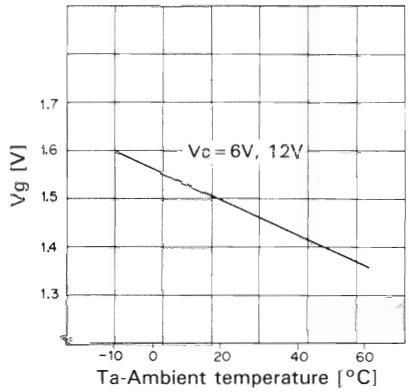


Sine wave oscillator
1Vp-p
$f = f_{CO} + \triangle f$
$f_{CO} = 450Hz$

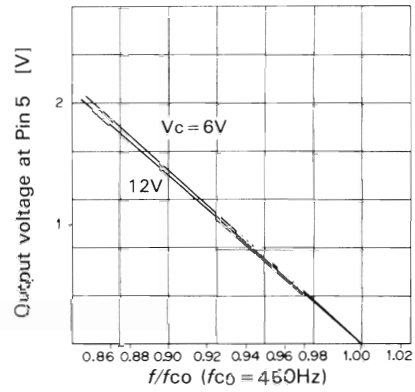
Note) 1. An application circuit is formed by setting SW1 to (b), SW2 to off, and SW3 to (b).

2. The F-V characteristics test circuit is formed by setting SW1 to (a), Sw2 to on, and SW3 to (a). Input is applied so that the voltage at Pin 5 is zero with Fco = 450 Hz by controlling VR. The voltage is then recorded for each frequency reduced from the above.

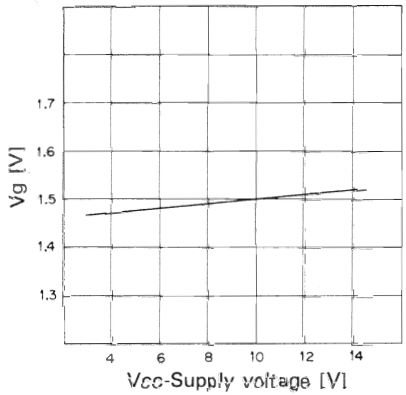
Temperature characteristics of voltage gain



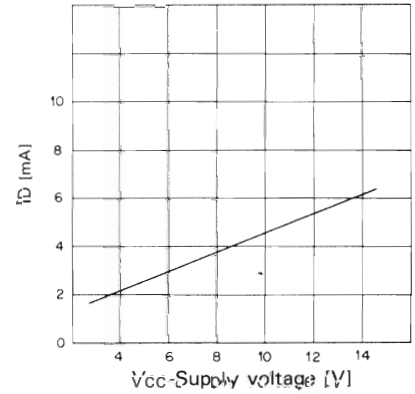
Voltage vs. Frequency characteristics



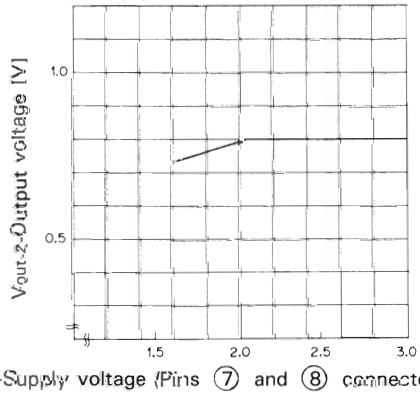
Voltage gain vs. Voltage characteristics



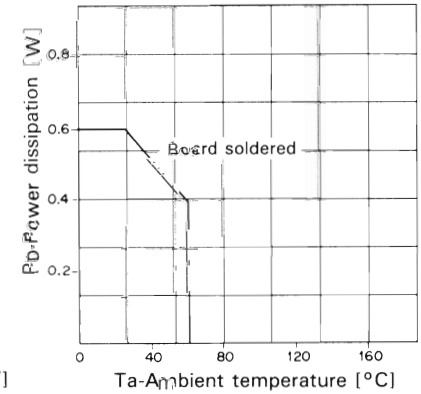
Circuit current vs. Voltage characteristics



Output voltage (2) vs. Supply voltage characteristics



Maximum power dissipation decreasing curve



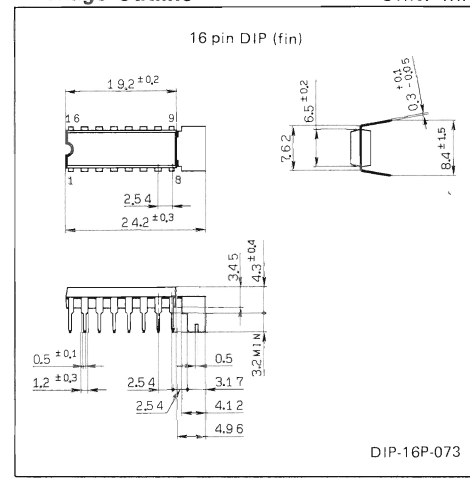
2-Phase Brushless Motor Control

Description

The CX10031A is two-phase linear brushless motor control IC designed for cassette tape deck. The CX10031A is made compact with reduced cost by having servo system and driver system incorporated in a single chip.

Package Outline

Unit: mm



Features

- Split power supply
- Low distortion factor (0.2%)
- Maximum output current (300 mA)
- Hall device for detecting magnetic position
- Normal/Reverse rotation switch
- 16 pin Dual-In-Line Package with copper radiation fin

Structure

Bipolar Silicon Monolithic IC

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage (quiescent)	V_{CC1}	±15	V
• Supply voltage (operation)	V_{CC2}	±12	V
• Circuit current	I_{CC}	0.5	A
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−40 to +150	°C
• Allowable power dissipation	P_D	2*	W

*Ta=40°C

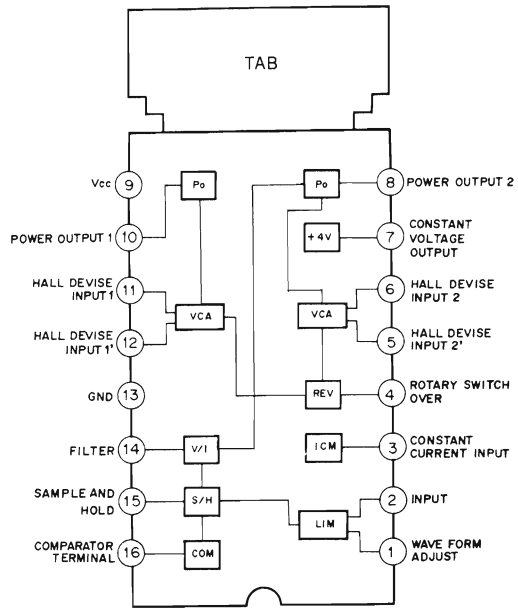
Recommended Operating Condition (Ta=25°C)

Supply voltage	V_{CC}	±9 to ±12	V

Pin Description

No.	Description	No.	Description
1	Waveform adjustment	9	Power supply pin (positive)
2	Input	10	Power output 1
3	Constant current input	11	Hall device input1
4	Rotary switch	12	Hall device input1
5	Hall device input 2	13	GND
6	Hall device input 2	14	Filter
7	Constant voltage output	15	Sample and hold
8	Power output 2	16	Comparator
TAB	Power supply pin (negative)		

Block Diagram and Pin Configuration (Top View)



Electrical Characteristics

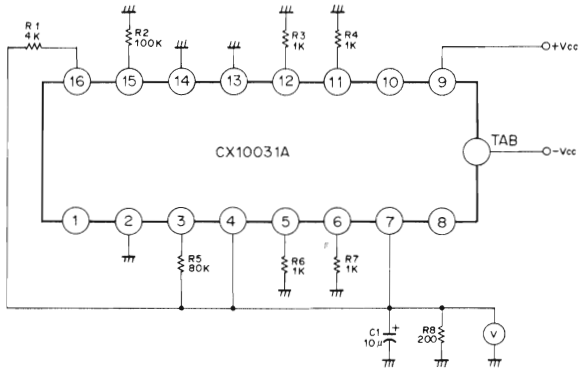
(Vcc=±11V, f=400 Hz Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test circuit
Output voltage	Vo	3.6	4.0	4.4	V	No. 1
Circuit current	Icc		±20	±30	mA	No. 2
FG threshold input voltage	Vth		0.14	0.5	V	No. 3
Constant current output	Ig	38	46	54	μA	No. 4
Maximum hold voltage	Vh (Max.)	2.8	3.2	3.7	V	No. 5
Voltage gain (power amp)	GPO	39	42	45	dB	No. 7
Channel balance (power amp)	ΔGPO		0	±1.5	dB	No. 7
Off-set voltage (power amp)	Vio	−0.7	0.3	1.3	V	No. 6
Distortion factor (power amp)	THD		0.2	1.5	%	No. 7
Maximum output voltage	Vom	±7.2	+8.7 −8.5		V	No. 8
Saturation voltage	Vsat		90	200	mV	No. 9
Reference voltage	Vref		0	±5	%	No. 10

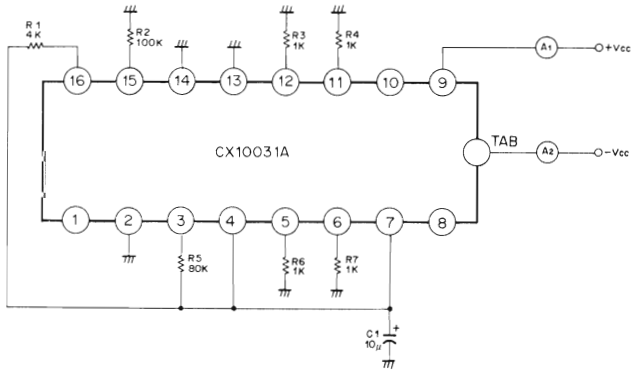
Electrical Characteristics Test Circuit

1. Vo=V

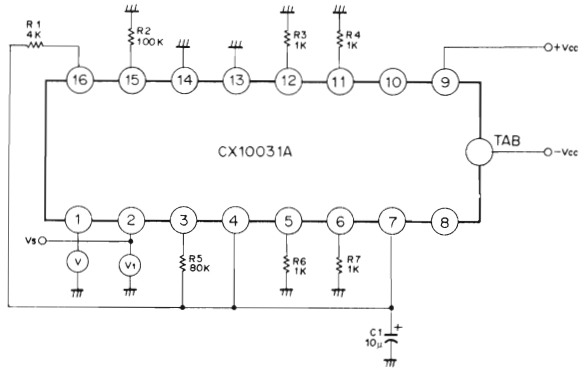
Unit R : OHM
C : F



2. Icc=A1, −Icc=A2

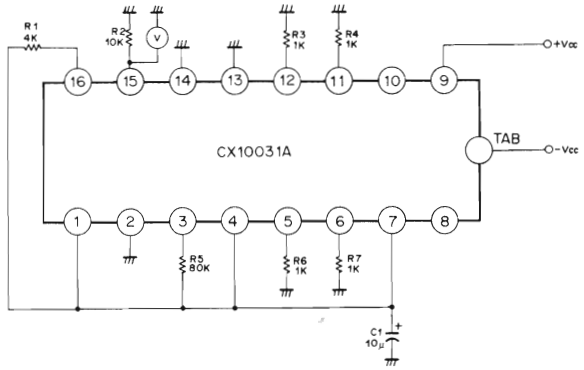


3. Vth=V1

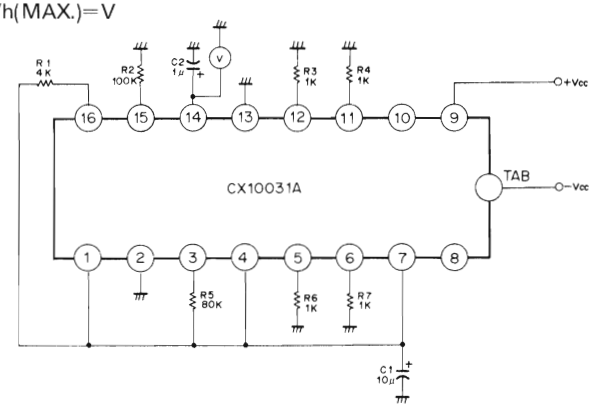


V_S changes from low to high and from high to low
V_1=V_S when V changes from low to high and from high to low

4. Ig=V/R2

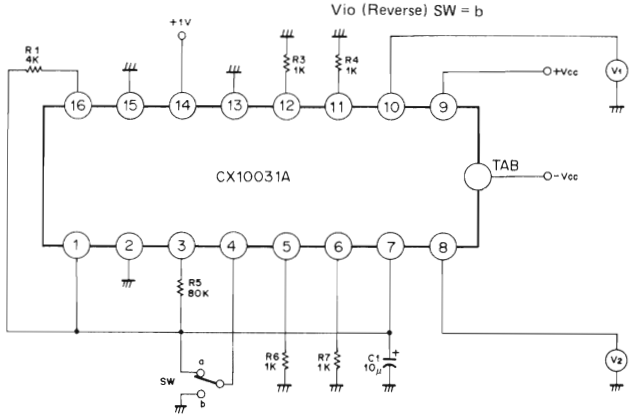


5. Vh(MAX.)=V

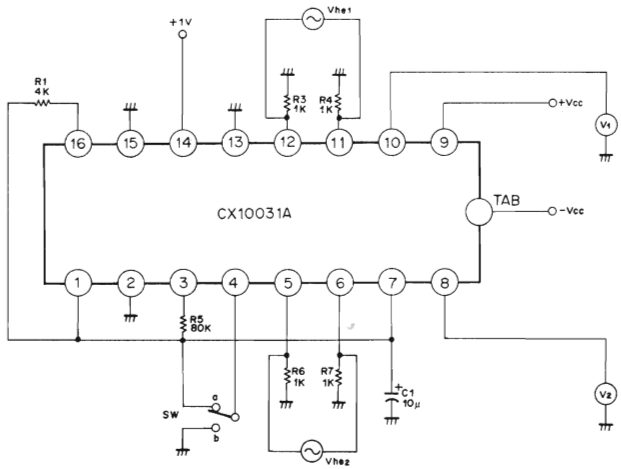


6. Vio=V1−V2

Vio (Nomal) SW = a
Vio (Reverse) SW = b



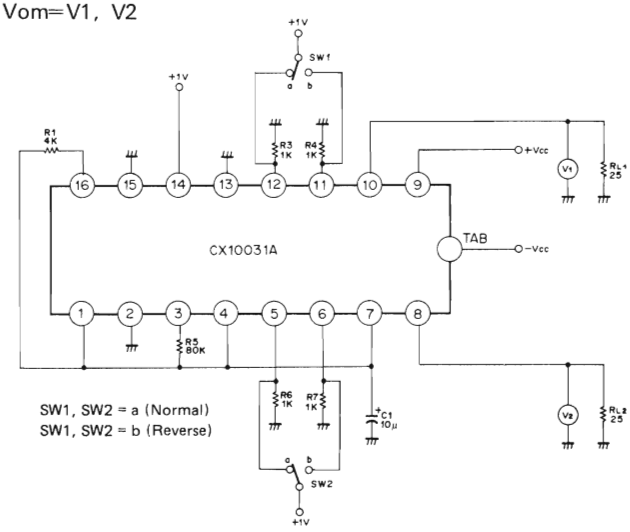
7. GPO, ΔGPO, THD



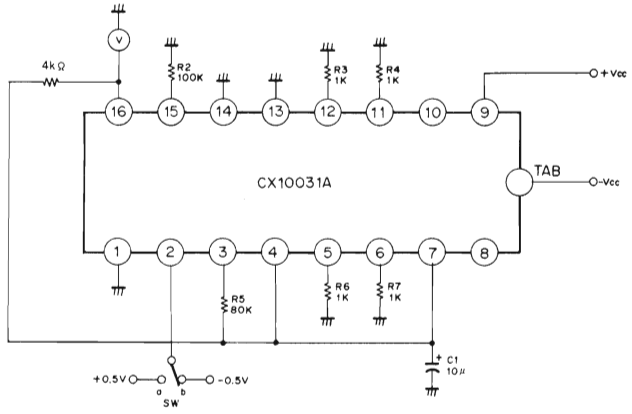
SW : a Gpo1 (Nomal) = $20\log\frac{V1}{Vhe1}$, Gpo2 (Nomal) = $20\log\frac{V2}{Vhe2}$

SW : b Gpo1 (Reverse) = $20\log\frac{V1}{Vhe1}$, Gpo2 (Reverse) = $20\log\frac{V2}{Vhe2}$

8. Vom=V1, V2

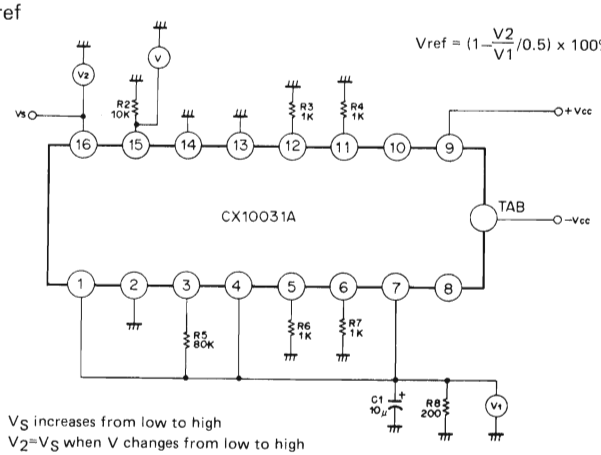


9. Vsat=V at SW=b



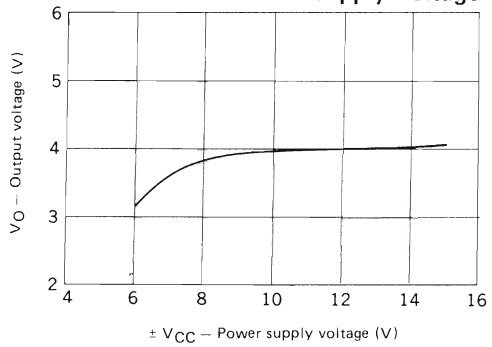
10. Vref

$$Vref = (1-\frac{V2}{V1}/0.5) \times 100\%$$

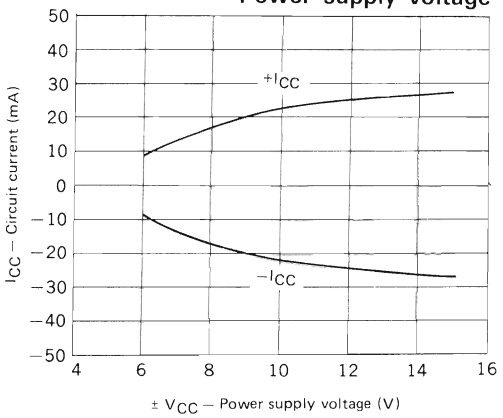


V_S increases from low to high
V_2=V_S when V changes from low to high

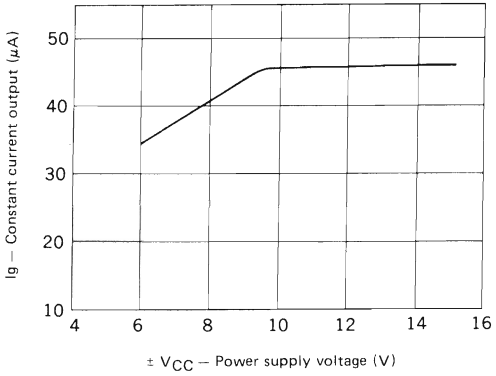
Output voltage vs. Power supply voltage



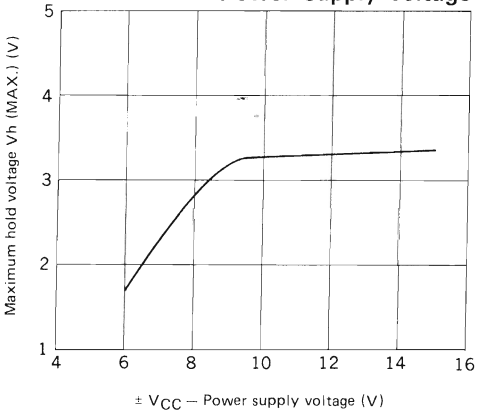
Circuit current vs. Power supply voltage



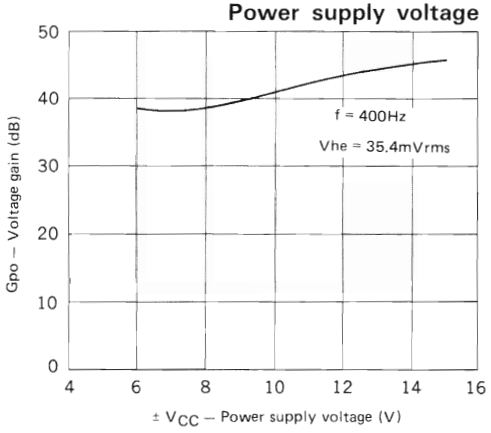
Constant current output vs. Power supply voltage



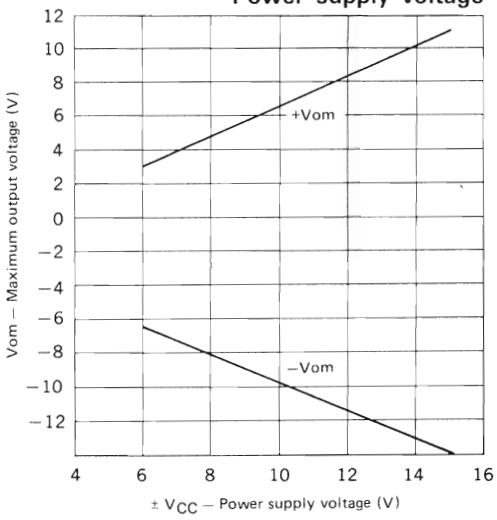
Maximum hold voltage vs. Power supply voltage



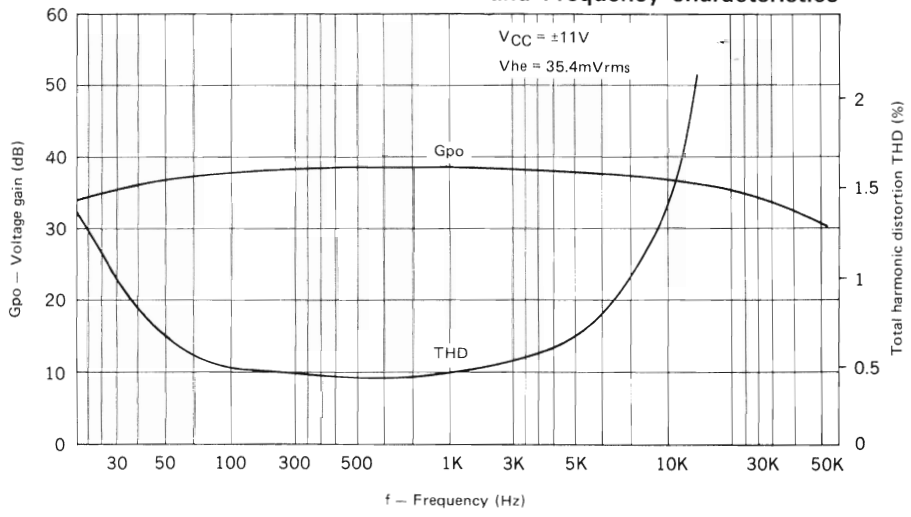
Voltage gain vs. Power supply voltage



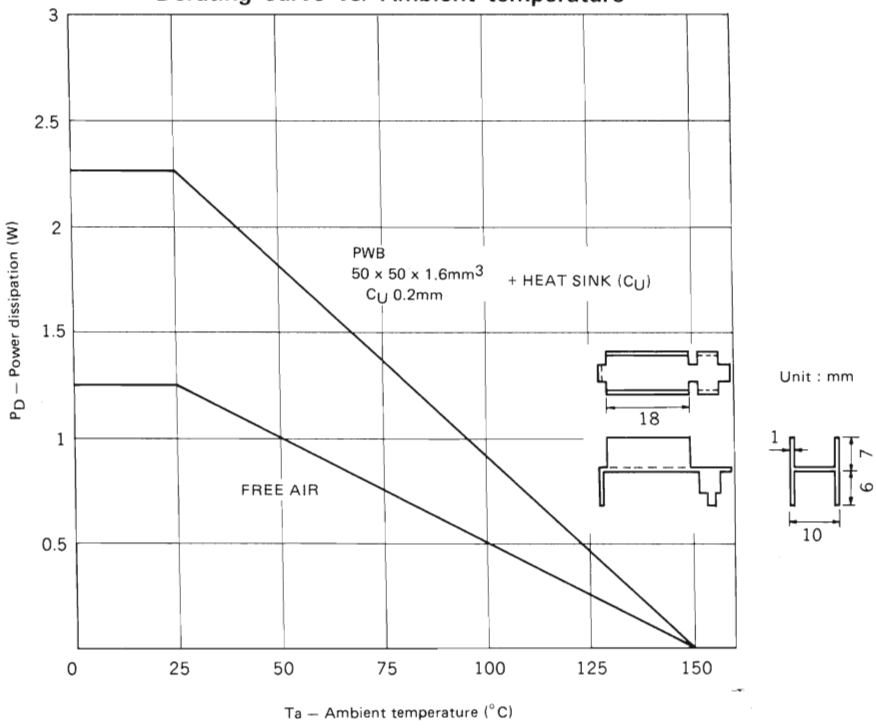
Maximum output voltage vs. Power supply voltage



Voltage gain, Total harmonic distortion and Frequency characteristics



Derating curve vs. Ambient temperature



2-Phase DC Brushless Motor Control

Description

The CX10040/CX10060 are ICs which have been developed for 2-phase DC brushless motor control. The controlling system and driving system are put into 1 chip. For phase detection, utilizing hall device, FG amplifier, F/V converter, and sample and hold circuits are incorporated within 1 chip which composes the motor driving system of F servo.

Features

- Controlling system and driving system are put into 1 chip
- 2-phase motor full wave driving
- Large output current (1.2A/phase)
- Built-in FG amplifier, F/V converter, and sample and hold circuit
- Gain adjustment of the controlling amplifier of the final stage of servo system is possible
- Built-in reference voltage source
- Built-in output current limiter circuit
- Normal rotation and inverse rotation control pin is attached
- Start and stop control pin is attached

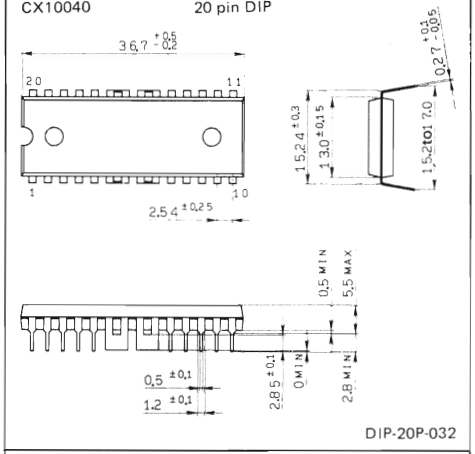
Structure

Bipolar silicon monolithic IC

Package Outline

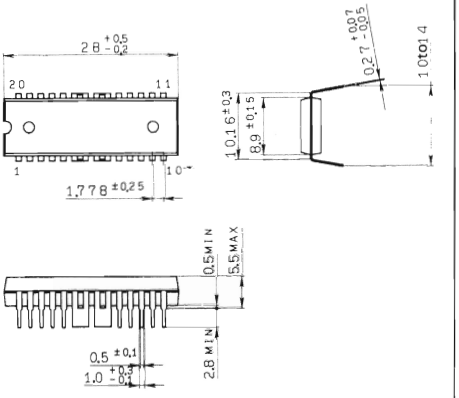
Unit: mm

CX10040 20 pin DIP



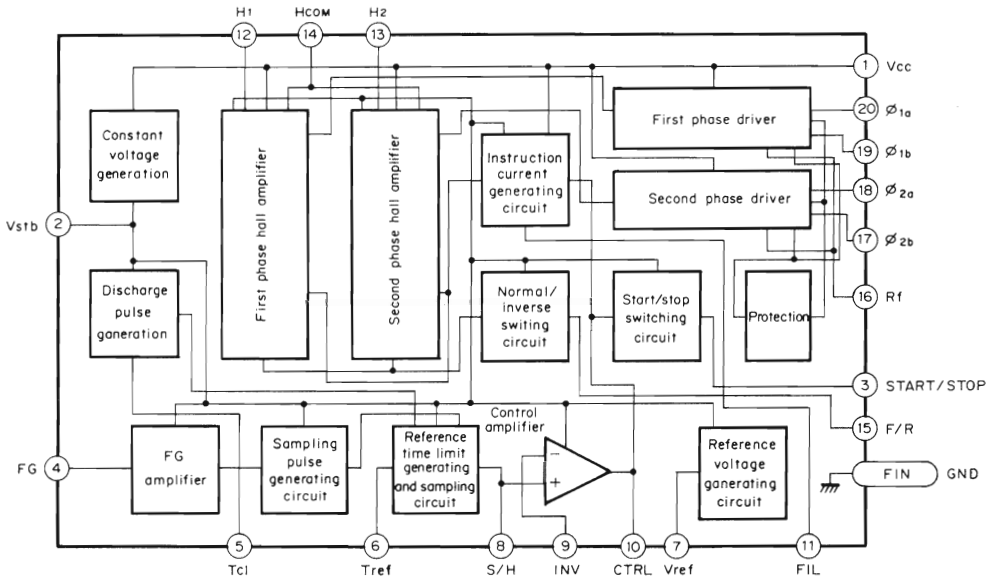
DIP-20P-032

CX10060 20 pin SRK

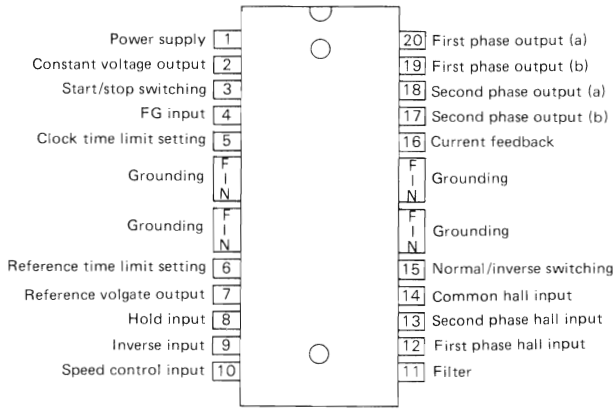


SRK-20P-031

Block Diagram



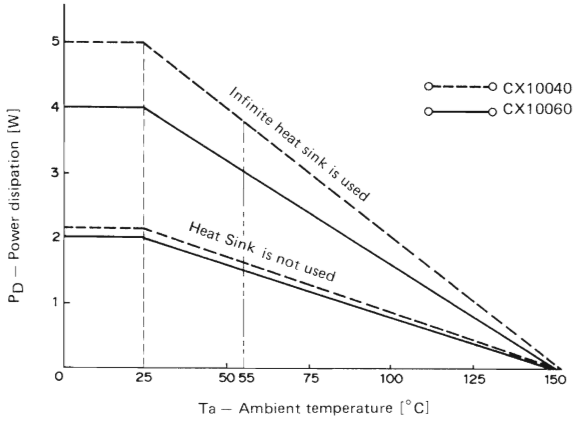
Pin Configuration (Top View)



Absolute Maximum Ratings (Ta=25°C unless otherwise specified)

No.	Item	Symbol	Rated value	Unit	Remark
1	Supply voltage	V_{CC}	18	V	
2	Rush current	I_{LMax}	1.2	A/phase	
3	Output current	I_L	0.4	A/phase	
4	Applied voltage between 12 — 14 and 13 — 14	V_H	5	Vp-p	
5	Input voltage of pin 4	V_4	−0.2 to Vstb	V	
6	Applied voltage to pin 3	V_3	−0.2 to Vstb	V	
7	Applied voltage to pin 15	V_{15}	−0.2 to Vstb	V	
8	Output current of pin 2	Istb	20	mA	
9	Inflowing current of pin 5	$I_{OL}5$	10	mA	When time constant capacitor discharge has been completed
10	Inflowing current of pin 6	$I_{OL}6$	10	mA	When time constant capacitor discharge has been completed
11	Output current of pin 7	Iref	1	mA	Both inflowing and outflowing currents
12	Applied voltage to pin 8	V_8	−0.2 to Vstb	V	
13	Applied voltage to pin 9	V_9	−0.2 to Vstb		
14	Applied voltage betwewn pins 8 and 9	V_{8-9}	±0.7	V	
15	Inflowing current of pin 10	$I_{OL}10$	5	mA	
16	Hall input inphase voltage	$V_{H(C)}$	1 to Vstb −1	V	Pins between 12 and 14, and 13 and 14
17	Operating voltage range	V_{OP}	7.2 to 18	V	Voltage of pin 1
18	Internal power consumption	Pd_F	4 (CX10060) 5 (CX10040)	W	Use infinite radiation plate
19	Junction temperature	Tj	150	°C	
20	Heat diminishing rate	K_θ	(32)	mW/°C	Use infinite radiation plate
21	Operating ambient temperature	Topr	0 to 55	°C	
22	Storage temperature	Tstg	−40 to +125	°C	

Power Disipation Derating Curve



Electrical Characteristics (V_{CC}=12V, Ta=25°C unless otherwise specified)

No.	Item	Symbol	Standard value	Min.	Typ.	Max.	Unit
1	Circuit current (1)	$I_{CC}(1)$		1.9	3.3	5.0	mA
2	Circuit current (2)	$I_{CC}(2)$	V_{CC}=18V	2.1	3.7	6.1	mA
3	Constant-voltage output voltage (1)	Vstb(1)		5.2	5.6	6.0	V
4	Constant-voltage output voltage (2)	Vstb(2)	270Ω between Vstb and GND	5.0	5.6	6.0	V
5	Reference-voltage output voltage	Vref	V_{CC}=Vstb=5.6V	2.70	2.81	2.94	V
6	Low level of pin 5	$V_{OL}5$	V_{CC}=Vstb=5.6V 10 kΩ between Vstb and pin 5	—	80	120	mV
7	Low level of pin 6	$V_{OL}6$	V_{CC}=Vstb=5.6V 10 kΩ between Vstb and pin 6	—	30	70	mV
8	Clock threshold value voltage (1)	$V_{TH}(1)$	V_{CC}=Vstb=5.6V	1.78	1.90	2.00	V
9	Clock threshold value voltage (2)	$V_{TH}(2)$	V_{CC}=Vstb=5.6V	2.67	2.81	2.95	V
10	Clock threshold value voltage (3)	$V_{TH}(3)$	V_{CC}=Vstb=5.6V	3.01	3.17	3.33	V
11	Clock threshold value voltage (4)	$V_{TH}(4)$	V_{CC}=Vstb=5.6V	3.95	4.17	4.37	V
12	Low level of pin 10	$V_{OL}10$	V_{CC}=Vstb=5.6V 5.1 kΩ between Vstb and pin 10	—	0.75	1.00	V
13	Stop circuit operating voltage	V_{STOP}	V_{CC}=Vstb=5.6V Monitor with pin 10	—	—	2	V
14	Input offset voltage of pin 4	Voffset 4	V_{CC}=Vstb=5.6V	—	0	±6	mV
15	Offset voltage between pins 6 and 8	Voffset 6-8	V_{CC}=Vstb=5.6V	—	0	±10	mV
16	Offset voltage between pins 8 and 9	Voffset 8-9	V_{CC}=Vstb=5.6V	—	0	±10	mV
17	Offset voltage between pins 12 and 14	Voffset 12-14		—	30	60	mV
18	Offset voltage between pins 13 and 14	Voffset 13-14		—	30	60	mV
19	Outflowing current of pin 11	Is11	V_{CC}=Vstb=5.6V	1.20	1.64	2.24	mA
20	Inverse circuit operating voltage	V_{REV}	Monitor with pins 20 and 18	—	—	2	V
21	Maximum bias current of a output	$I_{Ba(Max)}$	Measured at pin 16	9	13	—	mA

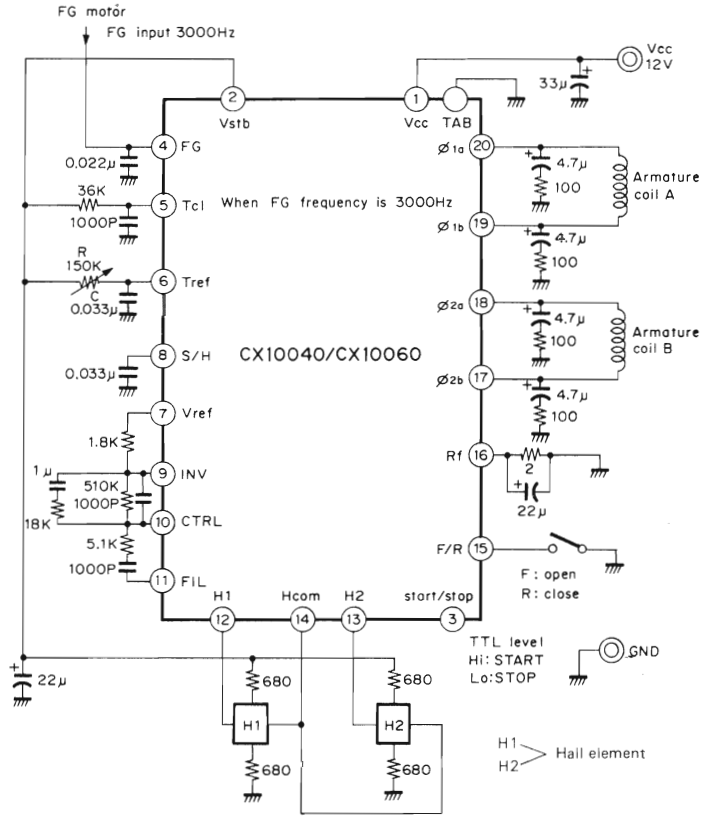
No.	Item	Symbol	Standard value	Min.	Typ.	Max.	Unit
22	Maximum bias current of b output	$I_{Bb(Max)}$	Measured at pin 16	9	13	—	mA
23	Maximum bias current ratio	$KI_{B(Max)}$	Calculated from $\frac{I_{Ba(Max)}}{I_{Bb(Max)}}$	0.9	1	1.1	A/A
24	Output saturation voltage (upper side)	Vsat(U)	Applicable to pins 17 to 20 I_O=0.4A I_O=0.8A	—	 1.0 1.5	 1.5 2.2	V
25	Output saturation voltage (lower side)	Vsat(D)	Applicable to pins 17 to 20 I_O=0.4A I_O=0.8A	—	 0.5 1.0	 0.75 1.5	V
26	Limiter current	Ilim	Rf=2Ω Measured with voltage conversion	1.6	2.0	2.4	V
27	Individual pin leakage currents	I_{LO}	Applying voltage of 1V between individual pins and GND	—	—	0.1	μA
28	Discharge pulse timing	T_{DP}	The time length from the leading edge of the rectangular wave of pin 5 to that of pin 6	70	—	—	μs
29	Output function	F_{OUT}	See attached table Hi	8.5	—	—	V
			See attached table Lo	—	—	2.5	V
30	Output current ratio (V_{CC} to pin, pin to GND)	KI_O	See KI_O test circuit	0.85	1.00	1.15	A/A
31	Output current 1 between pins	$I_{OUT}1$	Measure at pins 17 to 20	6	10	14	mA
32	Output current 2 between pins	$I_{OUT}2$	Measure at pins 17 to 20	13	20	27	mA
33	Output current ratio between pins	KI_{OUT}	See KI_{OUT} test circuit	0.8	1.0	1.2	A/A
34	Output saturation voltage between pins (Upper side)	Vosat(u)	Measure at pins 17 to 20	1.8	—	—	V
35	Output saturation voltage between pins (Lower side)	Vosat(d)	Measure at pins 17 to 20	1.1	—	—	V
36	Output bias current 1	I_{B1}	See Fig. 3 to 7	1.5	2.5	3.5	mA
37	Output bias current 2	I_{B2}	See test circuits of I_{B1}, I_{B2} and K_IB	9.5	13.0	16.5	mA
38	Output bias current ratio	K_IB	See test circuits of I_{B1}, I_{B2} and K_IB	0.8	1.0	1.2	A/A
39	Output current between pins (Inverse)	I_{ROUT}	Measure at pins 17 to 20	−13	−20	−27	mA

No.	Item	Symbol	Standard value	Min.	Typ.	Max.	Unit
40	Output current ratio between pins (Inverse)	KI_{ROUT}	See KI_{ROUT} measuring circuit	0.8	1.0	1.2	A/A
41	High voltage 1 of pin 10	$V_{OH}10\text{-}1$	V_{CC}=Vstb=5.8V	4	5	—	V
42	High voltage 2 of pin 10	$V_{OH}10\text{-}2$	V_{CC}=Vstb=7V	5.2	6	—	V
43	Low voltage 1 of pin 10	$V_{OL}10\text{-}1$	V_{CC}=Vstb=5.8V	—	0.75	1.00	V
44	Low voltage 2 of pin 10	$V_{OL}10\text{-}2$	V_{CC}=Vstb=7V	—	0.75	1.00	V
45	Individual phases and relative phase upper side saturation voltage difference	$\Delta V\phi$		−0.82	0	0.82	V
46	Offset voltage difference between pins 8 and 9	Voff	Measure the difference between V_{CC}=Vstb=7.2V and 5.6V	−2	0	+2	mV

Attached Table Output Function

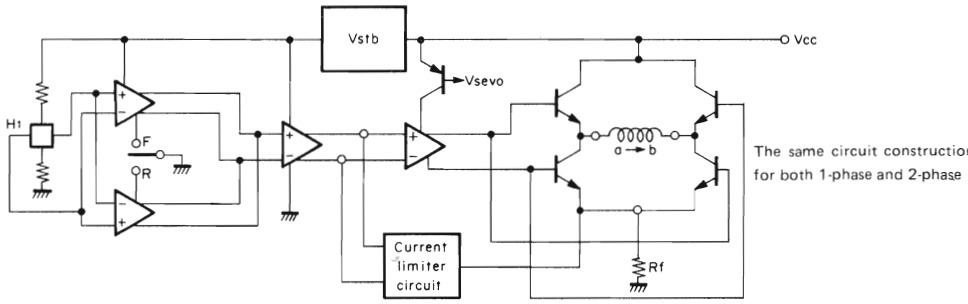
Item	Symbol	Pin17	Pin18	Pin19	Pin20
Output function (1)	$F_{OUT}(1)$	Lo	Hi	Lo	Hi
Output function (2)	$F_{OUT}(2)$	Hi	Lo	Lo	Hi
Output function (3)	$F_{OUT}(3)$	Lo	Hi	Lo	Hi
Output function (4)	$F_{OUT}(4)$	Hi	Lo	Hi	Lo
Output function (5)	$F_{OUT}(5)$	Lo	Hi	Hi	Lo
Output function (6)	$F_{OUT}(6)$	Hi	Lo	Hi	Lo

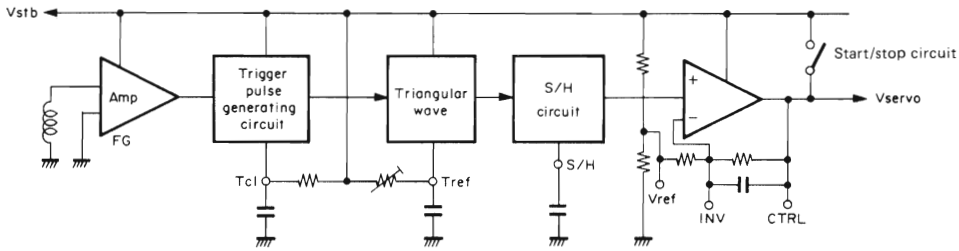
Application Circuit



※ Calculate with Tref of CR = $\frac{1}{\text{Fref-in } 0.5}$

Block Diagram





Test Condition

(See the Test Circuit)

Item	Symbol	State of switch																										Condition	Test point
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	
Circuit current (1)	$I_{CC}(1)$	b	c	a	c	d	d	a	e	b	a	a	a	a	a	a	a	a	a	a	b	off	off	a	a	a	a	e		A_1
Circuit current (2)	$I_{CC}(2)$	b	c	b	c	a	d	a	e	b	a	a	a	a	b	a	a	a	a	a	a	off	off	a	a	a	a	e		A_1
Constant voltage output voltage (1)	Vstb(1)	a	b	a	c	a	d	a	b	b	a	a	a	a	a	a	a	a	a	a	b	off	off	a	a	a	a	e		V_1
Constant voltage output voltage (2)	Vstb(2)	a	b	a	c	a	d	a	b	b	a	a	a	a	a	a	a	a	a	a	b	off	on	a	a	a	a	e		V_1
Reference voltage output voltage	Vref	a	a	a	c	a	d	b	b	b	a	a	a	a	a	a	a	a	a	a	c	off	off	a	a	a	a	e		V_4
Lower level of pin 5	V_{OL} 5	a	a	a	c	c	d	a	b	b	a	a	a	a	a	a	a	a	a	a	c	off	off	a	a	a	a	e		V_3
Lower level of pin 6	V_{OL} 6	a	a	a	d	d	b	a	b	b	a	a	a	a	a	a	a	a	a	a	c	off	off	a	a	a	a	e		V_3
Clock threshold value voltage (1)	$V_{TH}(1)$	a	a	a	d	b	c	a	c	b	a	a	a	a	a	a	a	a	a	a	c	on	off	a	a	a	a	e	Value of V_2 when V_3 becomes Lo from Hi	V_3, V_2
Clock threshold value voltage (2)	$V_{TH}(2)$	a	a	a	d	b	c	a	c	b	a	a	a	a	a	a	a	a	a	a	c	on	off	a	a	a	a	e	Value of V_2 when V_3 becomes Hi from Lo	V_3, V_2
Clock threshold value voltage (3)	$V_{TH}(3)$	a	a	a	d	b	b	a	b	b	a	a	a	a	a	a	a	a	a	a	c	on	off	a	a	a	a	e	Value of V_2 when V_3 becomes Lo from Hi	V_3, V_2
Clock threshold value voltage (4)	$V_{TH}(4)$	a	a	a	d	b	b	a	b	b	a	a	a	a	a	a	a	a	a	a	c	off	off	a	a	a	a	e	Value of V_2 when V_3 becomes Hi from Lo	V_3, V_2
Lower level of pin 10	V_{OL} 10	a	a	a	c	a	d	a	e	b	b	a	a	a	a	a	a	a	a	a	c	off	off	a	a	a	a	e		V_7
Stop circuit operating voltage	V_{STOP}	a	a	a	c	a	d	a	b	a	b	a	a	a	a	a	a	a	a	a	c	off	off	a	a	a	a	e	$V_7 \geqq 2V$	V_7
		a	a	b	c	a	d	a	b	a	b	a	a	a	a	a	a	a	a	a	c	off	off	a	a	a	a	e	$V_7 \geqq 1V$	
Input offset voltage of pin 4	Voffset 4	a	a	a	a	c	a	a	b	b	a	a	a	a	a	a	a	a	a	a	c	off	off	a	a	a	a	e	$V_3 \leqq 0.5V$	V_3
		a	a	a	b	c	a	a	b	b	a	a	a	a	a	a	a	a	a	a	c	off	off	a	a	a	a	e	$V_3 \geqq 4V$	
Offset voltage between pins 6 and 8	Voffset 6 — 8	a	a	a	d	e	d	c	a	b	a	a	a	a	a	a	a	a	a	a	c	off	off	a	a	a	a	e		V_5
Offset voltage between pins 8 and 9	Voffset 8 — 9	a	a	a	c	a	a	d	d	c	a	a	a	a	a	a	a	a	a	a	c	off	off	a	a	a	a	e	Measure V_{CC}=Vstb=5.6V and V_{CC}=Vstb=7.2V, respectively.	V_6
Offset voltage between pins 12 and 14	Voffset 12 — 14	a	c	a	c	a	d	a	b	a	d	b	c	c	a	a	b	b	b	b	b	off	off	a	a	a	a	e	Value of V_9 when V_{11} becomes Hi from Lo	V_9, V_{11}
Offset voltage between pins 13 and 14	Voffset 13 — 14	a	c	a	c	a	d	a	b	a	d	b	c	c	a	a	b	b	b	b	b	off	off	a	a	a	a	e	Value of V_9 when V_{10} becomes Hi from Lo	V_9, V_{10}
Outflowing current of pin 11	I_S 11	a	a	a	c	a	d	a	b	b	a	c	a	a	a	a	a	a	a	a	c	off	off	a	a	a	a	e		A_2
Inverse circuit operating voltage	V_{REV}	a	c	a	c	a	d	a	b	a	d	b	a	a	a	a	b	b	b	b	b	off	off	a	a	a	a	e	Both V_{10} and V_{11} are Hi	V_{10}, V_{11}
		a	c	a	c	a	d	a	b	a	d	b	a	a	b	a	b	b	b	b	b	off	off	a	a	a	a	e	Both V_{10} and V_{11} are Lo	
a maximum output bias current	$I_{Ba\ (MAX)}$	a	c	a	c	a	d	a	b	a	a	a	a	a	a	b	a	a	a	a	b	off	off	a	a	a	a	e		A_3
b maximum output bias current	$I_{Bb\ (MAX)}$	a	c	a	c	a	d	a	b	a	a	a	b	b	a	b	a	a	a	a	b	off	off	a	a	a	a	e		A_3
Pin 17 upper side output saturation voltage	Vsat(u) 17	a	c	a	c	a	d	a	b	a	a	a	b	b	a	a	c	c	c	c	b	off	off	a	a	a	a	a		V_{12}
Pin 17 lower side output saturation voltage	Vsat(d) 17	a	c	a	c	a	d	a	b	a	a	a	a	a	a	a	c	c	c	c	b	off	off	b	b	b	b	a		V_{12}

Item	Symbol	State of switch																												Test point
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S21	S22	S23	S24	S25	S26	S27	
Pin 18 upper side output saturation voltage	Vsat(u) 18	a	c	a	c	a	d	a	b	a	a	a	a	a	a	a	c	c	c	c	b	off	off	off	b	b	b	b	b	V_{12}
Pin 18 lower side output saturation voltage	Vsat(d) 18	a	c	a	c	a	d	a	b	a	a	a	b	b	a	a	c	c	c	c	b	off	off	off	a	a	a	a	b	V_{12}
Pin 19 upper side output saturation voltage	Vsat(u) 19	a	c	a	c	a	d	a	b	a	a	a	b	b	a	a	c	c	c	c	b	off	off	off	a	a	a	a	c	V_{12}
Pin 19 lower side output saturation voltage	Vsat(d) 19	a	c	a	c	a	d	a	b	a	a	a	a	a	a	a	c	c	c	c	b	off	off	off	b	b	b	b	c	V_{12}
Pin 20 upper side output saturation voltage	Vsat(u) 20	a	c	a	c	a	d	a	b	a	a	a	a	a	a	a	c	c	c	c	b	off	off	off	b	b	b	b	d	V_{12}
Pin 20 lower side output saturation voltage	Vsat(d) 20	a	c	a	c	a	d	a	b	a	a	a	b	b	a	a	c	c	c	c	b	off	off	off	a	a	a	a	d	V_{12}

Test Circuit

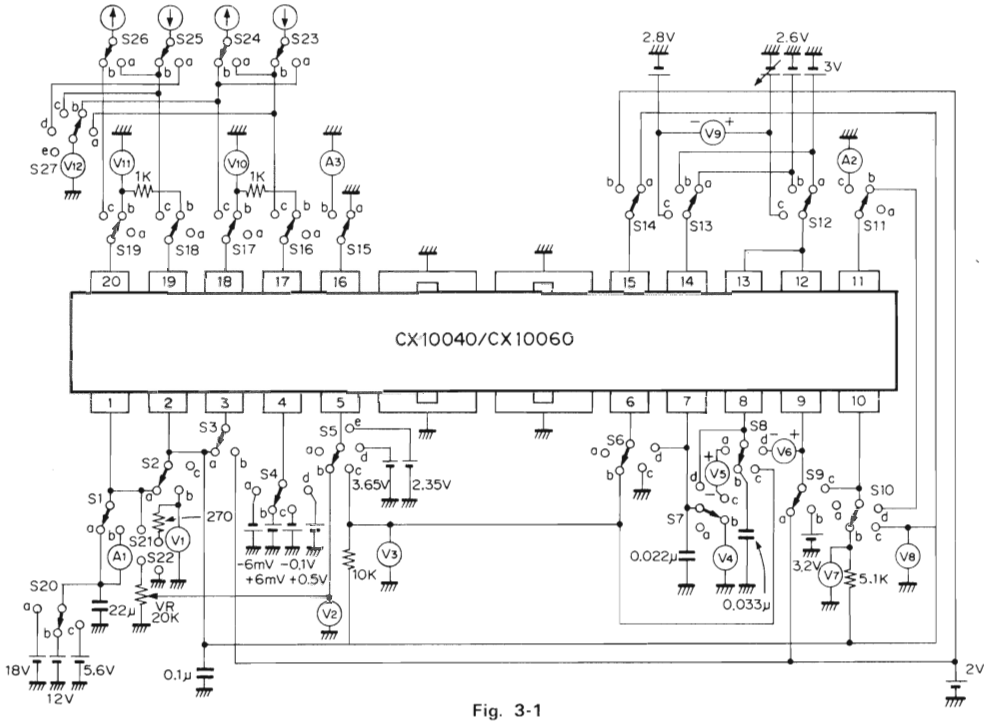


Fig. 3-1

Ilim

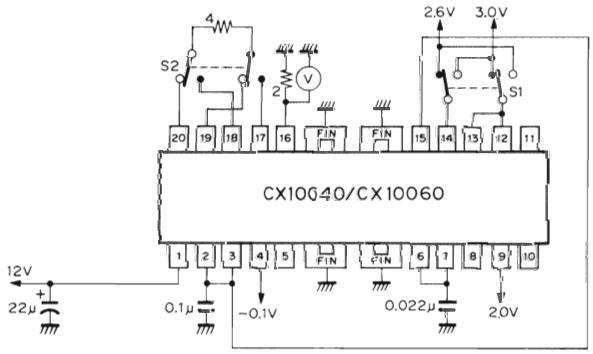


Fig. 3-2

- S1 ON and S2 OFF: The first phase limiter current (1)
- S1 ON and S2 ON: The second phase limiter current (1)
- S1 OFF and S2 OFF: The first phase limiter current (2)
- S1 OFF and S2 ON: The second phase limiter current (2)

ILO

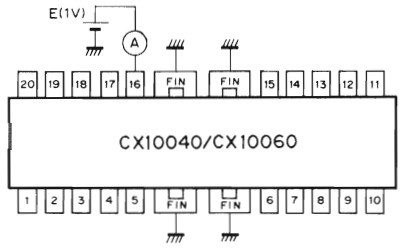


Fig. 3-3

Measure the leakage current between individual pins and GND.
Regarding the applying voltage, apply a voltage corresponding to the breakdown voltage of individual pins.

For example, apply 1V to pin 16.

TDP

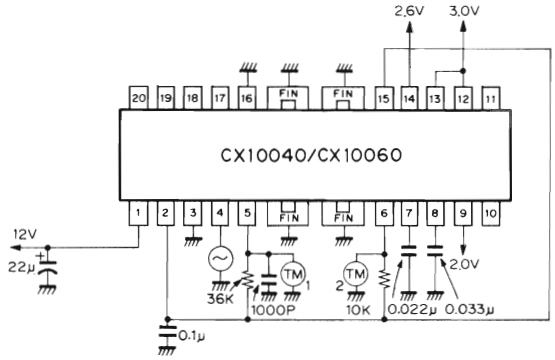


Fig. 3-4

- Apply a sine wave of 300 Hz and input 40 mVp-p to pin 4.
- Measure the time difference between the leading edge of waveform of pin 5 and that of pin 6.

FOUT

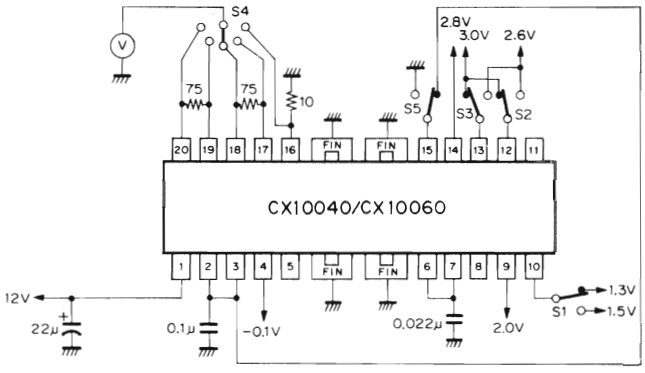


Fig. 3-5

- S1 ON and S2 ON: FOUT(1) and FOUT(3)
- S1 ON and S2 OFF: FOUT(2)
- S1 OFF and S2 OFF: FOUT(4) and FOUT(6)
- S1 OFF and S2 ON: FOUT(5)

KIo

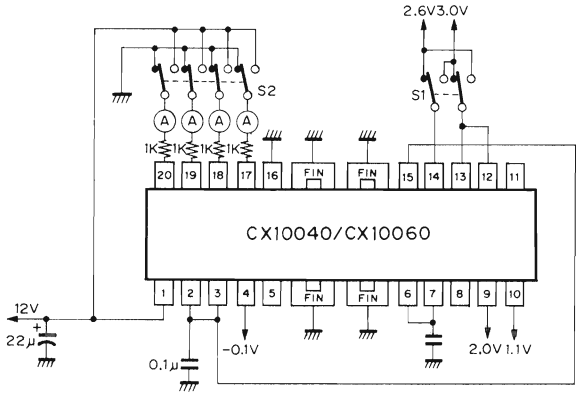


Fig. 3-6

- S1 ON and S2 OFF: Absorbing currents of pins 17 and 19
- S1 OFF and S2 OFF: Measure current ratios among these 4 absorbing currents of pins 18 to 20
- S1 OFF and S2 ON: Outflowing currents of pins 17 and 19
- S1 ON and S2 ON: Measure current ratios among these 4 outflowing currents of pins 18 to 20

$I_B(1)$, $I_B(2)$, KI_B

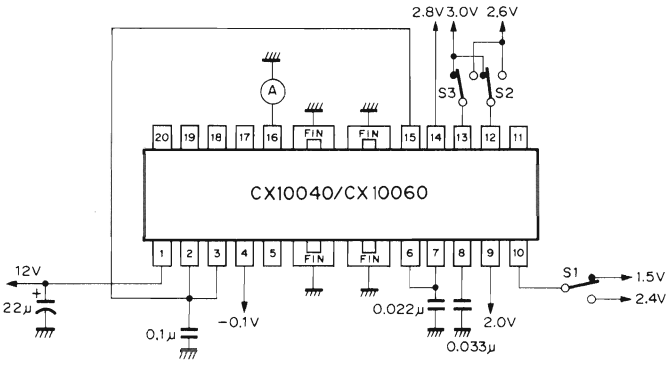


Fig. 3-7

- S1 ON: $I_B(1)$ and S2 OFF: $I_B(2)$
- Measure the current under the following 4 conditions and obtain their current ratios:
  S2 ON and S3 ON
  S2 ON and S3 OFF
  S2 OFF and S3 ON
  S2 OFF and S3 OFF

IOUT(1), (2), KIOUT, Vosat(u), (d), IROUT, KIROUT, $\Delta V\phi$

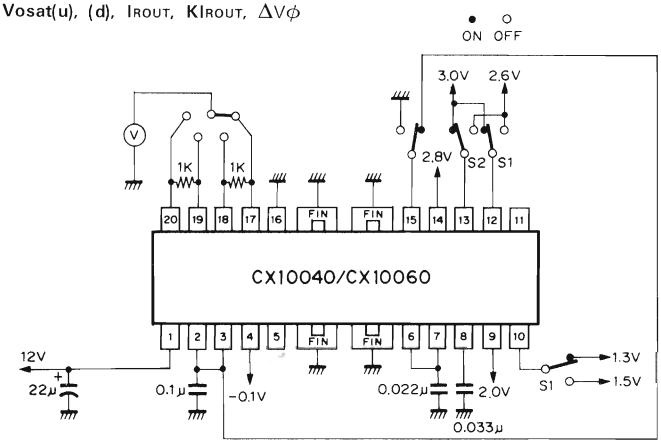


Fig.3-8

1. Measuring of IOUT, KIOUT and Vosat can be carried out when the currents flow in the directions of from pin ⑳ to pin ⑲ and from pin ⑱ to pin ⑰ under the conditions that S2, S3 and S5 are all switched ON. (Current IOUT(1) flows when S1 is switched ON and CUrrent IOUT(2) flows when S1 is OFF.)
2. Measuring of the individual items can be carried out when the currents flow in the directions of from pin ⑳ to pin ⑲ , and from pin ⑰ to pin ⑱ under the conditions that S2 is switched ON, S3 is OFF, and S5 is ON.
3. Measuring of the individual items can be carried out when the currents flow in the directions of from pin ⑲ to pin ⑳ , and from pin ⑱ to pin ⑰ under the conditions that S2 is switched OFF, and both S3 and S5 are ON.
4. Measuring of the individual items can be carried out when the currents flow in the directions of from pin ⑲ to pin ⑳ , and from pin ⑰ to pin ⑱ under the conditions that both S2 and S3 are switched OFF and S5 is ON.
5. Measuring of the individual items when the current flowing directions are inversed with S5 switched OFF.

- I_{OUT} ⑳ → ⑲, I_{OUT} ⑲ → ⑳ $= \dfrac{\text{Potential of pin 20} - \text{Potential of pin 19}}{75}$

  I_{OUT} ⑱ → ⑰, I_{OUT} ⑰ → ⑱ $= \dfrac{\text{Potential of pin 18} - \text{Potential of pin 17}}{75}$

  The current flowing directions of ⑲ → ⑳ and ⑰ → ⑱ become negative values in the above equation; therefore, when inversing them by multiplying (−1), the above eq. is also applied.
- Output saturation voltages between pins (upper side) are the potential difference between V_{CC} and pin ⑰ and V_{CC} and pin ⑱
- Output saturation voltages between pins (lower side) are the potential differences between pins ⑰ to ⑳ and pin ⑯

V_{OH} ⑩-1, V_{OH} ⑩-2

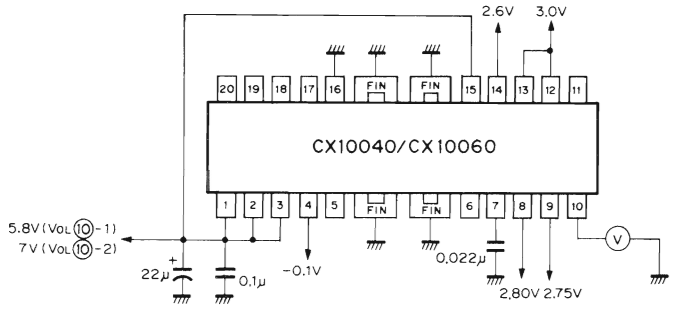


Fig. 3-9

V_{OL} ⑩-1, V_{OL} ⑩-2

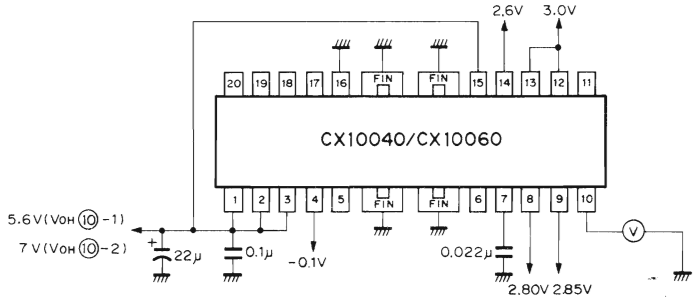


Fig. 3-10

Description of Operation

The CX10040/CX10060 are ICs which is comprised of a servo system which controls rotation of the motor with F/V converting and sample and hold circuits, and a drive system which drives the motor by a signal from the servo system. These two systems are incorporated within one chip as a F servo motor driving system.

FG output of the motor is amplified and waveform shaped by the FG amplifier, and it generates discharge pulse and sampling pulse by passing through the discharge and sampling pulse generating circuit. The holding voltage of the sample and hold capacitor is determined by these discharge pulse and sampling pulse.

This holding voltage becomes input voltage of the control amplifier of the final stage of the servo system, and the signal amplified by the control amplifier goes into the instruction current generating circuit and it controls the output of the hole amplifier to have the rotation of the motor become constant.

In addition, the driving system performes the following operations. The motor phase selecting signal from the hall devise is amplified by the hall amplifier. Since the previously mentioned signal current has been applied to the hall amplifier, the driving current to the final stage of the driving circuit is increased or decreased in accordance with the signal current.

In the final stage of the driving circuit, the output of the hall amplifier is current amplified to rotate the motor.

Waveforms of individual sections in the servo system

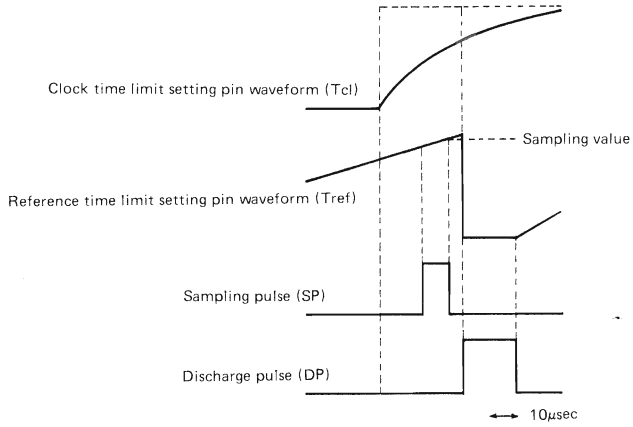


Fig. 4

The waveforms in individual circuits in a steady state are as shown in Fig. 5. If the number of rotations of the motor is increased, the FG frequency is increased. The frequency of Tcl waveform becomes increased in accordance with the increase of FG waveform. As a result, the repetition time of the SP and DP waveforms become smaller. Since the Tref waveform has a large time constant, the sampling value shown in Fig. 4 decreases its amount in accordance with the amount which has been reduced in the repetition time. When the holding voltage becomes low, the output of the controlling amplifier in the final stage also becomes low, and this tends to affect to reduce the signal current of the instruction current generating circuit to become lower than the initial state.
Accordingly, it causes to attenuate the number of rotations of the motor. Inversely, when the number of rotations of the motor is reduced, the output of the controlling amplifier becomes high to increase the number of rotations of the motor. As described above, the CX10040/CX10060 are disigned to maintain the rotation speed of their motor constantly by detecting the number of rotations of the motor with the FG, and to control the output of the hole amplifier by output of the controlling amplifier, that is a feedback loop.

The controlling of normal rotation and inverse rotation of the motor is carried out by switching the positive input — and negative input — of the hall amplifier. However, an electronic switchover circuit is incorporated within the CX10040/CX10060, and enabling control by potential switchover with their external pins.
In addition, switchover of the start and stop is carried out by dropping the output of the controlling amplifier of the final stage of servo system to Lo level, and thereby making the current to turn off of the instruction current generating circuit. As for the switchover, normal rotation and starting of the motor can be carried out by connecting the external pins of both circuits to the constant voltage output pin (5.6V), and inverse rotation and stopping of the motor can be carried out by dropping the potential lower than 2V.

Waveforms of individual pins and timing of sampling and discharge pulses

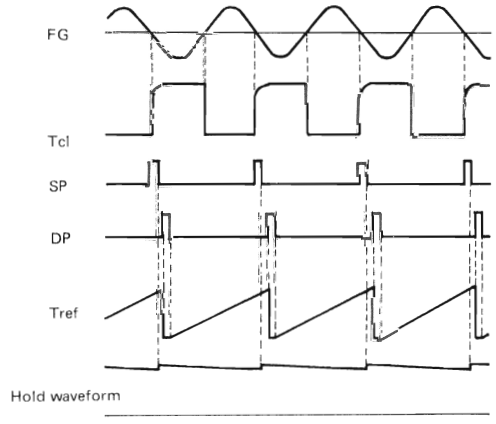


Fig. 5

OTM Motor Servo Control

Description

The CX20123 is a bipolar IC designed to be an OTM brushless motor servo amplifier for tape-recorders or turntables. It is most suitable for super-low voltage tape recorders such as the Walkman series.

OTM: One Sensor Two Phase Motor

Features

- Operational using a super-low voltage of the minimum 0.9V.
- Stable operation with a built-in differential FG.
- Control terminal for power ON/OFF is provided.

Structure

Bipolar silicon monolithic IC.

Absolute Maximum Ratings (Ta = 25°C)

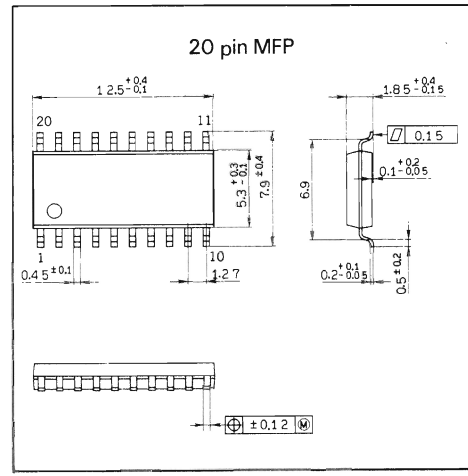
• Supply voltage	Vcc	4.5	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	660	mW

Recommended Operating Condition

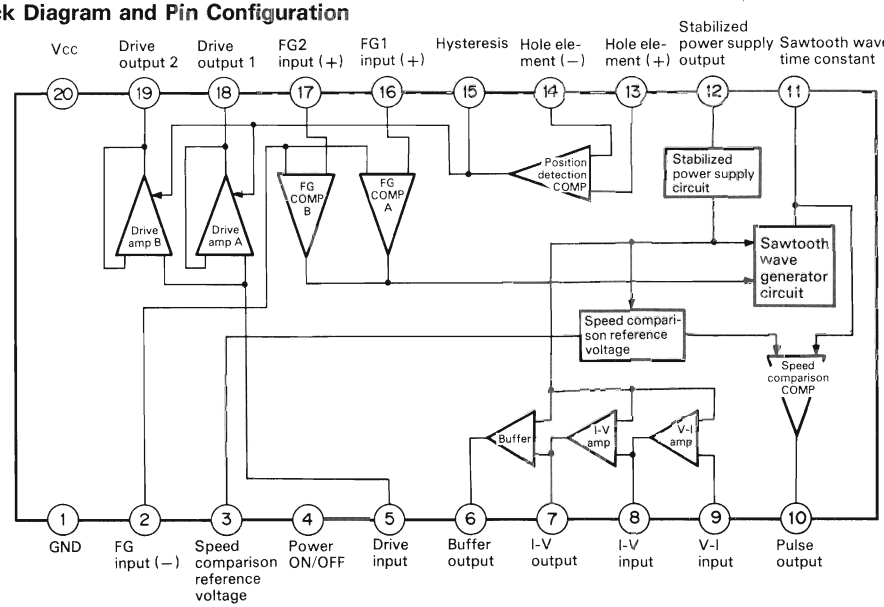
• Supply voltage	Vcc	0.9 to 4.2	V

Package Outline

Unit: mm



Block Diagram and Pin Configuration



Pin Description

No.	Name	Description	Reference DC voltage (V)
1	GND	Ground	0
2	FG input (−)	Gives a reference voltage for FG input. The ground voltage is supposed to be the reference but a divided voltage from the stabilized power supply is added because of voltage generation from printed circuit board handling, etc.	10m
3	Speed comparison reference voltage	0.566 times stabilized power supply voltage is generated for use as the speed comparison reference voltage. The speed can be increased by about 10% with an external resistor of about 100 kΩ.	0.38
4	Power ON/OFF	The IC ON/OFF operation is controlled only with the primary power supply Vcc. It can be used for dubbing or switching radio/tape recorder in the power supply ON/OFF. OFF: GND or OPEN. ON: Vcc	1.5
5	Drive input	Common input for both phases A and B. Input impedance > 100 kΩ	1.2
6	Buffer output	Output terminal of a DC amplifier with a gain of about 24 dB.	1.2
7	I-V output	I → V conversion amp output with an external LPF for converting a pulse duty with speed information to a DC voltage.	0.3
8	I-V input	The above I-V converted amplification is input in current pulse.	0.66
9	V-I input	V → I conversion amp input for converting the voltage pulse to a current pulse.	0.66
10	Pulse output	Pulse signal with its width incorporating speed information is input.	0
11	Sawtooth wave time constant	Terminal generating a sawtooth wave by an FG signal with an external CR time constant; it is charged from the stabilized power supply.	0.66
12	Stabilized power supply output	Stabilized DC voltage output terminal designed to withstand a primary power supply change. It is used as the internal reference voltage as well as for driving the hole element.	0.66
13	Hole element input (+)	Hole element (+) input terminal for position detection. Input impedance > 50 kΩ	0.3
14	Hole element input (−)	Hole element (−) input terminal for position detection. Input impedance > 50 kΩ	0.3
15	Hysteresis	Output terminal for giving a hysteresis to the position detection comparator. It is connected to Pin 14 via a resistor.	0
16	FG1 input (+)	Comparator input to retrieve speed information with a coil counter electromotive force voltage.	0
17	FG2 input (+)	In addition to the above, one more phase comparator is input.	0
18	Drive output 1	A phase driver output terminal for 2-phase motor driving.	0
19	Drive output 2	B-phase predriver output terminal	1.2
20	Vcc	Primary power supply terminal. Connectable to various equipment with one or two manganese batteries.	1.5

Electrical Characteristics

0 dBs = 0.775V (Ta = 25°C, See the Electrical Characteristics Measurement Circuit)

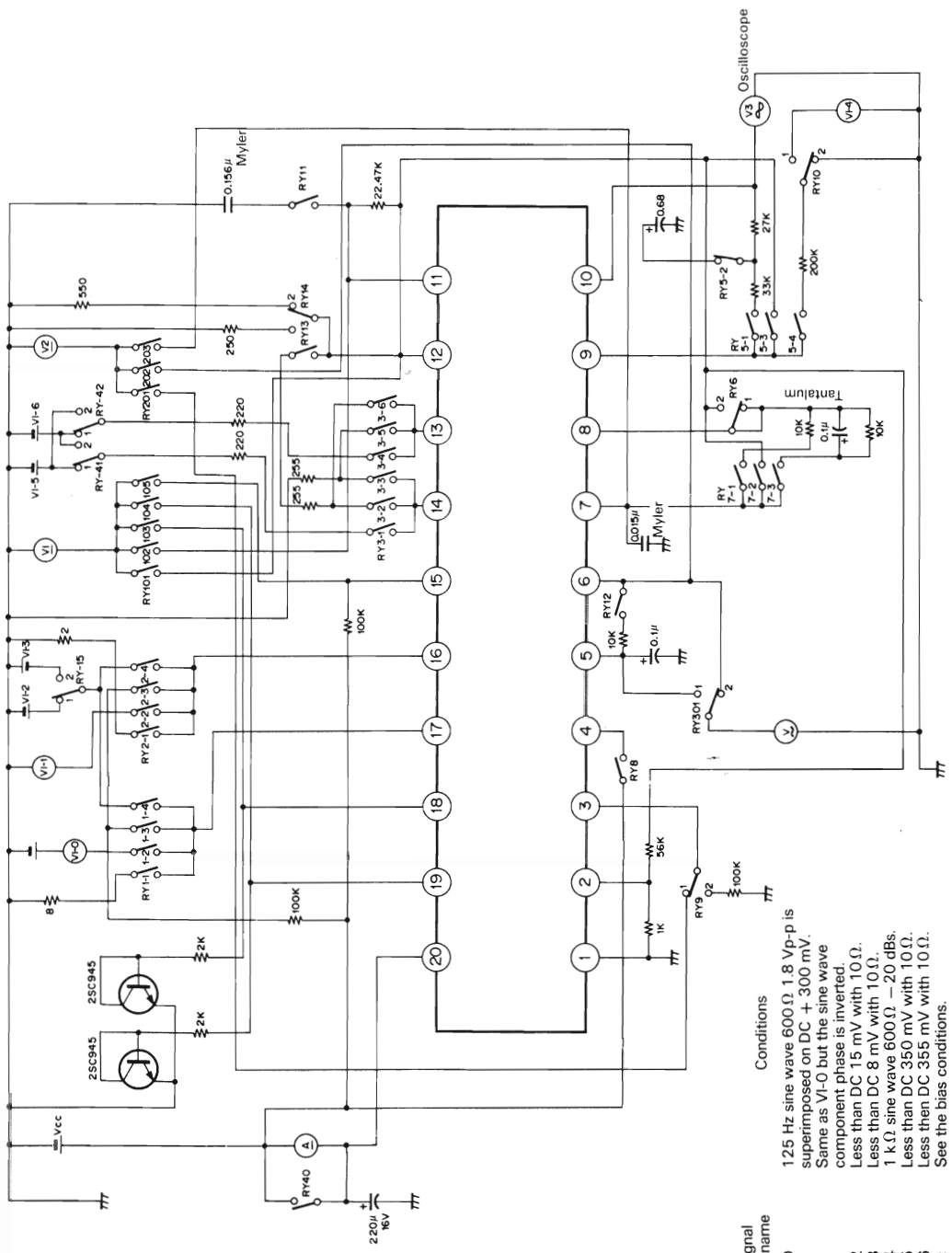
No.	Measuring item	Symbol	SW conditions		Bias condition		Measurement point	Description of output waveform and measurement method	Min.	Typ.	Max.	Unit
			ON switch	Switch position	V_{CC} (V)	V_1						
1	Circuit current when power is off	ID1	1-1, 2-1, 101, 3-3, 3-6, 13, 7-3, 12, 201,	15=1, 4=2, 10=1, 6=1, 301=1, 9=1, 41=2, 42=1,	1.8		A	DC current measurement		0.2	5.5	μA
2	Circuit current during no signal	ID2	1-1, 2-1, 101, 3-3, 3-6, 13, 7-3, 12, 8, 201,	15=1, 4=1, 10=1, 6=1, 301=1, 9=1, 41=2, 42=1,	1.8		A	DC current measurement (After this, the ammeter is shorted with RY40.)	2.7	6	11.6	mA
3	Stabilized power supply output voltage	V1	1-1, 2-1, 101, 3-3, 3-6, 13, 7-3, 12, 8, 201, 40,	15=1, 4=2, 10=1, 6=1, 301=1, 9=1, 41=2, 42=1,	1.2		V1	DC current measurement	590	680	780	mV
4	Voltage division ratio of the speed comparator reference voltage	V2	1-1, 2-1, 101, 3-3, 3-6, 13, 7-3, 12, 8, 201, 40,	15=1, 4=2, 10=1, 6=1, 301=1, 9=1, 41=2, 42=1,	1.2		V2/V1	Process using the result of item 3 after measuring the DC voltage.	49.8	57.3	65.2	%
5	Activating operation	V3	1-1, 2-1, 102, 3-3, 3-6, 13, 7-3, 12, 8, 201, 40,	15=1, 4=2, 10=1, 6=1, 301=1, 9=1, 41=2, 42=1,	1.0		V1	FG input is grounded with 2Ω. At this time, whether the sawtooth wave discharging Tr (Pin 11) is off can be determined by measuring the DC voltage with V1.	581	660	770	mV
6	Saturation voltage of sawtooth wave discharging transistor	V4(SAT)	1-3, 2-3, 102, 3-3, 3-6, 13, 7-3, 12, 8, 201, 40,	15=1, 4=2, 10=1, 6=1, 301=1, 9=1, 41=2, 42=1,	1.0		V1	Saturation voltage of the sawtooth wave discharging (Pin 11) is determined by measuring DC voltage with V1, with FG input biased by the power supply voltage.	—	4	6.6	mV
7①	FG comparator A Offset 1	V15-1 (O.S)	1-3, 2-4, 102, 3-3, 3-6, 13, 7-3, 12, 8, 201, 40,	15=1, 4=2, 10=1, 6=1, 301=1, 9=1, 42=2, 42=1,	1.2	V_I-2	V1	Pin 11 is determined as on by applying V_I-2 to FG input A (Pin 16), with FG input B (Pin 17) biased by the power supply voltage.	—	10	110	mV
7②	FG comparator A Offset 2	V15-2 (O.S)	1-3, 2-1, 102, 3-3, 3-6, 13, 7-3, 12, 8, 201, 40,	15=1, 4=2, 10=1, 6=1, 301=1, 9=1, 41=2, 42=1,	1.2		V1	Bias FG input B (Pin 17) by the power supply voltage and ground FG input A (Pin 16) using 2Ω and determine if Pin 11 is on.	450	660	770	mV
7③	FG comparator A Offset 3	V15-3 (O.S)	1-3, 2-4, 102, 3-3, 3-6, 13, 7-3, 12, 8, 201, 40,	15=2, 4=2, 10=1, 6=1, 301=1, 9=1, 41=2, 42=1,	1.2	V_I-3	V1	Pin 11 is determined as off by applying V_I-3 to FG input A (Pin 16), with FG input B (Pin 17) biased by the power supply voltage.	450	660	770	mV
8①	FG comparator B Offset 1	V16-1 (O.S)	1-4, 2-3, 102, 3-3, 3-6, 13, 7-3, 12, 8, 201, 40,	15=1, 4=2, 10=1, 6=1, 302=1, 9=1, 41=2, 42=1,	1.2	V_I-2	V1	Pin 11 is determined as off by applying V_I-3 to FG input A (Pin 16), with FG input A (Pin 16) biased by the power supply voltage.	—	10	110	mV
8②	FG comparator B Offset 2	V16-2 (O.S)	1-1, 2-3, 102, 3-3, 3-6, 13, 7-3, 12, 8, 201, 40,	15=1, 4=2, 10=1, 6=1, 301=1, 9=1, 41=2, 42=1,	1.2		V1	Bias FG input A (Pin 16) by the power supply voltage and ground FG input B (Pin 17) using 2Ω and determine if Pin 11 is on.	450	660	770	mV
8③	FG comparator B Offset 3	V16-3 (O.S)	1-4, 2-3, 102, 3-3, 3-6, 13, 7-3, 12, 8, 201, 40,	15=2, 4=2, 10=1, 6=1, 301=1, 9=1, 41=2, 42=1,	1.2	V_I-3	V1	Pin 11 is determined as off by applying V_I-3 to FG input B (Pin 17), with FG input A (Pin 16) biased by the power supply voltage.	450	660	770	mV

SONY

No.	Measuring item	Symbol	SW conditions		Bias condition		Measurement point	Description of output waveform and measurement method	Min.	Typ.	Max.	Unit
			ON switch	Switch position	V_{CC} (V)	V_I						
9	Output pulse width	P.W(OUT)	1-2, 2-2, 11, 3-3, 3-6, 13, 5-1, 7-3, 12, 8, 40,	15=2, 4=2, 10=1, 6=1, 30I=1, 9=1, 41=2, 42=1,	1.2	V_I-0 V_I-1	V3 ∿	Pseudo FG is input and a sawtooth wave time constant is set. Measure the pulse width with a speed comparator resistor load.	252	340	495	μs
10	Speed increasing operation	P.W(S.U)	1-2, 2-2, 11, 3-3, 3-6, 13, 5-1, 7-3, 12, 8, 40,	15=2, 4=2, 10=1, 6=1, 30I=1, 9=2, 41=2, 42=1,	1.2	V_I-0 V_I-1	V3 ∿	Set as stated above, and measure the pulse width through setting the speed increasing conditions.	450	610	770	μs
11	Voltage after buffer output	V5(SAT)	1-2, 2-2, 102, 11, 3-3 3-6, 13, 5-3, 7-2, 12 8, 202, 40,	15=2, 4=2, 10=1, 6=2, 30I=1, 9=1, 41=2, 42=1,	1.8		V2	Short both V-I and I-V conversion outputs to the stabilized power supply and measure the buffer output DC voltage.	45	110	165	mV
12	Signal transmission gain	G1	1-2, 2-2, 102, 11, 3-3 3-6, 13, 5-4, 7-1, 8, 40,	15=2, 4=2, 10=1, 6=1, 30I=2, 9=1, 41=2, 42=1,	1.2	V_I-4	V ∿	Measure the gain before the buffer output by adding DC bias and V_I-4 to the V-I conversion input at 200 kΩ.	−6.5	−4	−1.5	dB
13	Drive A maximum output voltage	V6(DOA)	1-1, 2-1, 103, 11, 3-2 3-5, 13, 5-1, 5-2, 7-1 12, 8, 202, 40,	15=2, 4=2, 10=1, 6=1, 30I=2, 9=1, 41=2, 42=1,	1.0		V1	Ground FG input with 2 Ω and measure the drive A (ON) DC voltage by setting a position detection input.	783	890	1012	mV
14	Drive B maximum output voltage	V7(DOB)	1-1, 2-1, 104, 11, 3-3 3-6, 13, 5-1, 5-2, 7-1 12, 8, 202, 40,	15=2, 4=2, 10=1, 6=1, 30I=2, 9=1, 41=2, 42=1,	1.0		V1	Measure the drive B (ON) DC voltage by setting as item 13.	783	890	1012	mV
15①	Position detection comparator offset voltage ①	V17-1 (O.S)	1-1, 2-1, 105, 11, 3-1 3-4, 5-1, 5-2, 7-1, 12 8, 202, 40,	15=2, 4=2, 10=1, 6=1, 30I=2, 9=1, 41=2, 42=1,	1.2	V_I-5	V1	Determine whether the output (Pin 15) is on by applying V_I-5 and V_I-6 to the position detection input.	—	20	110	mV
15②	Position detection comparator offset voltage ②	V17-2 (O.S)	1-1, 2-1, 105, 11, 3-1 3-4, 5-1, 5-2, 7-1, 12 8, 202, 40,	15=2, 4=2, 10=1, 6=1, 30I=2, 9=1, 41=1, 42=2,	1.2	V_I-6	V1	Determine whether the output (Pin 15) is off by applying V_I-5 and V_I-6 to the position detection input.	1.0	1.15	1.3	V
16	Buffer DC operation point	V19(P)	1-1, 2-1, 101, 11, 3-1 3-4, 5-2, 5-4, 7-3, 12 8, 40,	15=2, 4=2, 10=2, 6=1, 30I=2, 9=1, 41=1, 42=2,	1.2	RY5-4 (200kΩ)	V2-V1	Measure the voltage difference between the buffer output DC operating voltage and the stabilized power supply, with the V-I conversion input grounded with 200 kΩ.	−165	−100	−45	mV
17	Carrier ripple	V20(RIP)	1-2, 2-2, 101, 11, 3-1 3-4, 5-1, 5-2, 7-3, 12 8, 202, 40,	15=2, 4=2, 10=2, 6=1, 30I=1, 9=1 41=1, 42=2,	1.2	V_I-0 V_I-1	V ∿	Measure carrier ripple before drive amp input with a pseudo FG input. (AC voltage)	−58	−53	−48	dBs
18	Overvoltage operation	V21(RIP)	1-2, 2-2, 101, 11, 3-1 3-4, 5-1, 5-2, 7-3, 12 8, 202, 40,	15=2, 4=2, 10=2, 6=1, 30I=1, 9=1, 41=1, 42=2,	4.2		V ∿	Measure carrier ripple change when the power supply voltage is changed with the above input.	−57	−52	−47	dBs

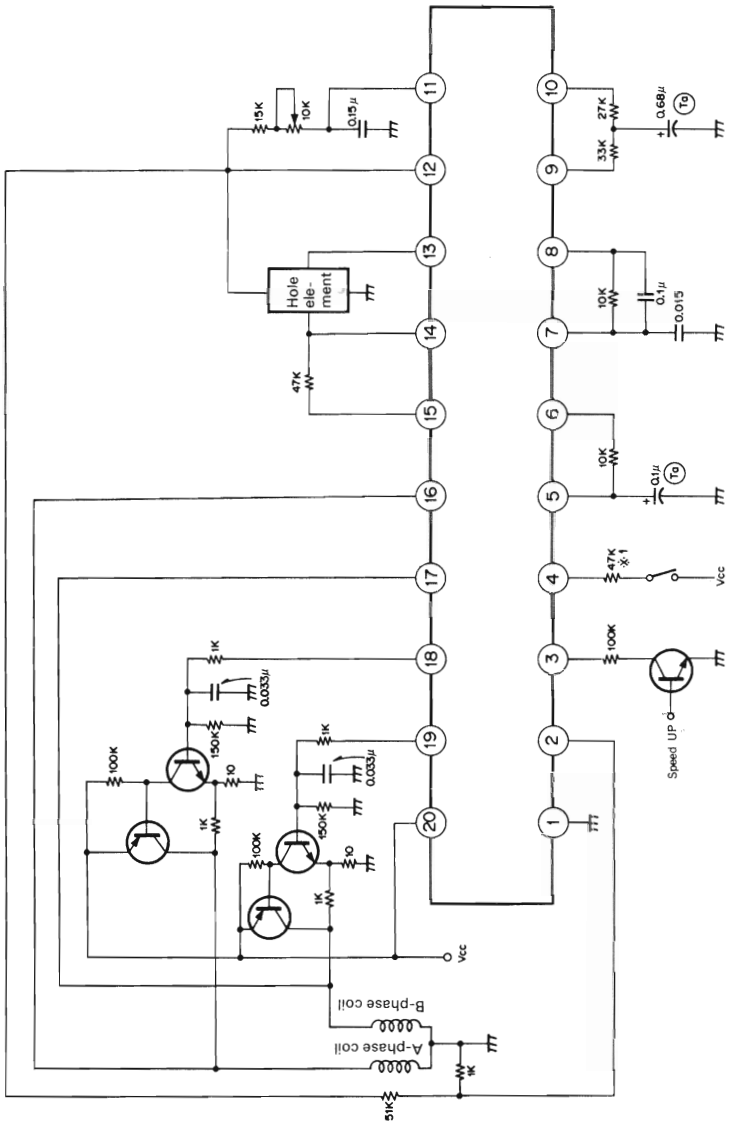
SONY

Electrical Characteristics Measuring Circuit



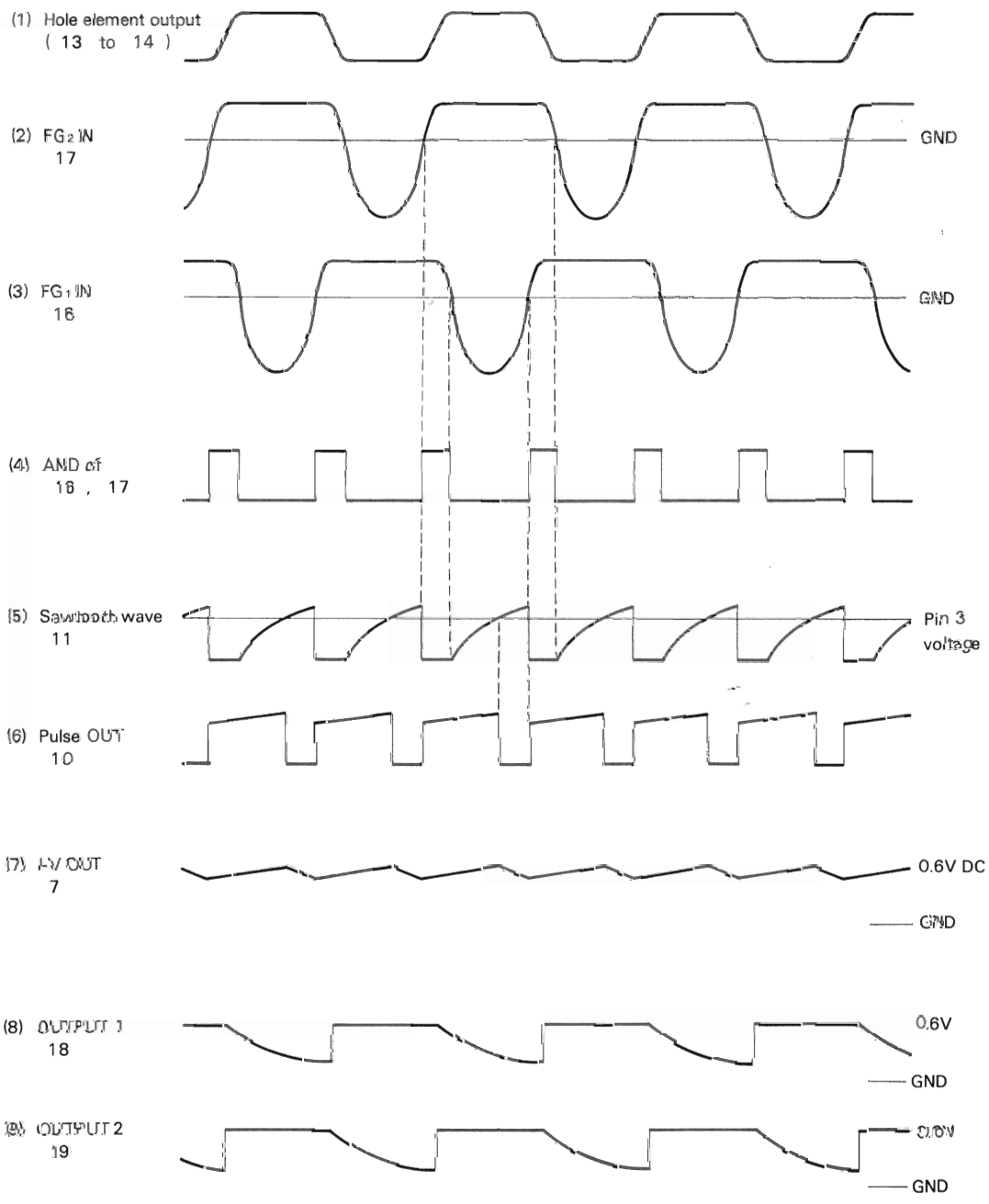
Input signal source name	Conditions
VI-0	125 Hz sine wave 600 Ω 1.8 Vp-p is superimposed on DC + 300 mV.
VI-1	Same as VI-0 but the sine wave component phase is inverted.
VI-2	Less than DC 15 mV with 10 Ω.
VI-3	Less than DC 8 mV with 10 Ω.
VI-4	1 kΩ sine wave 600 Ω – 20 dBs.
VI-5	Less than DC 350 mV with 10 Ω.
VI-6	Less then DC 355 mV with 10 Ω.
Vcc	See the bias conditions.

Application Circuit



※1: Not required when the applied voltage is < 1.5V.

Timing Chart



Description of Operation

The speed signal is detected with zero cross at the FG amp from the coil counter electromotive force, and amplified; its waveform is then rectified before both its phases are processed through AND logic and transmitted to the sawtooth generating circuit. The FG amp (Timing Chart Figs. 2, 3 and 4) is a comparator to compare the Pin 2 voltage with inputs of Pins 16 and 17. Therefore, unless a proper offset is given to Pin 2 in activation, the comparator is not inverted and only "High" is output from the AND gate and thereby neither a sawtooth wave is generated and nor is the motor activated. To prevent this possibility, a bias of about 10 mV is required for Pin 2 as shown in the application example.

The sawtooth wave is generated by repeatedly discharging the external capacitor discharge pulse (Timing Chart Fig. 4) of Pin 11 and charging with a time constant by using a resistor connected to the stabilizing power supply output Pin 12. The Pin 11 time constant is set to about 80% of the cycle of the discharging pulse (Timing Chart 4, 5).

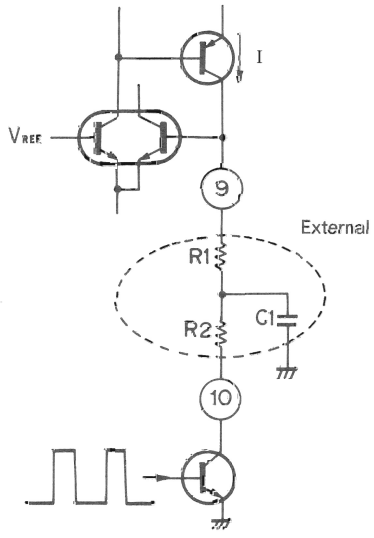


Figure (a)

where R1, R2 > 10 kΩ

Then, a pulse which becomes "high" when the sawtooth wave voltage is higher than Pin 3 voltage is generated. As Pin 10 is an open collector output, the above pulse is input to the transistor base to generate a wave form as shown in the Timing Chart Fig. 6. The equivalent circuit is shown in Fig. (a).

Pin 9 is connected to Pin 10 via two resistors and a capacitor as shown in Fig. (a). These external components of resistors and a capacitor constitute an LPF in which R1 and C1 determine a time constant in charging and R2 and C1 in discharging. The Pin 9 voltage is compared with the Pin 12 V_{REF}, and current I is output when Pin 9 voltage is lower. By increasing R1, the discharging becomes slower and vice versa; also, the current amount can be increased by lowering the Pin 9 voltage, thus increasing the V-I conversion gain and vice versa. However, because the R1 and R2 values determine the current, both resistors must be over 10 kΩ so that the current remains within the allowable value in the IC transistor. And the time constant value must be sufficiently larger than the Pin 10 pulse cycle, otherwise the smoothing effect is affected. Then, the time constant will have to be determined by the cut and try method in connection with the I-V conversion gain.

Next, I-V conversion will be described. A resistor and capacitor are connected in parallel between Pin 8 and Pin 7 to form an LPF. With a larger resistor value, the gain increases. A capacitor of about 0.015 μF is connected to Pin 7 to eliminate oscillation. Pin 6 is a buffer output after the I-V conversion and input to the drive amp. Pins 5 and 6 are connected with an LPF for which C and R do not influence the gain value.

Pins 13 and 14 are inputs for the hole element amp. When Pin 13 input is higher than that of Pin 14 drive amp A is switched off; otherwise drive amp B is switched off. A resistor is connected across Pin 14 and Pin 15 so that the drive amp switching may have a hysteresis. As Pin 15 is an open collector output, the Pin 14 voltage is lowered when the Pin 13 voltage is higher than that of Pin 14. Therefore, its larger resistor makes the hysteresis smaller. However, the resistor must be over 10 kΩ as a resistor which is too small makes the hole element input harder to invert.

With the above operation, the A phase and B phase 180° are supplied to Pins 18 and 19 to switch ON/OFF the external drive circuit which drives the motor.

OTM Motor (One Sensor Two Phase Motor)

The OTM motor principle is in Fig. A. When the rotor is rotated, the counter electromotive force is generated in the coil as shown in Fig. B.

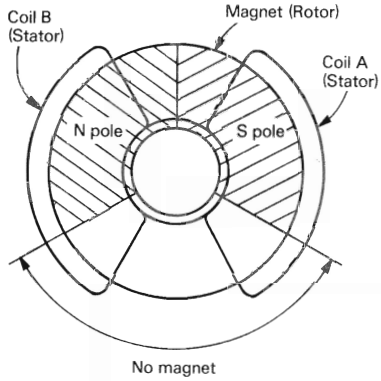


Fig. A

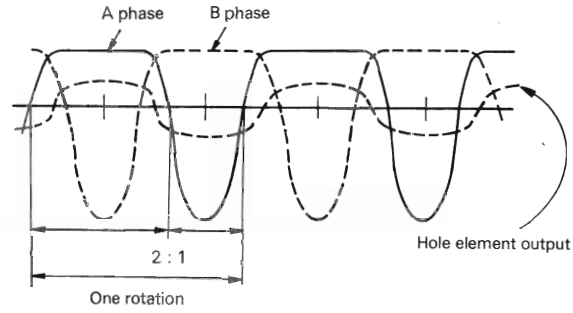


Fig. B

The magnetized section angle of the N and S poles is denoted in the following equation. The coil opening angle is the same.

$$\frac{360}{n} \times \frac{2}{3} = x^\circ \qquad (n \text{ is the number of poles: } n = 2, 4, 6 \cdots\cdots)$$

Therefore, when n = 2 (Fig. A), the magnetized section angle is 120°.
When n = 4 and n = 6, the magnetized angle will be as shown in Fig. C.

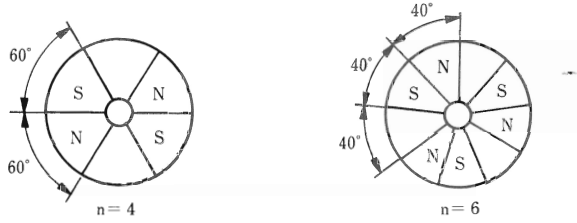


Fig. C

The sensor position must be as per Fig. B in terms of as the hole element output. The OTM motor, however, has sections of no magnetization as described above and generates portions where no hole element is output. Therefore, a magnetization technique is needed for the hole element detection. An example is shown in Fig. D.

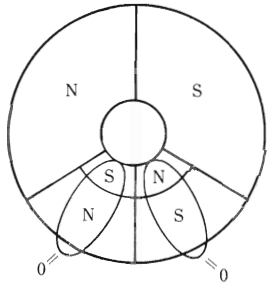
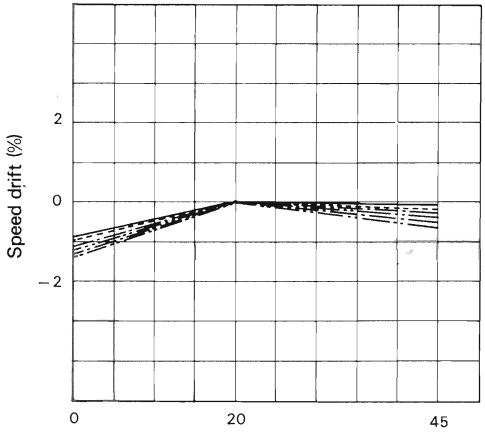


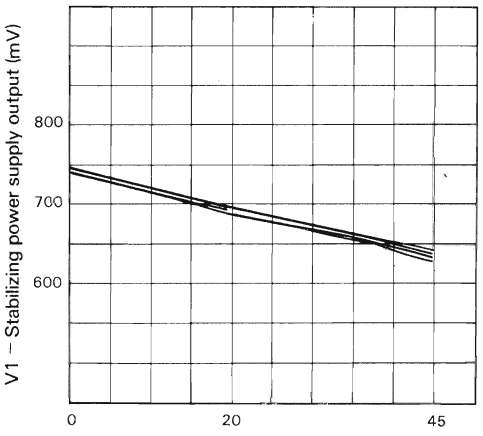
Fig. D

When the hole element is positioned at the outermost circumference as shown in Fig. D, it is tantamount to having only two poles of N and S. Furthermore, the counter electromotive force generated in the coil creates an effect similar to no magnetization.

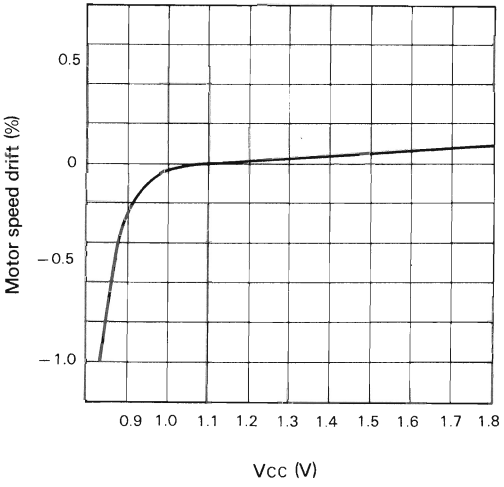
Speed Drift Temperature Characteristics



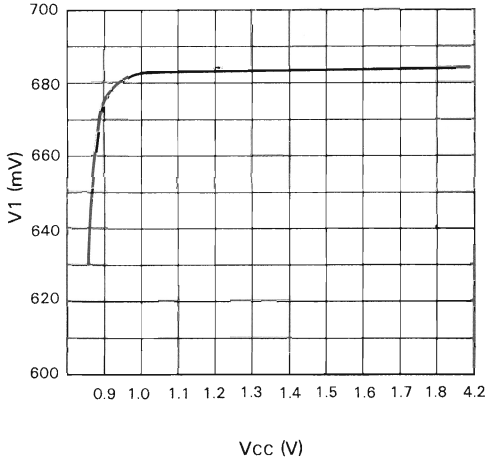
V1 Temperature Characteristics

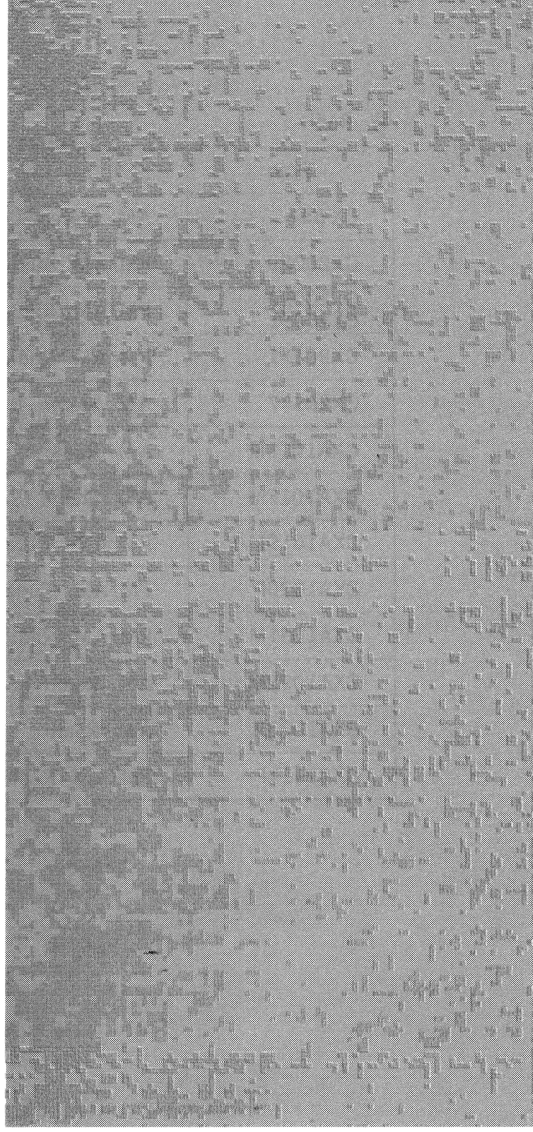


Motor Speed Power Supply Voltage Characteristics

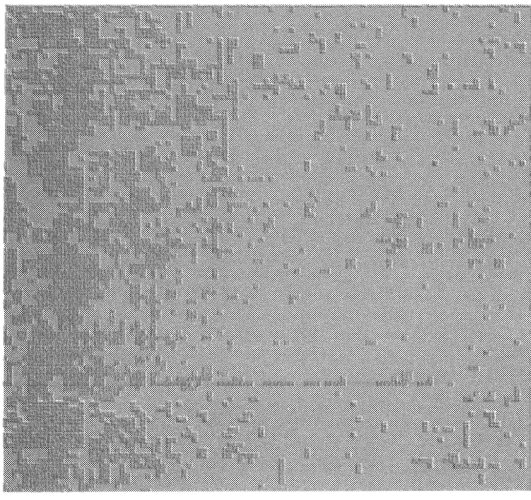


V1 vs. Power Supply Voltage Characteristics (Ta = 25°C)





Radio



4) Radio

Type	Function	Page
CX-857	AM Stereo Decoder	223
CX20029	FM/AM Stereo Radio	234
CX20090 CX20091	FM/AM Radio Circuit	240
CX20111	FM/AM Radio	247
CX20177	AM Stereo Radio	261
CXA1015M	AM Radio	281
CXA1017M	AM Stereo Radio	289
CXA1019M/P	FM/AM Radio	308
CXA1030P	FM/AM Tuner	318
CXA1031M	FM/AM Radio	332
CXA1032M	AM Radio	342
CXA1033P	AM Radio	351
CXA1111P	FM/AM Radio (P)	362

(P) : Preliminary

SONY CX-857

AM Stereo Decoder

Description

The CX-857 is an IC designed for PLL (Phase Locked Loop) synchronous detection, with the following functions especially required for AM stereo demodulation.

- Envelope detector or PLL sync AM detector
- PLL orthogonal sync detector
- Division-type inverse modulator
- Muting circuit
- PM (Phase Modulation) detection
- OP AMP circuit

Features

- A wide range of operating power supply voltage (Vcc = 1.9 to 12V)
- Compatible with all AM stereo systems (Motorola, Kahn/Hezeltine, Magnavox and Harris).
- A wide capture range due to the adaption of PLL system with variable capture range.

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	15	V
• Operating temperature	Topr	−10 to +70	°C
• Storage temperature	Tstg	−50 to +125	°C
• Allowable power dissipation	PD	670	mW
	$I_{O1\,1}$	≦ 10mA	
	$I_{O1\,2}$	≧ −10mA	

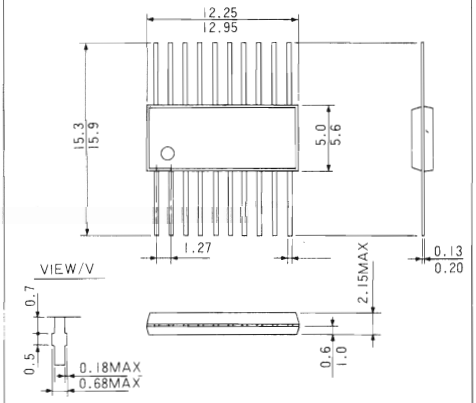
Recommended Operating Condition

• Supply voltage	Vcc	1.9 to 12	V

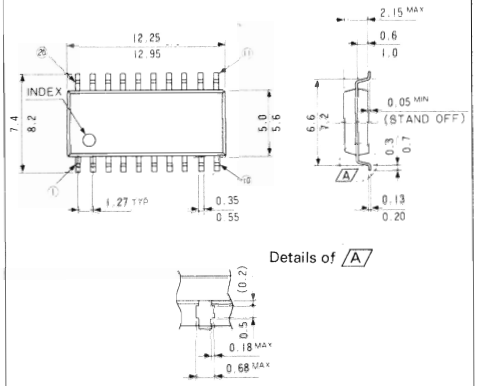
Package Outline

Unit: mm

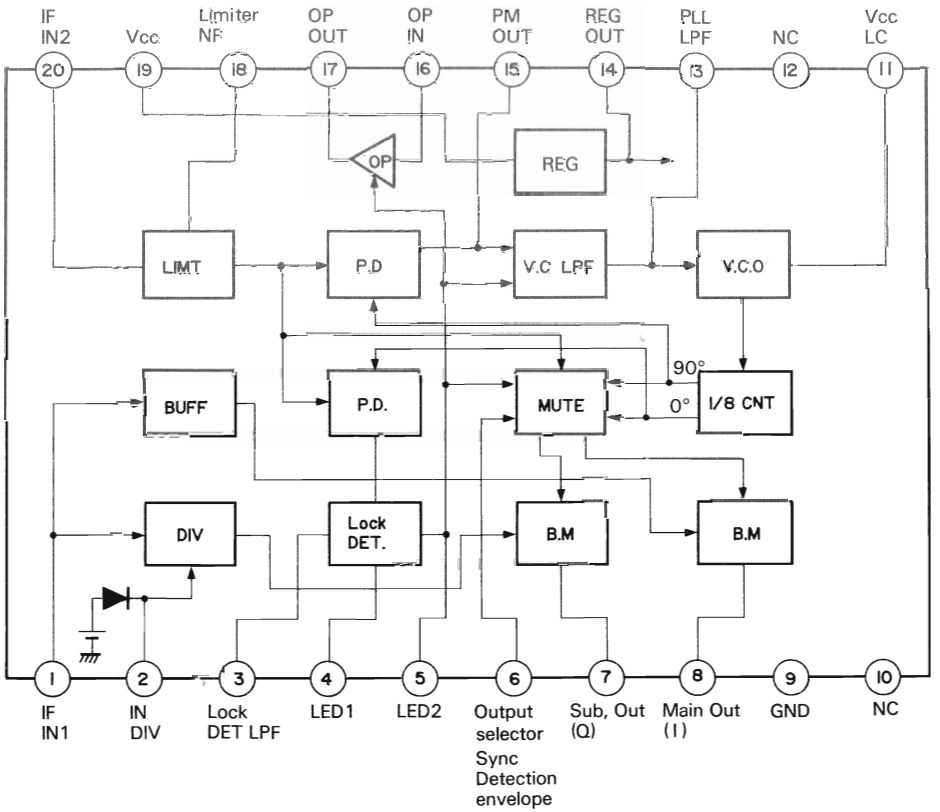
20 pin MFP (Straight type)



20 pin MFP (L type)



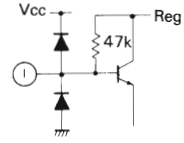
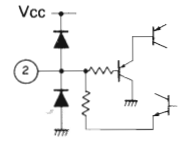
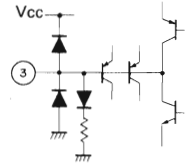
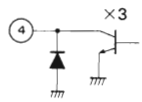
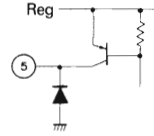
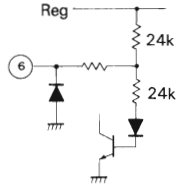
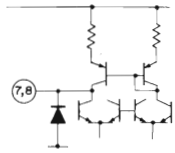
Block Diagram

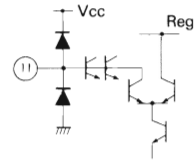
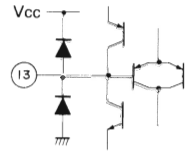
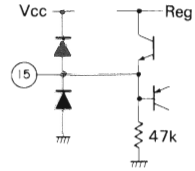
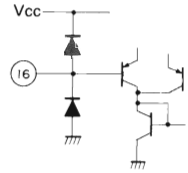
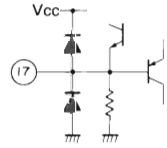
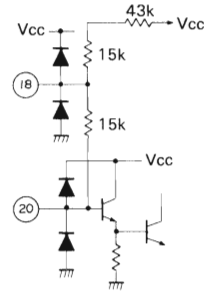


DIV: Divider
P.D: Phase Detector
B.M: Ballanced Modulator
LIMT: Limiter
Op: Operational Amp
REG: Regulator
V.C.O: Voltage Controlled Oscillator
CNT: Counter
LPF: Low Pass Filter
PLL: Phase Locked Loop

SONY

Pin Description

No.	Symbol	Voltage (V)	Equivalent Circuit	Description
1	IF IN	2.95		Input pin for IF signal
2	INV MOD IN	0.1		Input pin for divider
3	LOCK DET LPF	0.15		LPF for PLL lock detection
4	LED 1	10.4		LED activating circuit for PLL lock display
5	LED 2	0		MUTE drive pin
6	Output selector	2.2		Switchable between sync detection when connected to GND and envelope detection when open
7 8	Sub ch OUT Main ch OUT	2.5 2.8		L−R or L+R is output each
9	GND	0		GND
10	NC	–		

No.	Symbol	Voltage	Equivalent Circuit	Description
11	VCO	3.0		Oscillation coil for 3.6MHz is connected.
12	NC	–		
13	PLL LPF	2.3		LPF for PLL Vco is connected.
14	REG OUT	3.0		Regulator pin
15	PM OUT	1.9		PM (Phase Modulator) output pin
16	OP IN	1.9		OP AMP input pin
17	OP OUT	1.3		OP AMP output pin
18 20	LIMITER NF LIMITER IF IN	2.8 2.8		Limiter AMP input pin and NF pin
19	Vcc	12.0		Power supply

Test Conditions

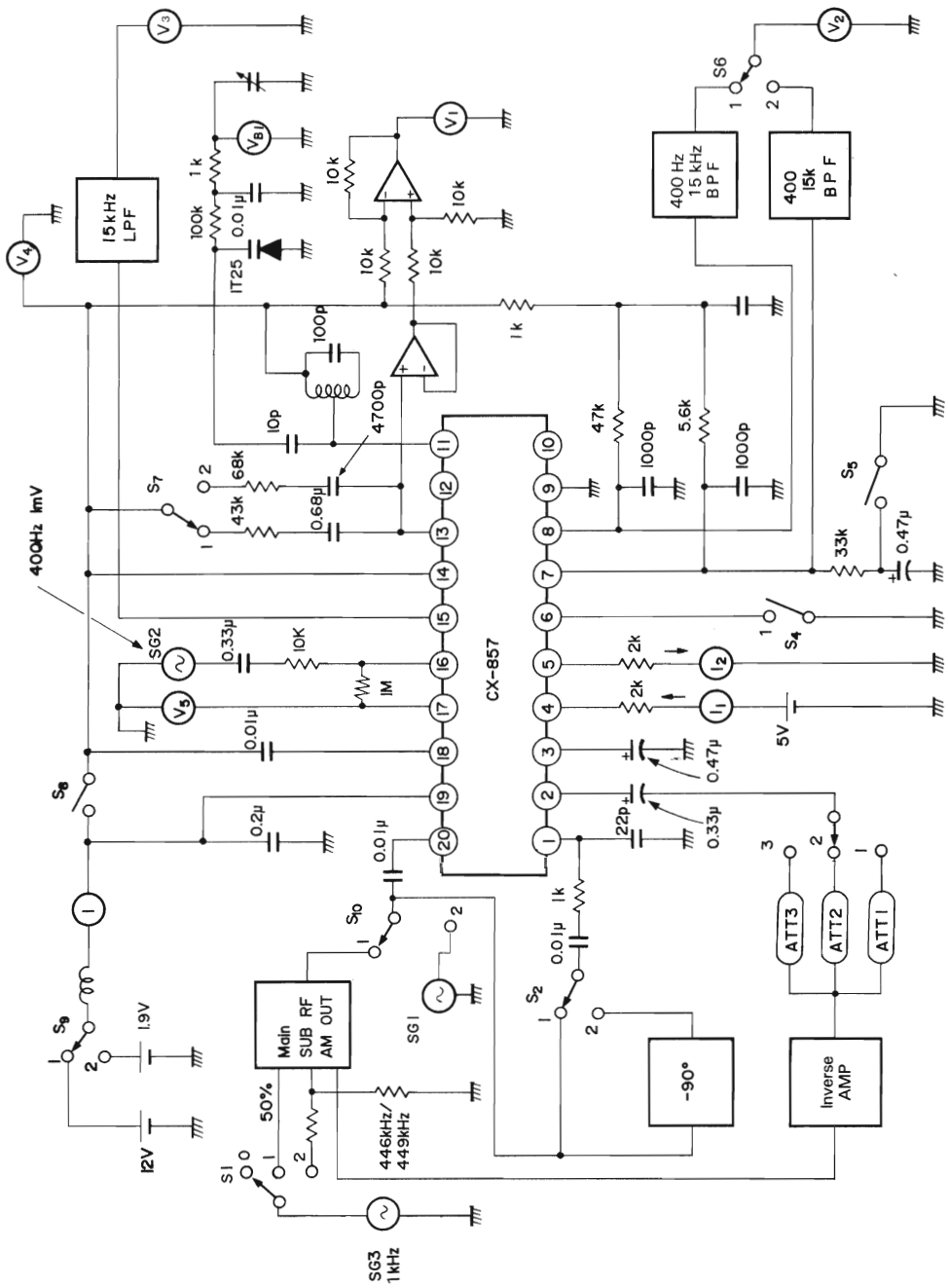
(Ta = 25°C, Vcc = 12V, see Fig. 2)

No.	Item	Symbol	SW conditions S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	Conditions	Test Point	Min.	Typ.	Max.	Unit
1	Circuit current	Icc	0	1	0	0	1	1	1	0	1	1	Non-modulation	I_3(mA)	5.0	7.4	11	mA
2	Reference voltage	Vrf	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	V_4(V)	2.7	2.95	3.2	V
	Free run adjustment												Adjust VB1 so V1 becomes 1.11V.					
3	LED current 1	$Io\|_1$	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	I_1	1.9	2.46		mA
4	LED current 2	$Io\|_2$	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	I_2		−0.64	−0.45	DA
5	Envelope output	Voe_1	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	1kHz 50%	V_2	−24.5	−21.4	−17.5	dBV
6	Envelope distortion factor	Dse	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	V_2 distortion factor		0.1	0.5	%
7	M→S cross talk 1	Cts1	↓	↓	↓	↓	↓	2	↓	↓	↓	↓	↓	V_2(dBV)		−61	−39	dBV
8	Main ch output	Vom	↓	↓	↓	1	↓	1	↓	↓	↓	↓	↓	V_2(dBV)	−24.5	−21.5	−17.5	dBV
9	Main ch distortion factor	Dsm	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	V_2 distortion factor		0.1	0.5	%
10	S→M cross talk	Ctm	↓	2	↓	↓	0	↓	↓	↓	↓	↓	↓	V_2(dBV)		−51	−39	dBV
11	Sub ch output 1	Vos1	↓	↓	↓	0	↓	2	↓	↓	↓	↓	↓	V_2(dBV)	−24.5	−21.6	−17.5	dBV
12	Sub ch distortion factor	Dss	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	V_2 distortion factor	0.2	0.2	0.8	%
13-1	Division error	ΔdV	↓	↓	2	↓	↓	↓	↓	↓	↓	↓	Jump to 14 if it is OK. ↓	V_2(dBV)		−61	−44	dBV
13-2			↓	↓	3	↓	↓	↓	↓	↓	↓	↓	Jump to 14 if it is OK. ↓	↓		−61	−44	dBV
13-3			↓	↓	1	↓	↓	↓	↓	↓	↓	↓	↓	↓		−61	−44	dBV
14	Output level difference 1	ΔV_{O1}	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	Calculate $\|Voe_1 - Vos_2\|$ ↓			0.2	1.2	dB
15	Output level difference 2	ΔV_{O2}	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	Calculate $\|Vom - Vos_1\|$ ↓			0	1.2	dB
16	PM output level	PmO	2	1	0	↓	↓	1	↓	↓	↓	↓	1kHz 0.1rad	V_3(dBV)	−49.2	−48.2	−47.3	dBV
17	PLL factor	Ko	↓	↓	↓	↓	↓	↓	2	↓	↓	↓	↓	V_3(dBV)	0.1 (−2.0)	0.13	0.18 (−6.5)	dB
18	OP AMP mid point	Vop	0	↓	↓	↓	↓	↓	1	↓	↓	↓	Non-modulation	V_5(V)	1.2	1.31	1.45	V
19	OP AMP gain	Opg	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	Input 400Hz 1mVrms from SG2 ↓	V_5(AC)	69	83		dB
20	Envelope noise	Vne	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	BW-400 to 15kHz ↓	V_2(dBV)		−84	−74	dBV
21	Main ch noise	Vnm	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	BW-400 to 15kHz ↓	V_2		−84		dBV
22	Sub ch noise	Vns	↓	↓	↓	↓	↓	2	↓	↓	↓	↓	BW-400 to 15kHz ↓	V_2(dBV)		−84	−74	dBV
23	Lock range 1*	Lcr_1	↓	↓	↓	↓	1	1	↓	↓	↓	2	SG1 449kHz 0.1Vrms ↓	I_1(mA)	4.9k	7k		Hz
24	Lock range 2*	Lcr_2	↓	↓	↓	↓	↓	↓	↓	1	2	↓	Vcc=1.9V SG1 449kHz 0.1Vrms ↓	I_2(mA)	2.9k	4.5k		Hz
25	Envelope output 2	ΔVoe	1	↓	↓	↓	↓	↓	↓	↓	↓	1	Vcc=12V → 1.9V 1kH 50%	V_2(dBV)	3.8	6.0	7.7	dBV
26	M→S cross talk 2	Cts2	↓	↓	↓	↓	↓	2	↓	↓	↓	↓	Vcc=1.9V ↓	V_2(dBV)		−60	−38	dBV
27	Sub ch output 2	ΔVos	↓	2	↓	↓	0	↓	↓	↓	↓	↓	Vcc=12V → 1.9V ↓	V_2(dBV)	3.3	5.0	7.2	dBV

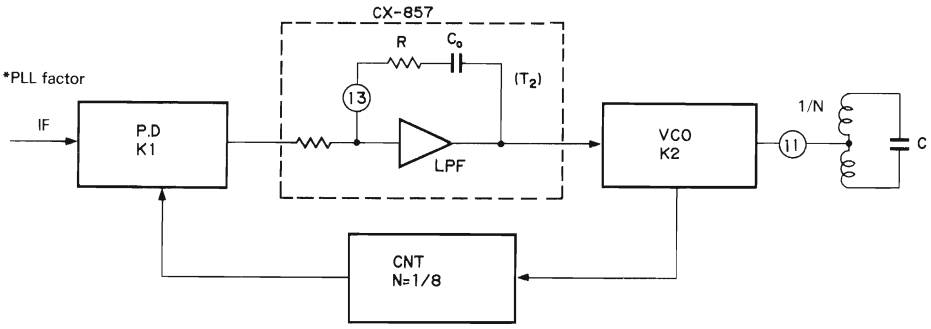
*See page 5.

SONY

Test Circuit



Phase Locking Loop (PLL) Equivalent Circuit



The diagram shown above may be interpreted as a PLL equivalent circuit of the CX-857. Here, the natural angle frequency WN and damping factor δ are

$$WN = \sqrt{\frac{NK_1K_2R}{\gamma_0 T_2}} \quad , \quad \delta = \frac{1}{2}\sqrt{\frac{NK_1K_2T_2}{\gamma_0}}$$

where VCO sensitivity K_2 is related to IF frequency (f_{IF}), coil tap ratio (N) and parallel capacitance (C) and the following is defined.

$$K_2 = Ko_2 \cdot gv$$

where VCO factor gv is shown as

$$gv = \frac{f_{IN}}{n^2 c} \times 10^{-15}$$

The lock range (Δf) is shown (using gv) as

$$\Delta f \fallingdotseq 4.5 \times gv \times 10^3 \quad [Hz]$$

and C and N can be determined from the required Δf.
Each factor can be combined to define the PLL factor K_0 as

$$K_0 = \frac{N K_1 Ko_2}{\gamma_0}$$

and this factor has its own IC property value.
When WN and δ are shown in Ko,

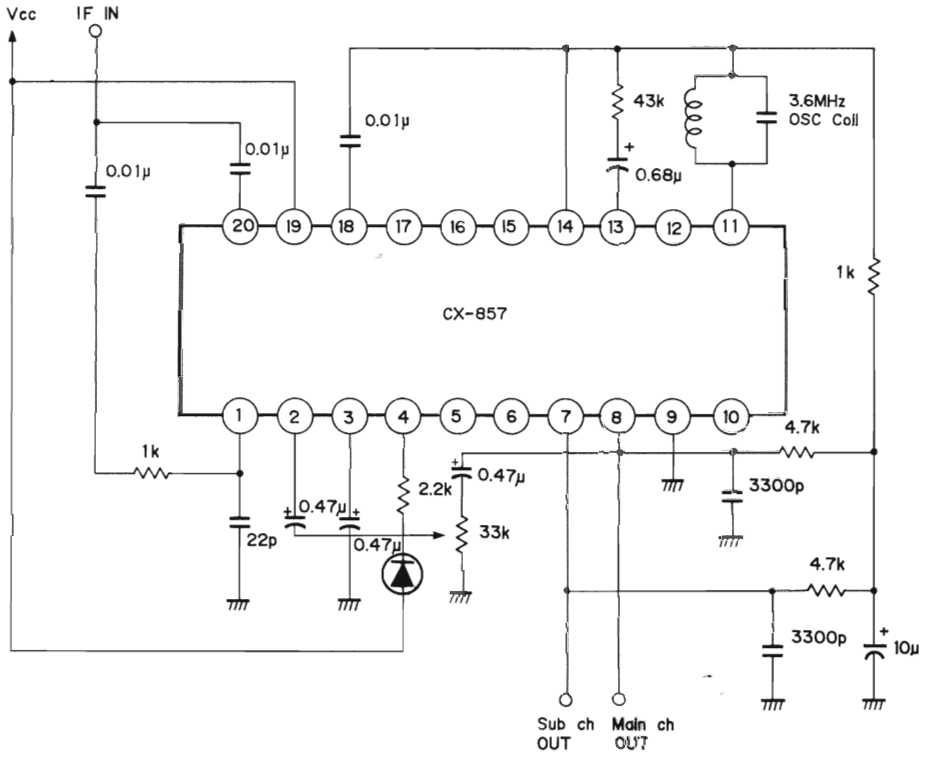
$$WN = \sqrt{\frac{Ko\ gv}{Co}} \qquad \delta = \frac{R}{2} \cdot \sqrt{Ko\ gv\ Co}$$

where

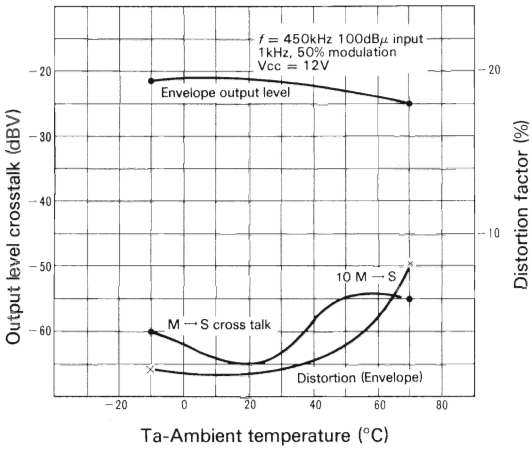
$$g_V = \frac{f_{IF}}{n^2 c} \times 10^{-15} \qquad Ko = 0.13 \text{ (Typ.)}$$

f_{IF} : IF frequency (Hz) N : coil tap ratio $\geqq 1$
C : VCO tank parallel capacitance (F)
Co : LPF Capacitance (F)
R : LPF resistor (Ω)

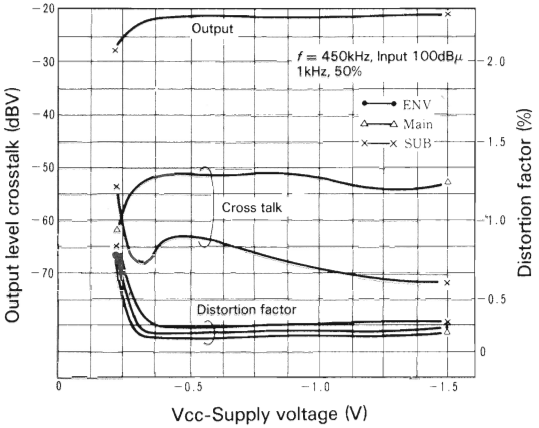
Application Circuit



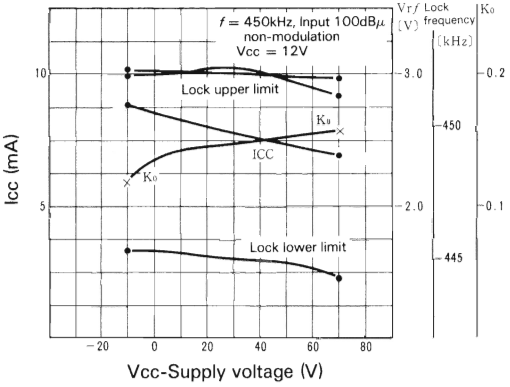
Output level crosstalk, distortion factor and Temperature characteristics



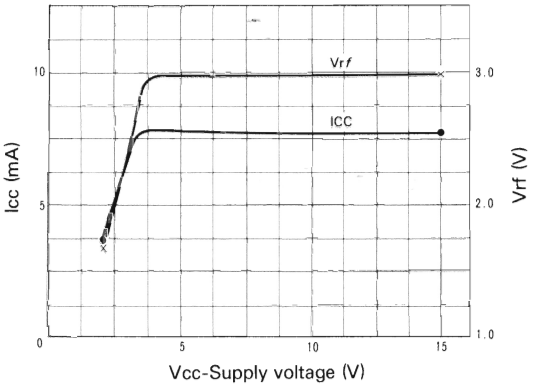
Output, distortion, crosstalk and supply voltage characteristics



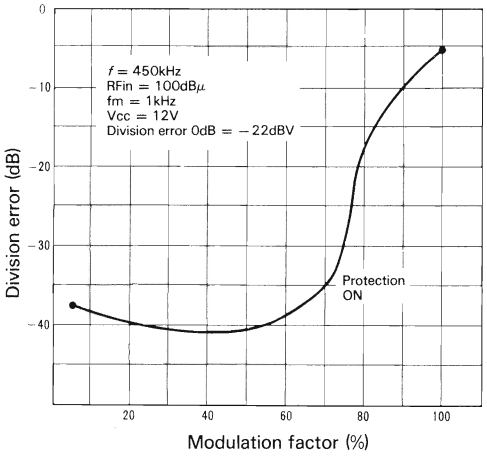
Supply current, reference voltage, lock range and PLL factor temperature characteristics



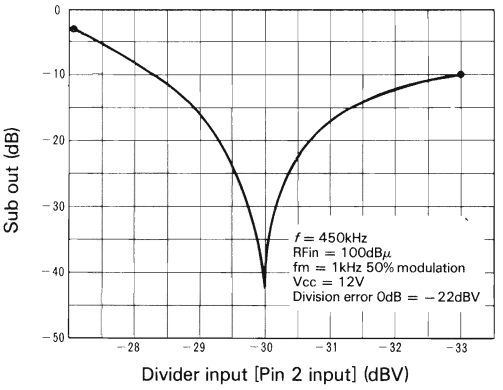
Current, reference voltage and supply voltage characteristics



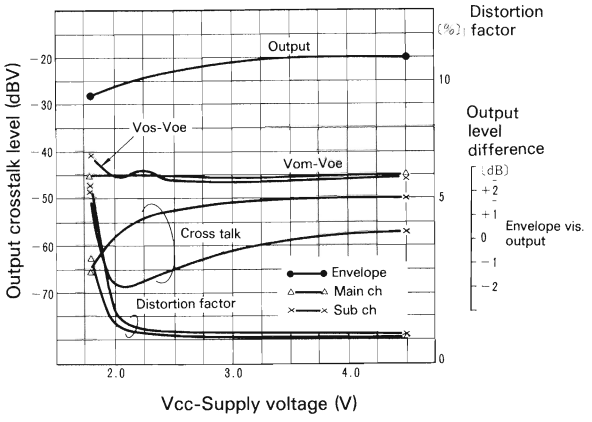
Divider characteristics (1)



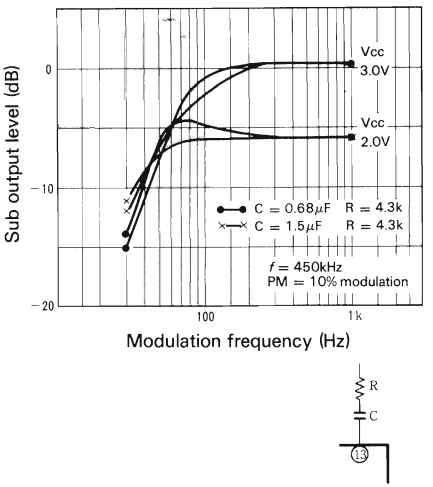
Divider characteristics (2)



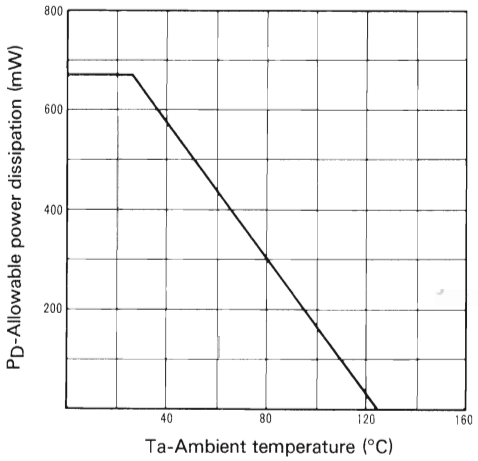
Output, distortion, cross talk and supply voltage characteristics (low voltage mode)



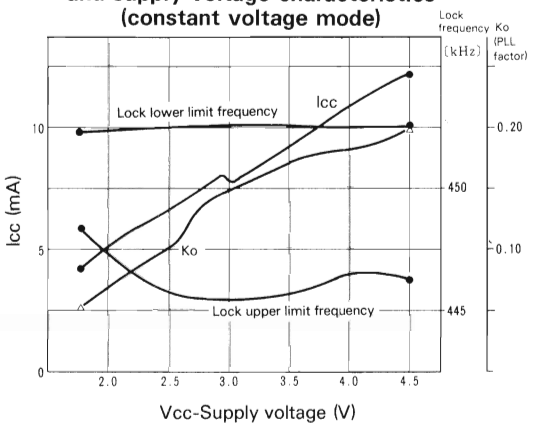
Sub channel frequency response



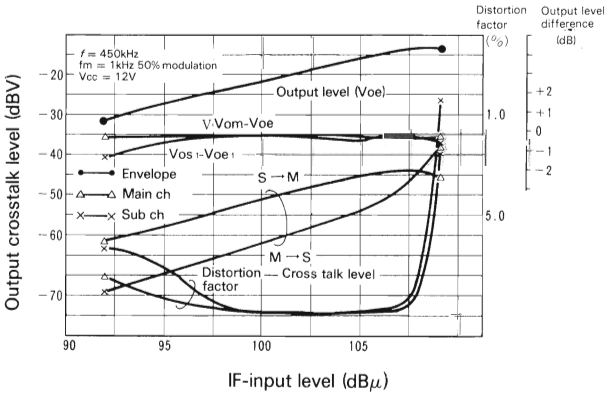
Derating curve



Circuit current, lock range, PLL factor and supply voltage characteristics (constant voltage mode)



IF I/O characteristics



SONY®

CX20029

FM/AM Stereo Radio

Description

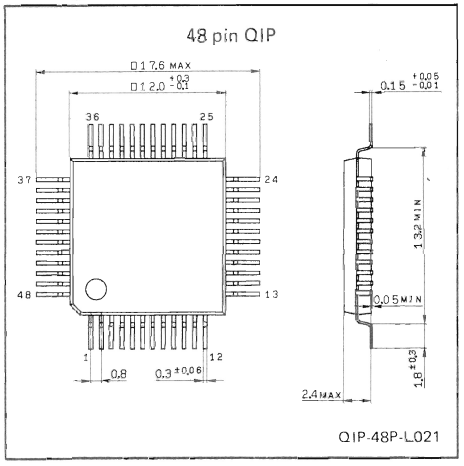
CX20029 is a high-performance one-chip bipolar IC specially designed for AM/FM stereo radios with an FM/AM front end, FM/AM IF AMP, FM/AM detection output, and FM stereo demodulator output.

Features

- Low current consumption.
  (In FM mode I_D=11.0 mA, in AM mode I_D=8.5 mA, V_{CC}=6.0V)
- LED drive circuit for tuning.
- LED drive circuit for stereo indicator.
- Muting circuit.
- Muting circuit for the FM band.
- Minimum external parts needed.

Package Outline

Unit: mm



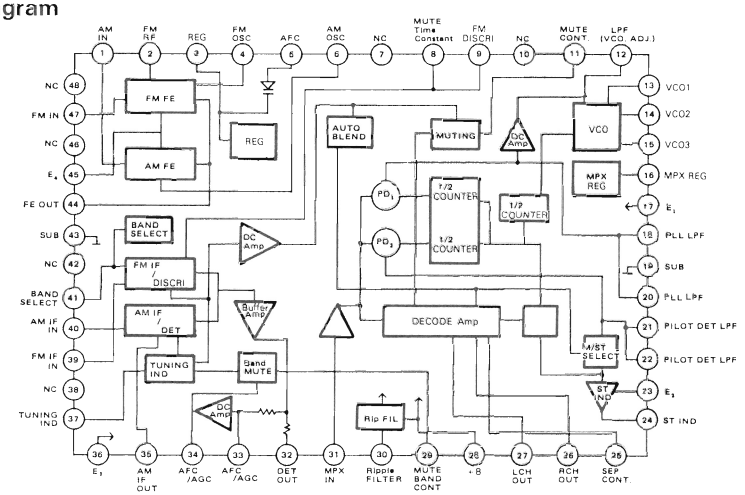
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	10	V
• Operating temperature	Topr	−15 to +60	°C
• Storage temperature	Tstg	−50 to +125	°C
• Junction temperature	Tjmax	125	°C
• Allowable power dissipation	P_D	833 (θja=120°C/W)	mW

Recommended Operating Condition

• Supply voltage	V_{CC}	2 to 9	V

Block Diagram



Electrical Characteristics (1)

(Ta=25°C)

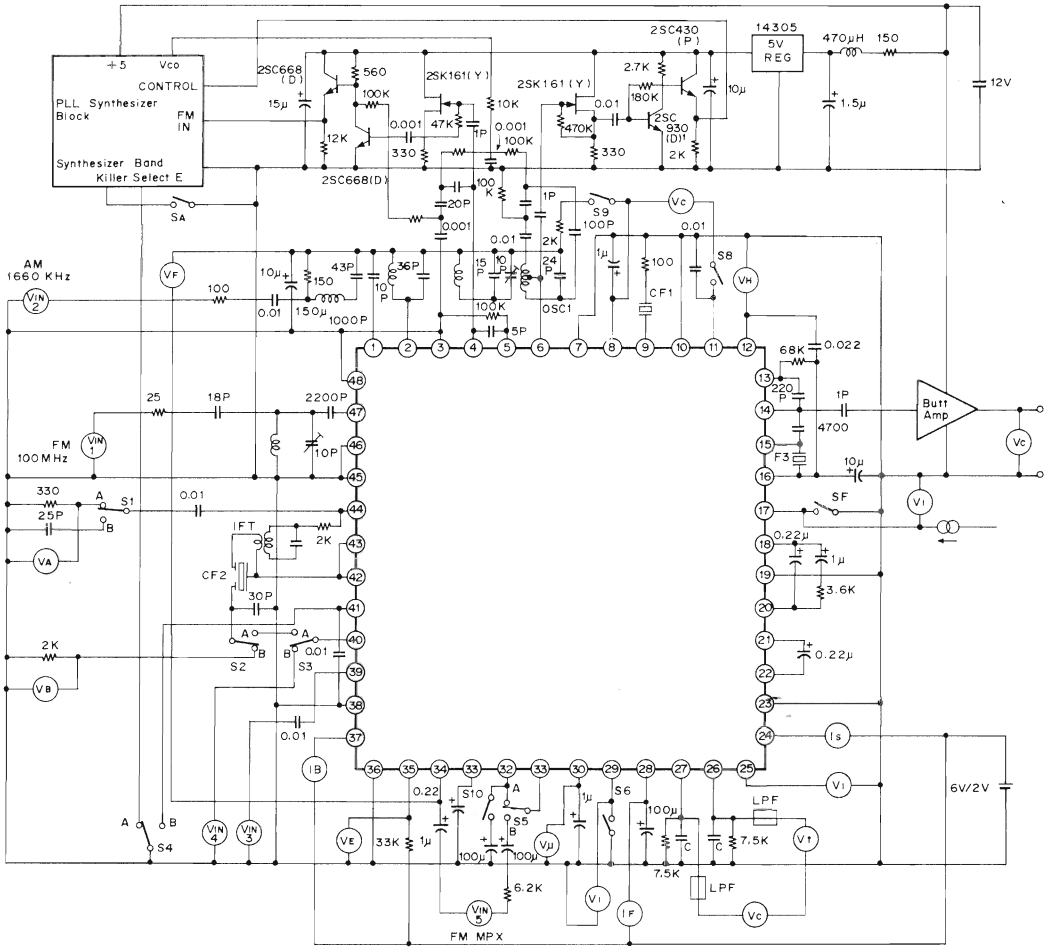
Item	Symbol	Switch Condition S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	Bias Condition V_{IN1}	V_{IN2}	V_{IN3}	V_{IN4}	V_{IN5}	Test Point	Output Waveform and Description of Test Method	Min.	Typ.	Max.	Unit
Circuit Current (1)	ID_1	A	B	B	B	B	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	I_D	During AM no signal \ V_1~V_4 input shorted	5.4	8.5	11.6	mA
Circuit Current (2)	ID_2	A	B	B	A	B	OFF	ON	ON	OFF	OFF						I_D	During FM no signal /	7.2	11.0	14.9	mA
VOC Oscillator Level	V_C	A	B	B	A	B	ON	ON	ON	OFF	ON						V_C	No signal 76kHz sine wave CW	225	300	385	mVrms
MPX VCO f deviation	$\Delta F2$	A	B	B	A	B	ON	ON	ON	ON	ON					↓	V_C	No signal. 76kHz sine wave CW (output level same as for VCO)	−110	0	+110	Hz
Separation	SEP	A	B	B	A	B	ON	ON	ON	ON	OFF					ON	$V_{D'}$ $V_{D'}$	V_{IN5}=−10dBs (MONO conversion) f=1kHz. Input STEREO L or R channel only and measure separation	39	70	−	dB
MPX S/N	VD4	A	B	B	A	B	ON	ON	ON	ON	ON					OFF	$V_{D'}$ $V_{D'}$	V_{IN5}: no signal. Noise is output in MONO mode.	−	−87.5	−79	dBs
	VD5	A	B	B	A	B	ON	ON	ON	ON	ON					ON	$V_{D'}$ $V_{D'}$	Noise is output in STEREO mode only with PILOT signal of V_{IN5}: 19kHz	−	−87.5	−79	dBs
MPX GAIN	GV5	A	B	B	A	B	ON	ON	ON	OFF	ON						$V_{D'}$ $V_{D'}$	V_{IN5}=−10dBs MONO 1kHz $V_{D'}$ $V_{D'}$: 1kHz sine wave	−2.0	−0.5	+1.5	dB
Channel Balance	GV6	A	B	B	A	B	ON	ON	ON	OFF	ON						$V_{D'}$ $V_{D'}$	V_{IN5}=−10dBs MONO 1kHz Output level ratio: Lch to Rch $V_{D'}$ $V_{D'}$: 1kHz sine wave	−1.5	0	+1.5	dB
MPX Distortion Factor	THD3	A	B	B	A	B	ON	ON	ON	OFF	ON						V_D, $V_{D'}$	V_{IN5}=−10dBs MONO 1kHz Lch, Rch: V_D, $V_{D'}$: 1kHz sine wave	−	0.015	0.11	%
	THD4	A	B	B	A	B	ON	ON	ON	ON	ON						$V_{D'}$ $V_{D'}$	V_{IN5}=−10dBs (MONO conversion) STEREO 1kHz Lch, Rch: $V_{D'}$ $V_{D'}$: 1kHz sine wave	−	0.015	0.11	%
FM MUTE	A1	A	B	B	A	B	ON	ON	ON	ON / OFF	ON						$V_{D'}$ $V_{D'}$	V_{IN5}=−10dBs MONO input 1kHz ATT Lch, Rch: V_{IN3}=no signal S9 ON/OFF $V_{D'}$ $V_{D'}$: 1kHz sine wave	16	23	30	dB
Attenuation during muting	A2	A	B	B	A	B	ON	ON	OFF	OFF	ON						$V_{D'}$ $V_{D'}$	V_{IN5}=−10dBs MONO 1kHz Output level of Lch, Rch: $V_{D'}$ $V_{D'}$ 1kHz sine wave	−	−79	−71	dBs
Noise during muting	VD6	A	B	B	A	B	ON	ON	ON / OFF	ON	ON					↓ OFF	$V_{D'}$ $V_{D'}$	No signal. DC voltage difference between terminal 26 and 27 for Lch and Rch	-66	0	+66	mV
STEREO Indicator Output	I_S	A	B	B	A	B	ON	ON	ON	ON	ON					ON	I_S	V_{IN5}=−10dBs STEREO 1kHz (MONO conversion)	1.8	3.0	4.4	mA
STEREO/ MONO Select Level	VM1	A	B	B	A	B	ON	ON	ON	ON	ON						I_S	MONO → STEREO (when I_S is ON) V_{IN5} PILOT signal (f=19kHz) only	−42	−38	−35	dBs
																↓					Becomes STEREO	
STEREO/ MONO Select Level	YM2	A	B	B	A	B	ON	ON	ON	ON	ON					ON	I_S	STEREO → MONO (when I_S is OFF) V_{IN5} PILOT signal (f=19kHz) only	−44	−40	−37	dBs
												↓							Becomes MONO			
FM Front End Voltage Gain (1)	GV1	A	B	B	A	B	OFF	ON	ON	OFF	OFF	ON				OFF	V_A	V_{IN1} = 40dBμV 100mHz CW V_A = 10.7mHz CW	29	35	41	dB

Electrical Characteristics (2)

(Ta=25°C)

Item	Symbol	Switch Condition S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	Bias Condition V_{IN1}	V_{IN2}	V_{IN3}	V_{IN4}	V_{IN5}	Test Point	Output Waveform and Description of Test Method	Min.	Typ.	Max.	Unit
FM Detection Output Level	VD_1	A	B	B	A	A	ON	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	V_D	V_{IN3} = 90dBμV 10.7MHz 1kHz 30% MOD V_D = 1kHz sine wave	−24	−20	−16	dBs
FM IF Knee Level	VD_2	A	B	B	A	A	ON	ON	ON	ON	OFF						V_{IN3}	Input level −3dB down on output of V_{IN3} =90dBμV 10.7MHz 1kHz; 30% MOD	−	25	31	dBμ
FM IF Distortion Factor (1)	THD_1	A	B	B	A	A	ON	ON	ON	OFF	OFF						V_D	V_{IN3}=90dBμV 10.7MHz 1kHz 100% MOD V_D=1kHz sine wave	−	0.1	1.1	%
FM IF Center Frequency Deviation	ΔF_1	A	B	B	A	A	ON	ON	ON	OFF	OFF						V_F	V_{IN3}=90dBμV 10.7MHz CW Voltage between terminal 3 and 34 (Regulated by DC voltage at ±50kHz)	−33	0	33	kHz
FM Meter Current (1)	IB_1	A	B	B	A	B	ON	ON	ON	ON	OFF					↓	I_B	V_{IN3}=60dBμV 10.7MHz CW	1.8	3.5	6.1	mA
M/ST Select Level for IF Input	VI_1	A	B	B	A	B	ON	ON	ON	OFF	ON					ON	I_S	Check that I_S current when V_{IN3}: f=10.7MHz CW is input at 48dBμV and that I_S does not current when 35dBμV is input in the V_{IN5}=−10 dBs 1kHz stereo input state (I_S regulates the leakage current)	M→ST 38	43	48	dBμV
																			ST→M 33	41	46	dBμV
Auto Blend	VI_2	A	B	B	A	B	ON	ON	ON	OFF	ON						V_{IN3}	V_{IN5}=−10dBs 1kHz Stereo V_{IN3} f = 10.7MHz L and Rch separation when 50dBμV is input For samples over 40dB, L and R ch separation is measured at V_{IN3}=48dBμV.	1	10	41	dB
Mute Band	B_1	A	B	B	A	B	ON	ON	ON	OFF	ON					OFF	I_B	V_{IN3}=90dBV Check DC voltage of terminal 29, then check if muted after increasing to more than f=10.7MHz ±170kHz (when MUTE ON→I_B does not current)	±63	±100	±154	kHz
AM Front End Voltage Gain (2)	GV_2	B	B	B	B	B	OFF	ON	ON	OFF	OFF		ON	OFF			V_B	V_{IN2}=60dBμV 1660kHz CW V_B: 455kHz CW	19	24	28	dB
AM IF Voltage Gain (4)	GV_3	A	B	B	B	A	OFF	ON	ON	OFF	OFF		OFF		ON		V_{IN4}	V_{CC} = 6V Level of V_{IN4} when output is -34dBs	15	21	26	dB
AM IF Voltage Gain (3)	GV_4	A	B	B	B	A	OFF	ON	ON	OFF	OFF		OFF		ON		V_{IN4}	Level of V_{IN4} with V_{CC} = 2V (regulated by level difference for V_{CC}=6V), V_{IN4}=455kHz (1kHz 30 x MOD), and output is −40dBs V_D = 1kHz sine wave	−3.5	0	+2.5	dB
AM Detection Output Level	VD_3	A	B	B	B	A	OFF	ON	ON	OFF	OFF						V_D	V_{IN4}=85dBμV 455kHz (1kHz 30% MOD) V_D = 1kHz sine wave	−24	−20	−16	dB
AM Meter Current (2)	IB_2	A	B	B	B	B	ON	ON	ON	OFF	OFF						I_B	V_{IN4} = 85dBμV 455kHz CW	1.6	3.0	5.5	mA
AM IF Output Output Level	V_E	A	B	B	B	A	OFF	ON	ON	OFF	OFF						V_E	V_{IN4} 85dBμV 455kHz CW Output Pin 35 455kHz	81	100	121	mV
AM Detection Output Level (2)	THD_2	B	A	A	B	A	OFF	ON	ON	OFF	OFF		ON			OFF	V_D	V_{IN2} = 95dBμV 1660kHz (1kHz 30% MOD) V_D = 1kHz sine wave	−	0.6	1.1	%

Electrical Characteristic Test Circuit



Output Levels of $V_{IN}1$ to 4 are for S · G output pin open circuited

$V_{IN}5$ is the output pin level when terminated in 600Ω

CF1: FM discriminator
CF2: AM:IF. CF
IFT: AM 4.55kHz IFT
OSC: AMOSC
CF3: 76 kHz Ceramic Lock

C deemphasis time constant: 0.01 μF when 75 μs.
0.0063 μF when 50 μs.

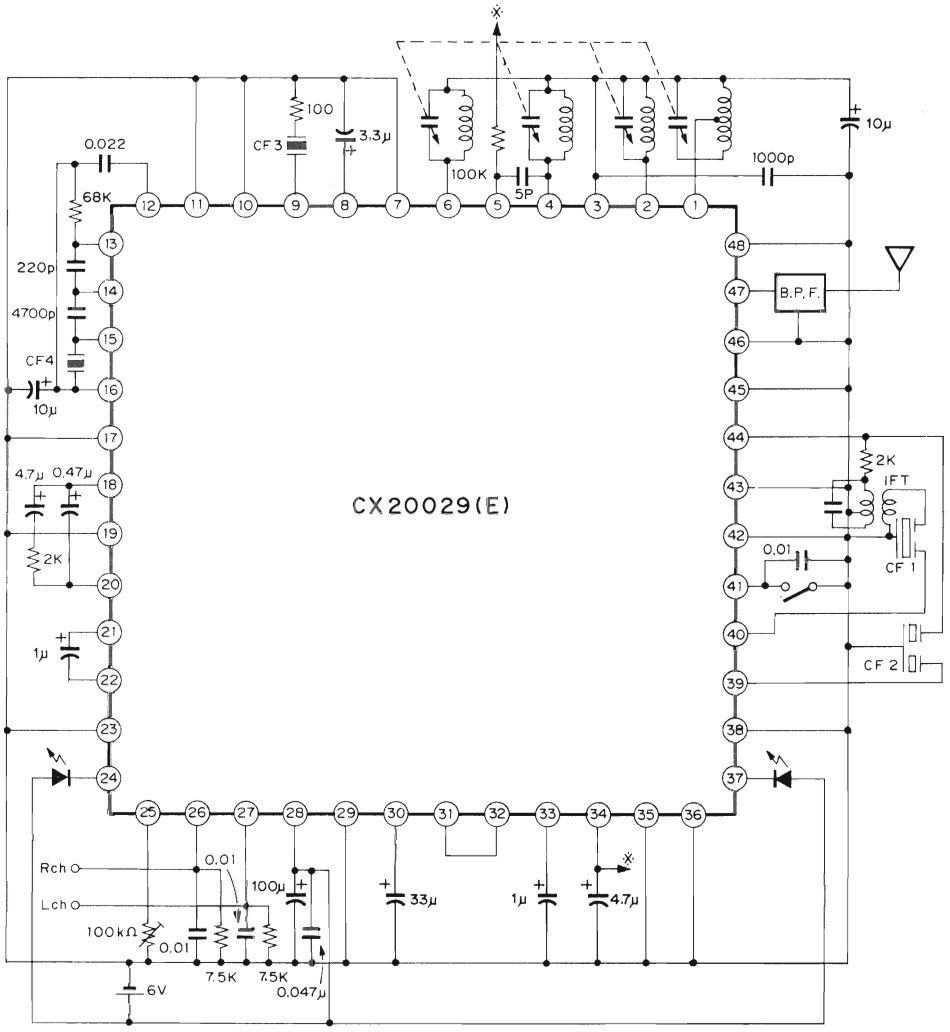
Standard Circuit Design Data

- Pin Voltage (Ta=25°C)

Note) The voltages of the pin when the power voltage is 3V are for a load resistance at the MPX output (pin 26 and 27) of 3.3 KΩ.

No.	3 V		6 V		No.	3 V		6 V	
	FM	AM	FM	AM		FM	AM	FM	AM
1	1.25	1.25	1.25	1.25	25	0.35	0.35	0.35	0.35
2	1.25	1.25	1.25	1.25	26	0.66	0.66	1.5	1.5
3	1.25	1.25	1.25	1.25	27	0.66	0.66	1.5	1.5
4	1.25	1.25	1.25	1.25	28	3.0 (V_{CC})	3.0 (V_{CC})	6.0 (V_{CC})	6. (V_{CC})
5	1.15	1.47	1.15	1.47	29	0	0	0	0
6	1.25	1.25	1.25	1.25	30	2.7	2.7	4.0	4.0
7	0	0	0	0	31	1.0	1.0	1.0	1.0
8	0.05	0.01	0.05	0.01	32	1.0	1.0	1.0	1.0
9	2.18	2.70	3.08	3.60	33	1.47	1.15	1.47	1.15
10	0	0	0	0	34	1.15	1.47	1.15	1.47
11	0	0	0	0	35	0	0	0	0
12	1.0	1.0	1.0	1.0	36	0 (GND)	0 GND)	0 (GND)	0 (GND)
13	1.0	1.0	1.0	1.0	37	1.6	1.6	4.5	4.5
14	1.0	0.6	1.0	0.6	38	0	0	0	0
15	1.65	0	1.65	0	39	1.25	0	1.25	0
16	1.65	1.65	1.65	1.65	40	0	0	0	0
17	0 (GND)	0 (GND)	0 (GND)	0 (GND)	41	1.25	0	1.25	0
18	0.95	0.95	0.95	0.95	42	0	0	0	0
19	0 (GND)	0 (GND)	0 (GND)	0 (GND)	43	0 (GND)	0 (GND)	0 (GND)	0 (GND)
20	0.95	0.95	0.95	0.95	44	0.57	0.2	0.8	0.2
21	0.95	0.95	0.95	0.95	45	0 (GND)	0 (GND)	0 (GND)	0 (GND)
22	0.95	0.95	0.95	0.95	46	0	0	0	0
23	0 (GND)	0 (GND)	0 (GND)	0 (GND)	47	0.3	0	0.3	0
24	1.6	1.6	4.5	4.5	48	0	0	0	0

Standard Circuit Design Data (DC Filter)



Example of Circuit to Test Standard Circuit Design Data

(FM Mode)

Change the MPX output load resistance to 3.3 kΩ when the power voltage is lower than 3 V.

BPF:FM	BAND PASS FILTER
CF1:AM	455 kHz C.F
CF2:FM	10.7 MHz CF
CF3:FM	10.7 MHz Discriminator
CF4:	76 kHz Ceramic Lock
IFT:AM	455 kHz IFT

FM/AM Radio Circuit

Description

CX20090/CX20091 is a high-performance one-chip bipolar IC designed to integrate all the required functions, for FM/AM radios.

Futures

- From front end to audio final stage, contains all functions.
- Minimum supply voltage is 1.8V.
- Low current consumption.
  (In FM mode: I_D=5.3 mA, in AM mode: I_D=3.4 mA, V_{CC}=3V)
- LED drive circuit for tuning.
- Electronic volume control.
- Minimum external components.
- Large output (V_{CC}=6V 8Ω load, EIAJ output= 500 mW)

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	9	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−50 to +125	°C
• Junction temperature	Tj	125	°C
• Allowable power dissipation	P_D	1160 (CX20090)	mW
		800 (CX20091)	mW

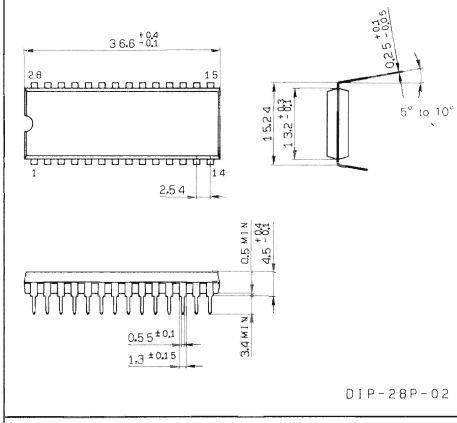
Recommended Operating Conditions

• Supply voltage	V_{CC}	2 to 8.5 (CX20090)	V
		2 to 7.5 (CX20091)	V

Package Outline

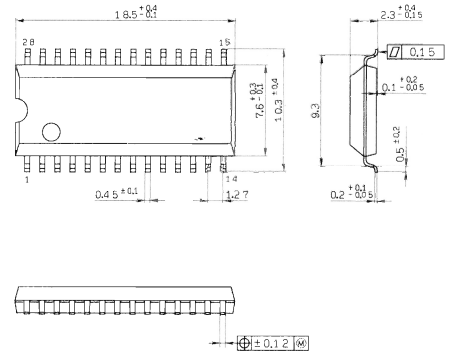
Unit: mm

CX20090 28 pin DIP



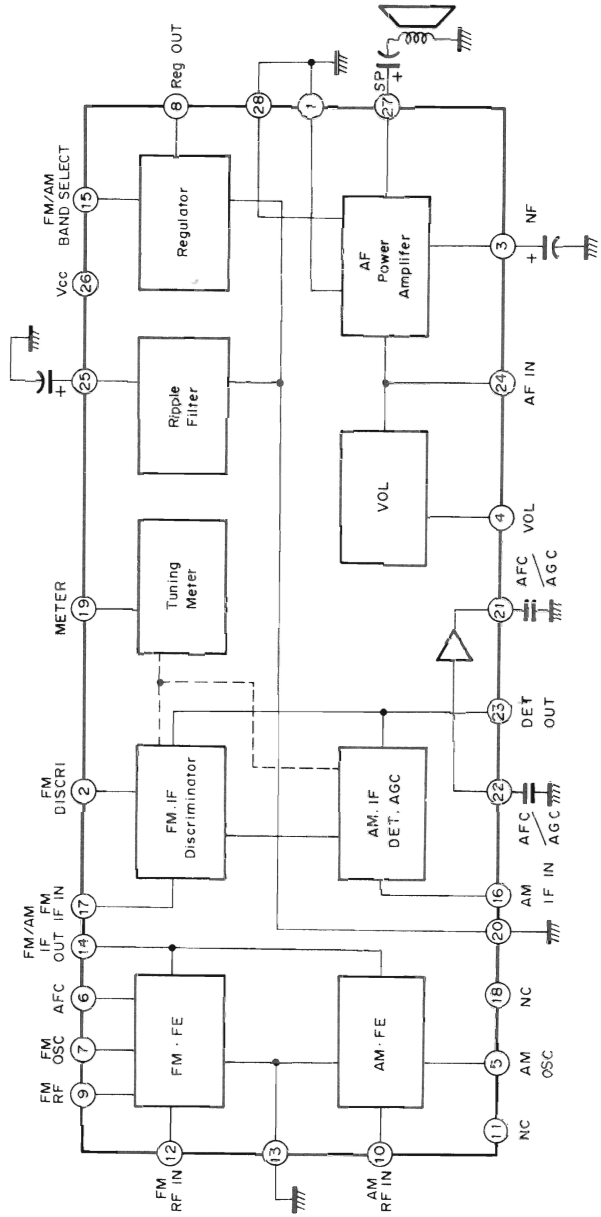
DIP-28P-02

CX20091 28 pin MFP



MFP-28P-L03

Block Diagram

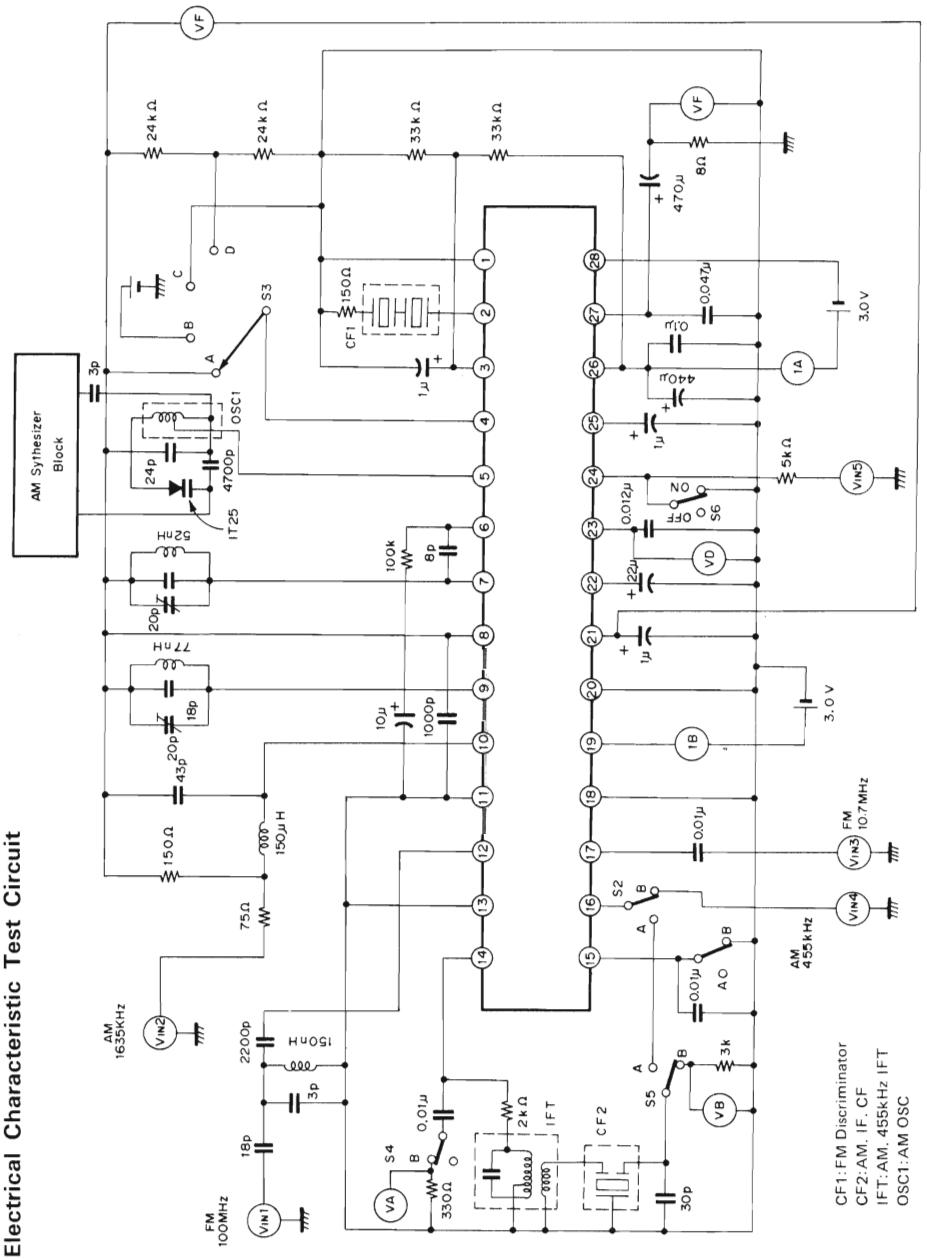


Electrical Characteristics

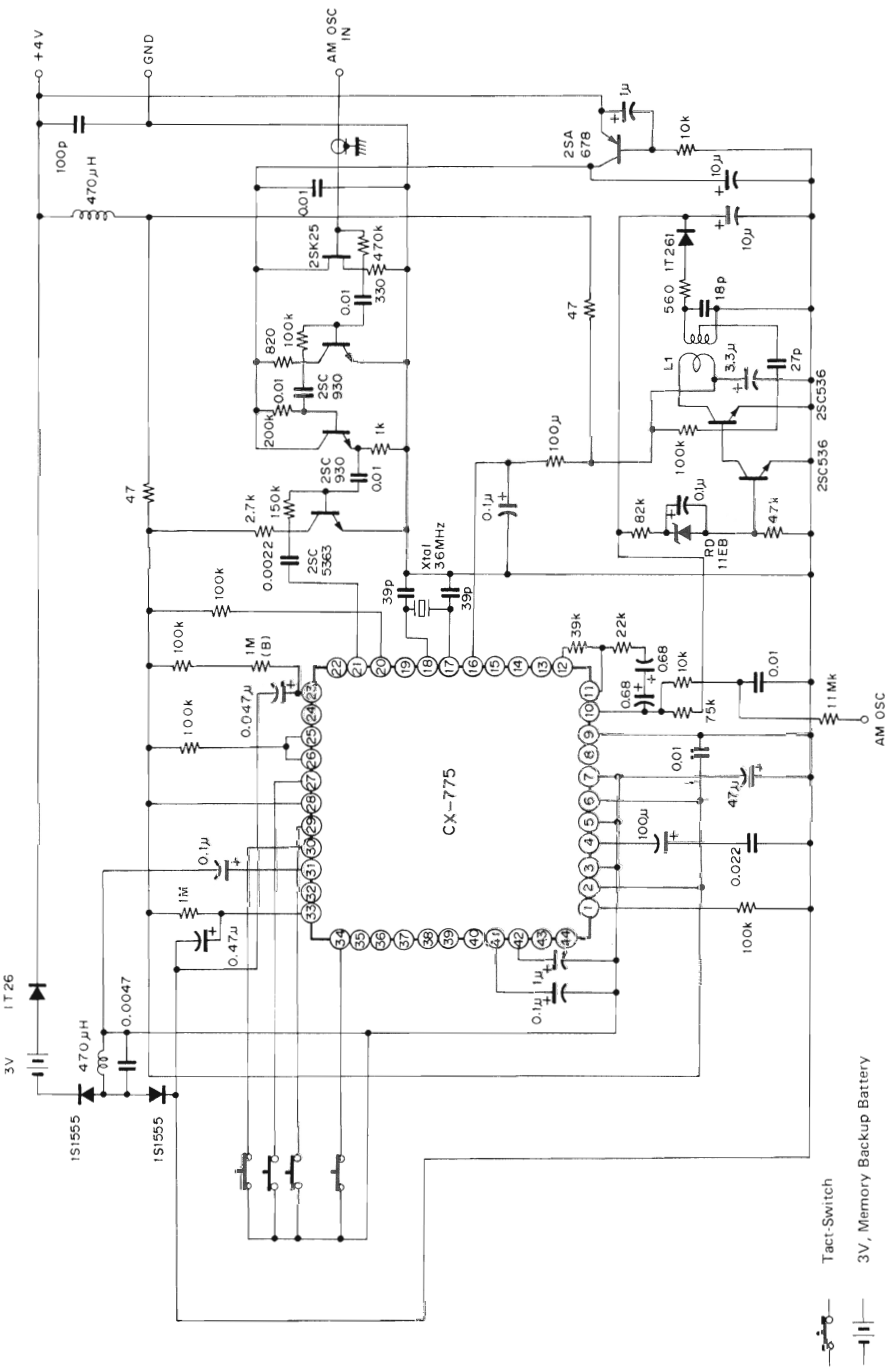
(Ta=25°C, V_{CC}=6V)

Characteristic	Symbol	SW Status						Test Point	Condition	Min.	Typ.	Max.	Unit
Circuit Current (1)	ID1	B	B	A	B	B	ON	IA	No signal, AM	1.8	3.5	7.15	mA
Circuit Current (2)	ID2	A	B	A	B	B	ON	IA	No signal, FM	4.1	7.0	10.5	mA
FM Front End Voltage Gain (1)	GV1	A	B	A	B	B	ON	VA	$V_{IN}1$=40dBu, 100MHz	33	39	45	dB
FM Detection Output Level	VD1	A	B	A	B	B	ON	VD	$V_{IN}3$=90dBu, 10.7MHz (1kHz, 22.5kDEV)	−25.5	−20	−15.5	dBs
FM Detection Output Level (2)	ΔVD	A	B	A	B	B	ON	VD	$V_{IN}3$=90dBu, 10.7MHz (1kHz, 22.5kDEV Level difference between V_{CC}=9.0V and VD1)	−3.5	0	3.5	dB
FM IF Knee Level	VD2	A	B	A	B	B	ON	VD	$V_{IN}3$ level at a point 3dB down from $V_{IN}3$=90dBμV, 10.7MHz (1kHz, 22.5kDEV)	–	24	31	dBu
FM Detection Output Distortion Factor (1)	THD1	A	B	A	B	B	ON	VD	$V_{IN}3$=90dBu, 10.7MHz (1kHz, 75kHz DEV)	–	0.3	1.1	%
FM IF Center Frequency Deviation	F	A	B	A	B	B	ON	VF	Frequency at which voltage between $V_{IN}3$=90dBμV and 10.7MHz unmodulated terminals 8 and 21 becomes 0V.	−55	0	55	kHz
FM Meter Current (1)	IB1	A	B	A	B	B	ON	IB	$V_{IN}3$=60dBu, 10.7MHz	1.8	3.5	6.1	mA
AM Front End Voltage Gain (2)	CV2	B	B	A	A	B	ON	VB	$V_{IN}2$=60dBu, 1635kHz	16	22	28	dB
AM IF Voltage Gain (3)	CV3	B	B	A	A	B	ON	VD	Level of $V_{IN}4$ when 455kHz (1kHz 30% MOD) output is −34dBm.	15	20	26	dBu
AM Detection Output Level (3)	VD3	B	B	A	A	B	ON	VD	$V_{IN}4$=85dBu, 455kHz (1kHz 30% MOD)	−25	−20	−15	dBs
AM Meter Current (2)	IB2	B	B	A	A	B	ON	IB	$V_{IN}4$=85dBu, 455kHz (1kHz 30% MOD)	1.35	3.0	5.5	mA
AM Detection Output Level (2)	THD2	B	A	A	A	A	ON	VD	$V_{IN}2$=95dBu, 1635kHz (1kHz, 30% MOD) cc=7.8V	–	0.6	1.1	%
Audio Voltage Gain (3)	GV4	B	A	C	A	A	OFF	VE	$V_{IN}5$=−30dBm, 1kHz	27.5	31.5	35.5	dB
Attenuation (1)	AT1	B	A	D	A	A	OFF	VE	Output level difference between $V_{IN}5$=−30dBm, 1kHz VOL MAX and center	11	24.5	38	dB
Attenuation (2)	AT2	B	A	A	A	A	OFF	VE	$V_{IN}5$=−10dBm, 1kHz	–	−76	−69	dBs
EIAJ Output	VE	B	A	B	A	A	OFF	VE	$V_{IN}5$=−20dBm, 1kHz, R_L=8Ω	410	540	–	mW
Audio Distortion Factor (3)	THD3	B	A	B	A	A	OFF	VE	Distortion factor for output of 50mW $V_{IN}5$=20dBm, 1kHz	–	0.3	0.2	%
Residual Noise	N	B	A	C	A	A	ON	VE	$V_{IN}5$=CND	–	−64	−57	dBs

Electrical Characteristic Test Circuit



AM Synthesizer Circuit (Top View)



Standard Circuit Design Data

Pin Voltage (Ta=25°C)

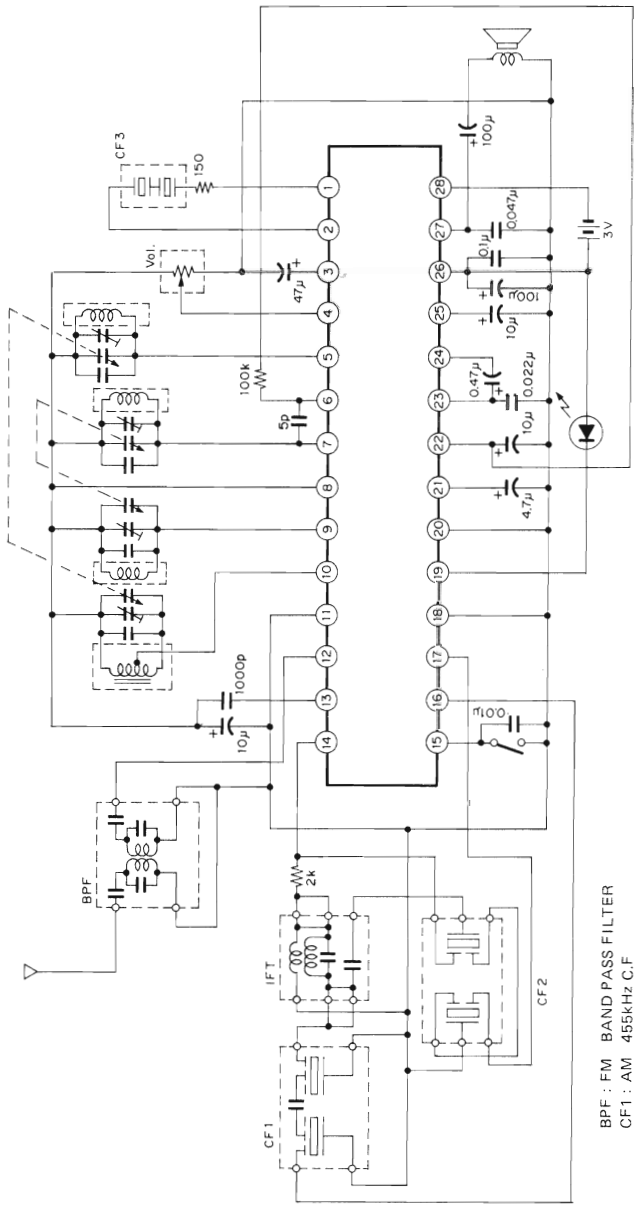
No.	3V		6V		No.	3V		6V	
	FM	AM	FM	AM		FM	AM	FM	AM
1	0	0	0	0	15	0.84	0	0.88	0
2	2.18	2.70	4.88	5.43	16	0	0	0	0
3	1.5	1.5	3.0	3.0	17	0.84	0	0.88	0
4	1.25	1.25	1.25	1.25	18	0	0	0	0
5	1.25	1.25	1.25	1.25	19	1.6	1.6	4.5	4.5
6	1.25	*	1.25	*	20	0	0	0	0
7	1.25	1.25	1.25	1.25	21	1.25	1.49	1.25	1.49
8	1.25	1.25	1.25	1.25	22	1.25	1.12	1.25	1.12
9	1.25	1.25	1.25	1.25	23	1.25	1.0	1.25	1.0
10	1.25	1.25	1.25	1.25	24	0	0	0	0
11	0	0	0	0	25	2.71	2.71	5.4	5.4
12	0.3	0	0.3	0	26	3.0	3.0	6.0	6.0
13	0	0	0	0	27	1.5	1.5	3.0	3.0
14	0.36	0.2	0.36	0.2	28	0	0	0	0

Note) 1. All values are standard values (based on the circuit shown in Fig. 3).

2. Test is made in the on signal state and at minimum volume in the condition in Fig. 3 (Pin 19 is the voltage with LED mounted).

* The voltage on Pin 6 in the AM mode is the same as that on Pin 22 in the J band and on Pin 21 in the W band.

Standard Circuit Design Data Test Circuit (FM Mode)



BPF : FM BAND PASS FILTER
CF1 : AM 455kHz C.F
CF2 : FM 10.7k
CF2 : FM 10.7MHz C.F
CF3 : FM 10.7MHz Discriminator
IFT : AM 455kHz LFT

Fig. 3

FM/AM Radio

Description

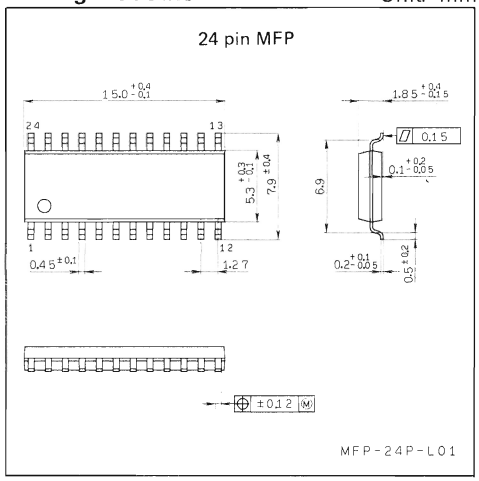
The CX20111 is an IC designed for use in FM/AM radios, integrating all necessary functions from the front end detector stage of a radio.

Features

- Wide application range as it contains functions from the front end to detector stage.
- Operable for a wide range of power supply voltages.(V_{CC}; 2 to 9V)
- Low current consumption. (For FM, I_{DD}=6.0 mA, for AM, I_{DD}=4.0 mA, at V_{CC}=6V)
- Self-contained LED drive circuit for tuning.
- Self-contained FM band signal output circuit.
- Variable capacitance diode for FM AFC.
- Low distortion factor (0.1% typ.) for FM detection output.
- AM IF output pin which can be adapted for the AM stereo.
- Needs few peripheral parts. Due to its small size, a high density packaging design is possible.

Package Outline

Unit: mm



Structure

Bipolar silicon monolithic IC

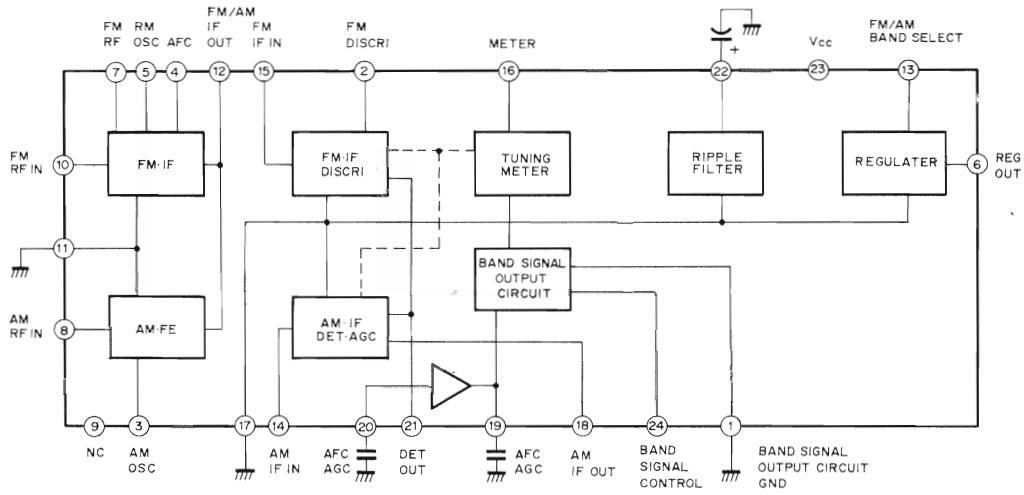
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	10	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	670	mW

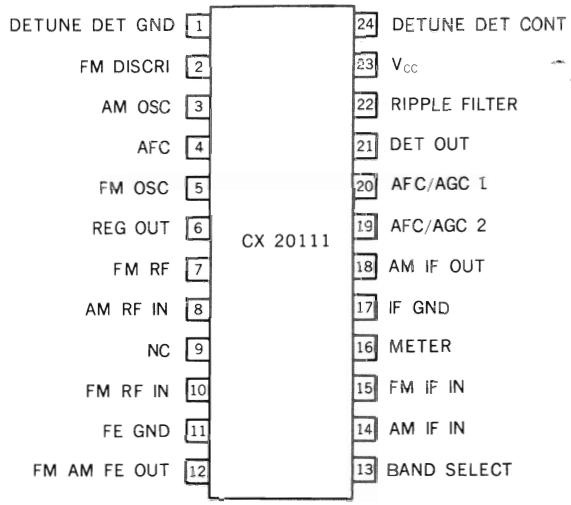
Recommended Operating Condition

• Supply voltage	V_{CC}	2 to 9	V

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	Description
1	GND	Ground for band signal output
2	FM DISCRI	Discriminator pin; to be connected to FM discriminator
3	AM OSC	AM local oscillator circuit
4	AFC	AFC input pin
5	FM OSC	FM local oscillator
6	REG OUT	Regulator; 1.25V (typ.)
7	FM RF	FM RF input; connected to RF tank circuit
8	AM RF IN	AM RF input; connected to BAR ANT
9	NC	
10	FM RF IN	FM RF amplifier circuit; FM RF input
11	GND	Ground for front end
12	FM/AM FE OUT	IF output circuit for AM and FM; connected to AM and FM IF filiters
13	BAND SELECT	Pin of FM and AM band switch; AM for "GND" and FM for "OPEN"
14	AM IF IN	Input stage of AM IF
15	FM IF IN	The first stage of FM IF amplifier circuit
16	METER	Meter drive circuit
17	IF GND	AM/FM IF stage; ground for detector stage
18	AM IF OUT	AM IF output; emitter output
19	AFC/AGC 2	AFC pin for W band; to adjust the time constant (using a capacitor of external circuit) with AM
20	AFC/AGC 1	AFC pin for J band; to adjust the time constant (using a capacitor in external circuit) with AM
21	DET OUT	Pin of detector output; impedence; approx. 5kΩ
22	RIPPLE	The ripple filter: the hum supression level of approx. 34.5 dB can be obtained by connecting a 10 μF capacitor
23	Vcc	IC power supply
24	BAND SIGNAL OUTPUT CONTROL	Band signal output amplitude is adjusted by connecting an outside resistor

Electrical Characteristics

(Ta=25°C, See the Electrical Characteristics Test Circuit)

No.	Test Item	Symbol	Switch Position									Bias Condition				Test point	Output Waveform and Method of Test	Min.	Typ.	Max.	Unit
			S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_{IN1}	V_{IN2}	V_{IN3}	V_{IN4}						
1.	Circuit current (1)	ID_1	OFF	B	OFF	B	B	A	A	ON	OFF	OFF	OFF	OFF	OFF	I_D	Short circuit V_{IN1} through V_{IN4} when either AM signal of FM signal is not present	1.8	4.0	6.6	mA
2.	Circuit current (2)	ID_2	↓	↓				B				↓				I_D		3.6	6.0	8.25	mA
3.	FM front end voltage gain(1)	GV_1	ON	A								ON			↓	V_D	V_{IN1}=100MHz 40dBμV CW V_A=10.7MHz CW	33	39	45	dB
4.	FM detector output level (1)	VD_1	OFF	B								OFF		ON	ON	V_D	V_{IN3}=10.7MHz 90dBμV 1KHz 22.5KHz dev V_D=1KHz sin Wave	−25.2	−22.5	−19.0	dBs
5.	FM detector output level (2)	ΔVD														V_D	V_{D1} and V_{CC}=9V; level difference with same value of V_{D1}	−4.0	−	+4.0	dB
6.	FM IF knee level	VD_2														V_{IN3}	V_{IN3} level is −3dB with reference to V_{D1}	−	25	31	dBμ
7.	FM detector output distortion factor (1)	THD_1														V_D	V_{IN3}=10.7MHz 90dBμV 1KHz 75KHz dev V_D=1KHz sin Wave	−	0.1	1.1	%
8.	Deviation of FM IF center frequency	F_1														−	V_{IN3}=10.7MHz 90dBμV CW	−55	0	55	kHz
9.	FM meter current (1)	IB_1									↓					I_B	V_{IN3}=10.7MHz 60 dBμV CW	1.8	3.5	6.05	mA
10.	FM band signal output band width	F_2	↓		↓			↓			ON		↓	↓	↓	I_B	V_{IN3}=10.7MHz 235KHz Confirm I_B=0 at 90dBμV	±67.5	±110	±170.5	kHz
11.	AM front end voltage gain (2)	GV_2	ON		ON		↓	A			OFF		ON	OFF	OFF	V_B	V_{IN2}=1660KHz 60dBμV CW V_B=455KH CW	19	24	28	dB
12.	AM IF voltage gain (3)	GV_3	OFF		OFF		OFF						OFF		ON	V_{IN4}	Level of V_{IN4} at V_D=−34dBS	17	23	28	dBμ
13.	AM IF voltage gain (4)	ΔGV														V_{IN4}	V_{CC}=2V; level difference with same condition as GV_3	−4	0	3	dB
14.	AM detector output level (3)	VD_3														V_D	V_{IN4}=455KHz 85dBμV 1KHz 30% MOD V_D=1KHz sin Wave	−25.5	−22.5	−19.0	dBs
15.	AM meter current (2)	IB_2							↓							I_B	V_{IN4}=455KHz 85dBμV CW	1.62	3.0	5.5	mA
16.	AM IF output level	V_E	↓			↓			B				↓		↓	V_E	V_{IN4}=455KHz 85dBμV CW V_E=455KHz CW	72	100	132	mV
17.	AM detector output distortion factor (2)	THD_2	ON	↓	↓	A	↓	↓	A	↓	↓	↓	ON	↓	OFF	V_D	V_{IN2}=95dBμV 1660KHz 1KHz 30% MOD, V_D=1KHz sin Wave V_{CC}=7.8V	−	0.6	1.1	%

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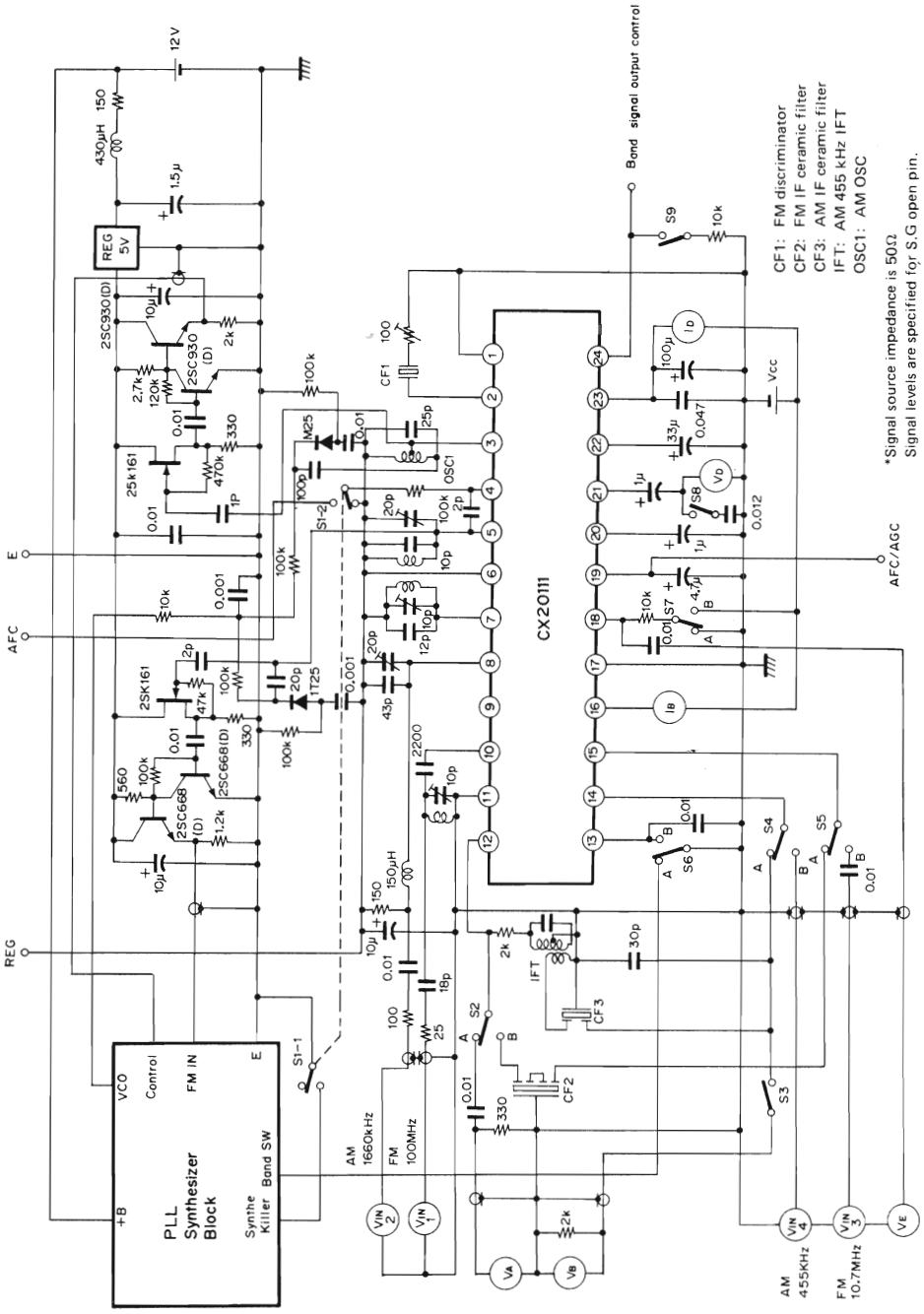
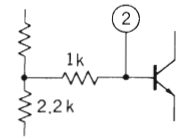
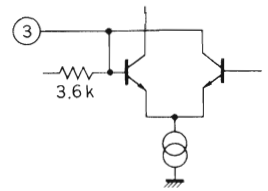
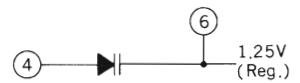
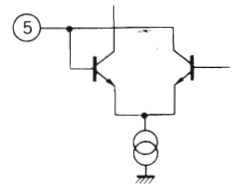
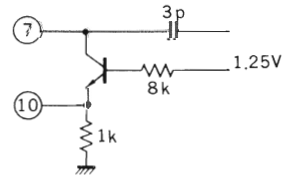
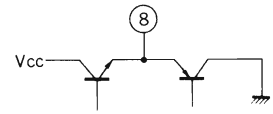
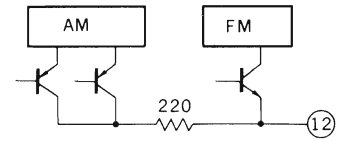
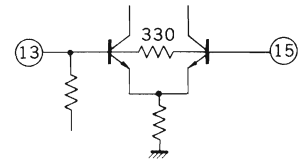
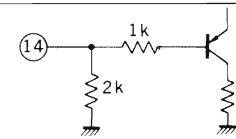
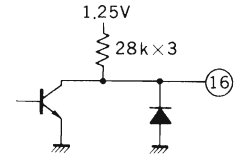
Electrical Characteristics Test Circuit

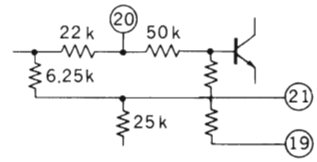
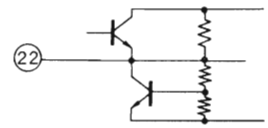
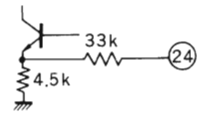


Standard Circuit Design Data

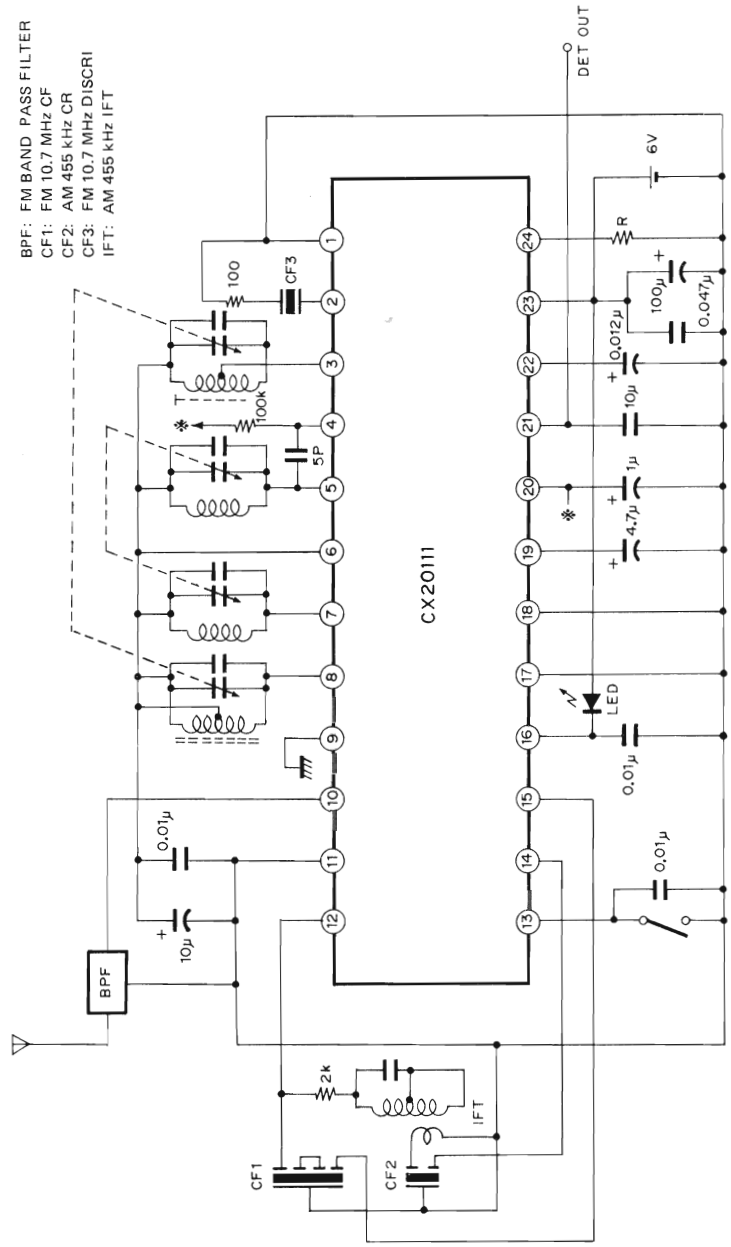
No.	Symbol	Voltage (V)*				Equivalent circuit
		Vcc=3V		Vcc=6V		
		FM	AM	FM	AM	
1	GND	—	—	—	—	—
2	FM DISCRI	2.18	2.70	3.08	3.60	
3	AM OSC	1.25	1.25	1.25	1.25	
4	AFC	1.25	1.15	1.25	1.15	
6	REG OUT	1.25	1.25	1.25	1.25	
5	FM OSC	1.25	1.25	1.25	1.25	
7	FM RF	1.25	1.25	1.25	1.25	
10	FM RF IN	0.3	0	0.3	0	

***Note)** See the DC Voltage Test Circuit.
Values are typical values.

No.	Symbol	Voltage (V)*				Equivalent circuit
		Vcc=3V		Vcc=6V		
		FM	AM	FM	AM	
8	AM RF IN	1.25	1.25	1.25	1.25	
9	NC	—	—	—	—	—
11	GND	—	—	—	—	—
12	FM/AM FE OUT	0.57	0.2	0.8	0.2	
13	BAND SELECT	1.25	0	1.25	0	
15	FM IF IN	1.25	0	1.25	0	
14	AM IF IN	0	0	0	0	
16	METER	1.6	1.6	4.5	4.5	
17	IF GND					
18	AM IF OUT					

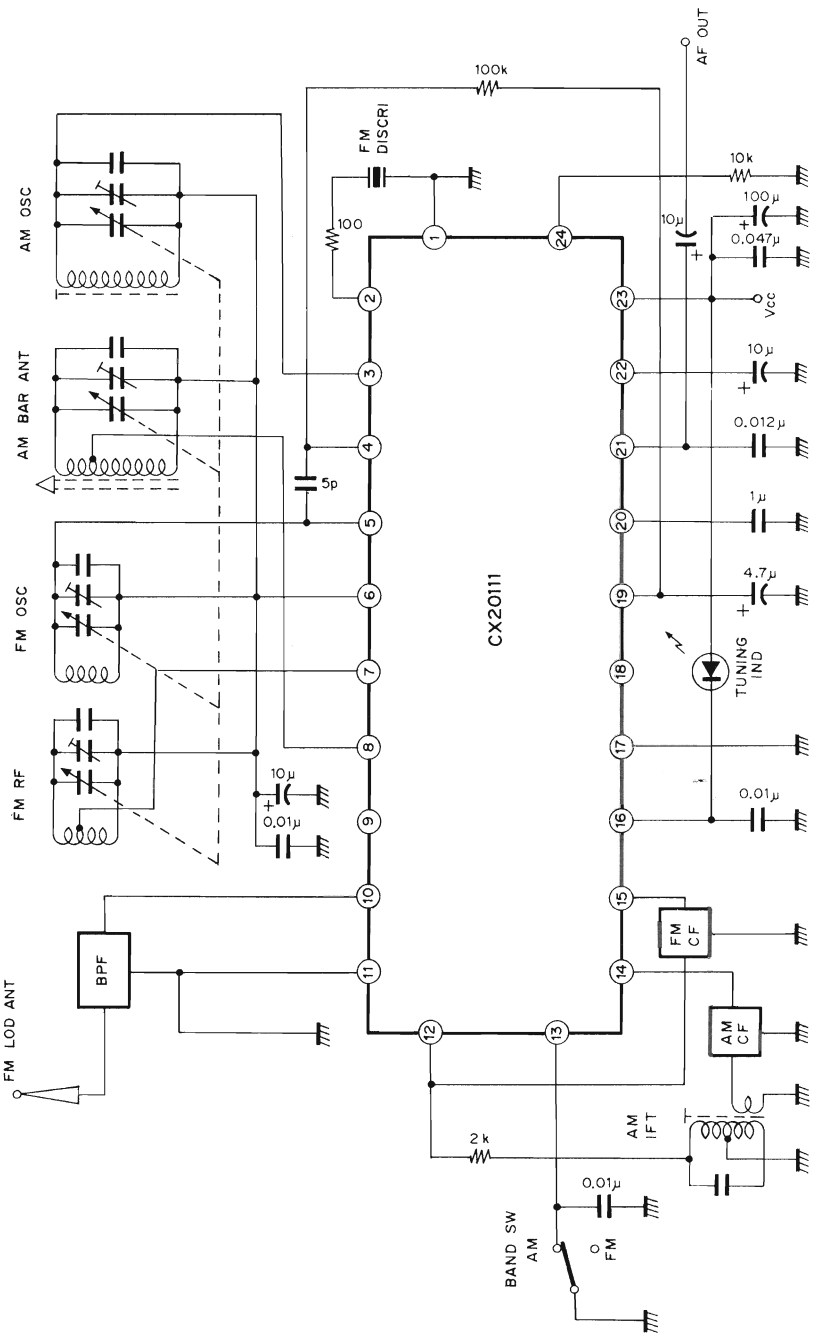
No.	Symbol	Voltage (V)*				Equivalent circuit
		Vcc=3V		Vcc=6V		
		FM	AM	FM	AM	
19	AFC/AGC 2	1.15	1.47	1.15	1.47	
20	AFC/AGC 1	1.47	1.15	1.47	1.15	
21	DET OUT	1.0	1.0	1.0	1.0	
22	RIPPLE	2.7	2.7	4.0	4.0	
23	Vcc	3.0	3.0	6.0	6.0	
24	BAND SIGNAL OUTPUT CONTROL					

DC Voltage Test Circuit

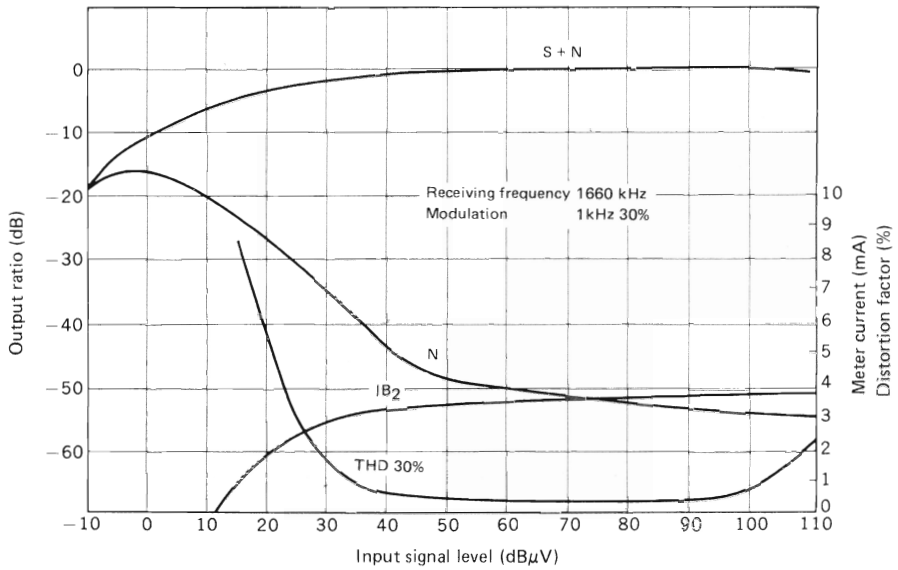


Note) • The meter current is cut off under the following conditions: CDA 10.7MG1 (Murata Seisakusho co.) is used as CF1, and the input frequency is either 10.7MHz ± 100kHz or more when R is 10kΩ, or 10.7MHz ± 150kHz or more when R is 100kΩ.
• The band signal output function cuts off the meter current when the signal is out of tuning by a specified frequency from the FM IF center frequency.
• The band signal output function is cut off when the voltage on pin 24 is the same as the regulator voltage or V_{CC}.

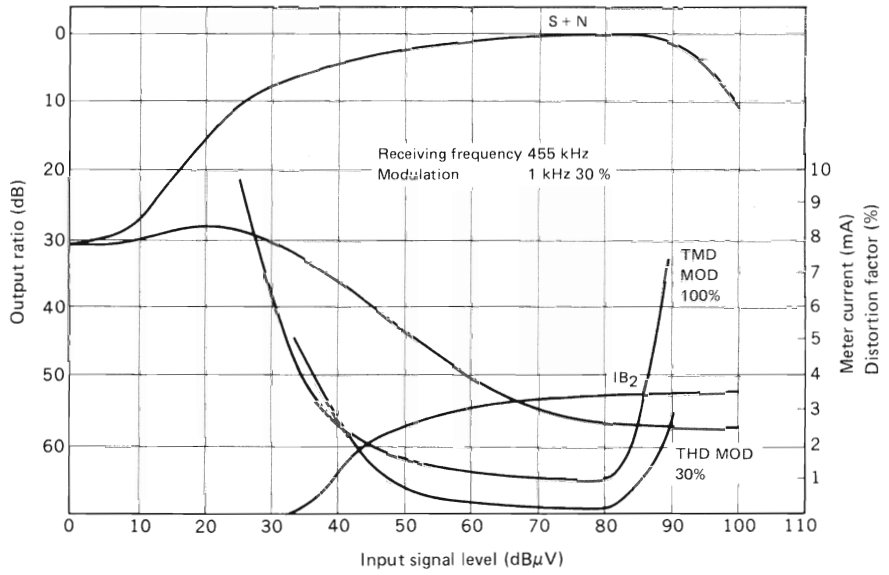
Application Circuit



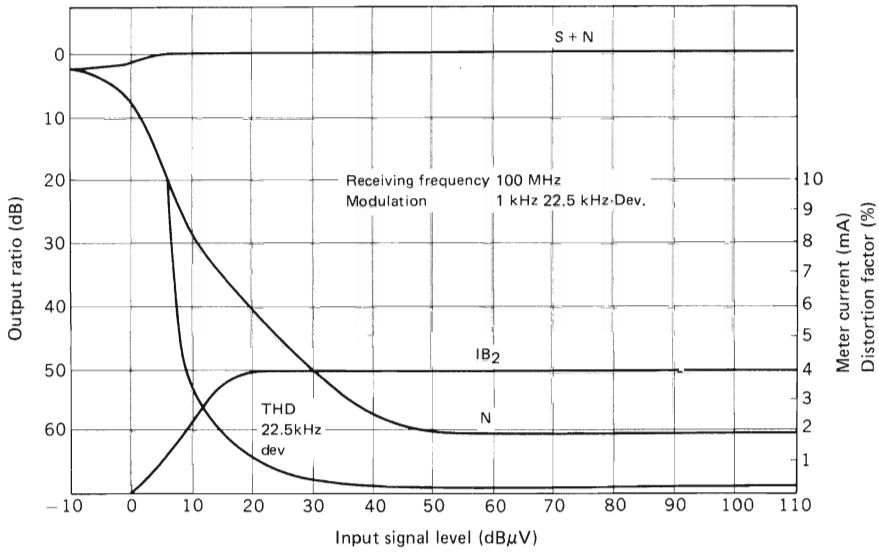
AM I/O Characteristic



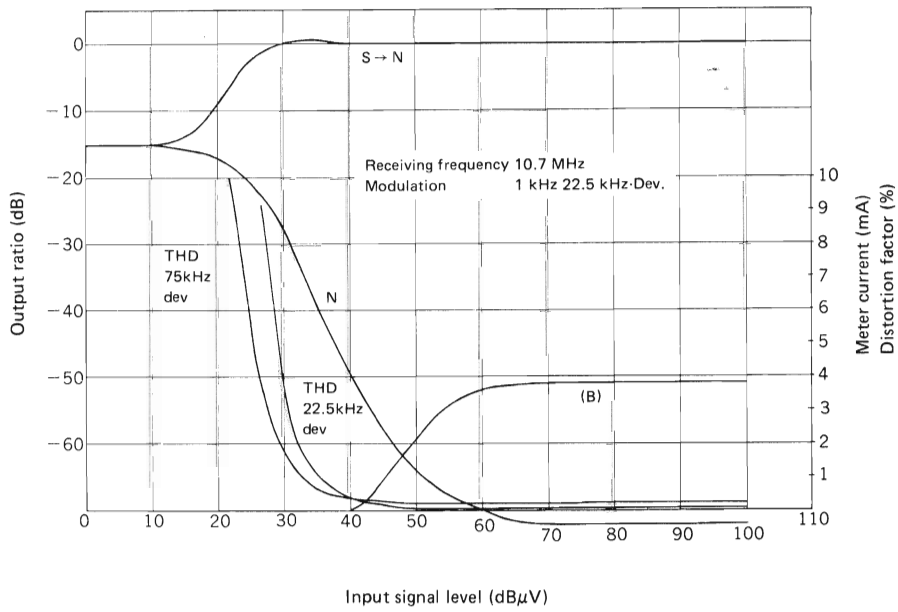
AM I/O Characteristic



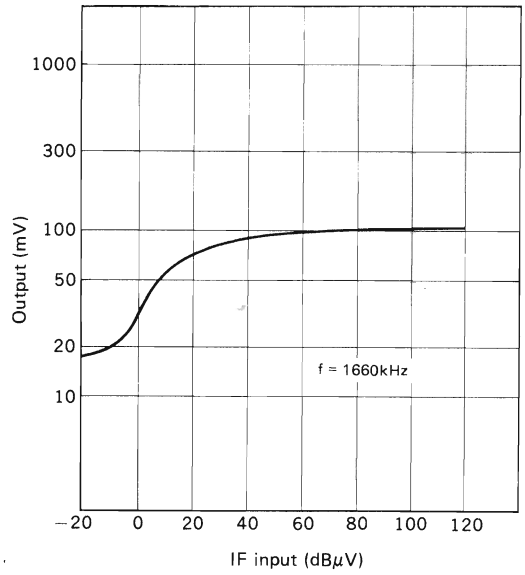
FM I/O Characteristic



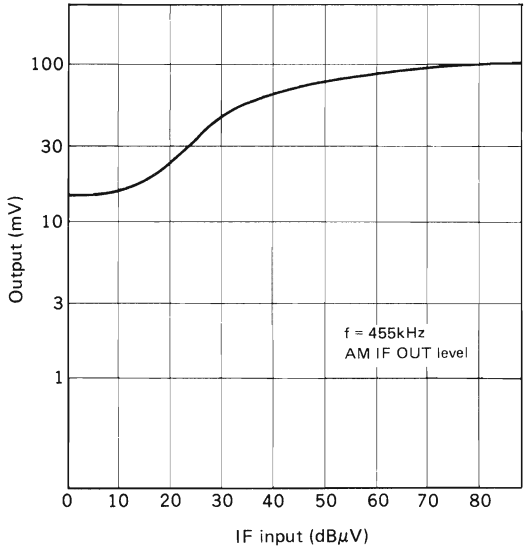
FM I/O Characteristic



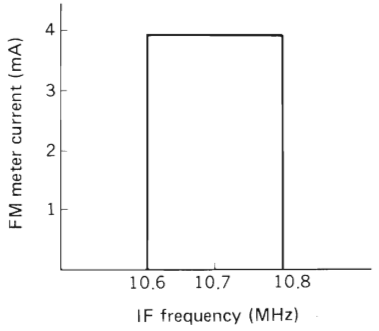
AM IF pin output vs. Input (Overall)



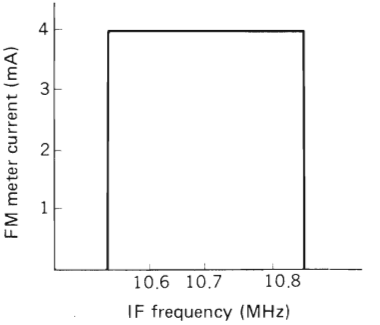
AM IF pin output vs. Input



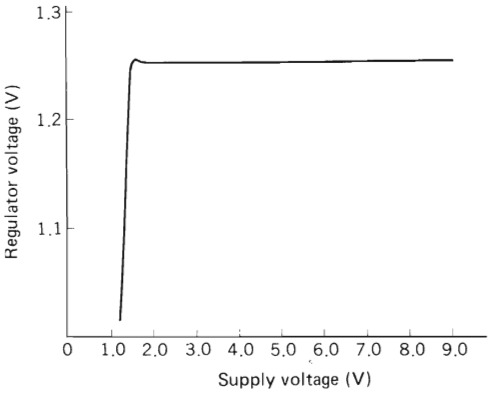
FM Band signal output characteristic (Narrow band)



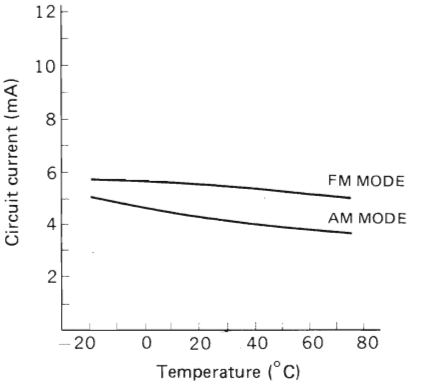
FM Band signal output characteristic (Normal)



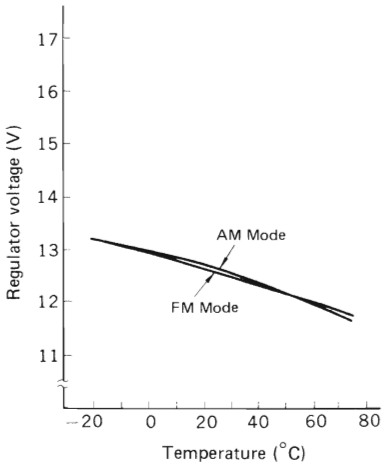
Regulater output vs. Supply voltage characteristics



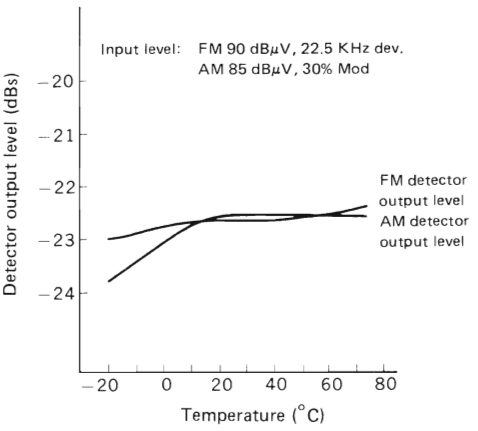
Temperature characteristics of circuit current



Temperature characteristics of regulator



Temperature characteristics of detector output



AM Stereo Radio

Description

The CX20177 is an IC for use with AM stereo radio, with an AM stereo system identification and audio signal processing functions integrated.

Features

- It identifies all AM stereo broadcasting systems (Magnavox, Kahn, Motorola and Harris) and displays the system, switching the reception mode automatically.
- By employing a PLL (Phase Locked Loop) pilot detection circuit and safety logic circuit, single channel interference or malfunction due to I.P.M. (Incidental Phase Modulation) is eliminated.
- System identification time is minimized to about one second.
- Single adjustment (using a semi-fixed resistor for VCO).
- Few peripheral parts required.
- High S/N ratio and low distortion factor.

Functions

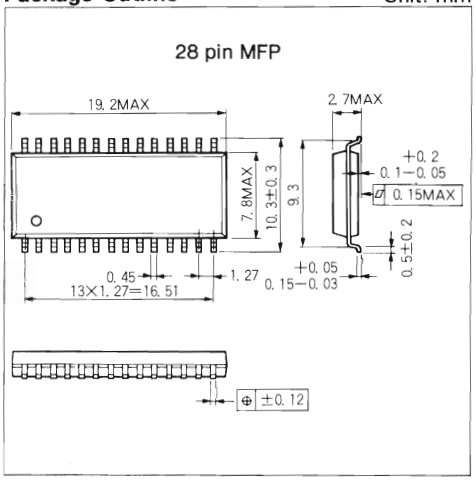
- PLL pilot detection circuit
- PSN (90° Phase Shift Network)
- Matrix circuit
- Malfunction preventive circuit
- Mute control output
- LED driver

Structure

Bipolar silicon monolithic IC

Package Outline

Unit: mm



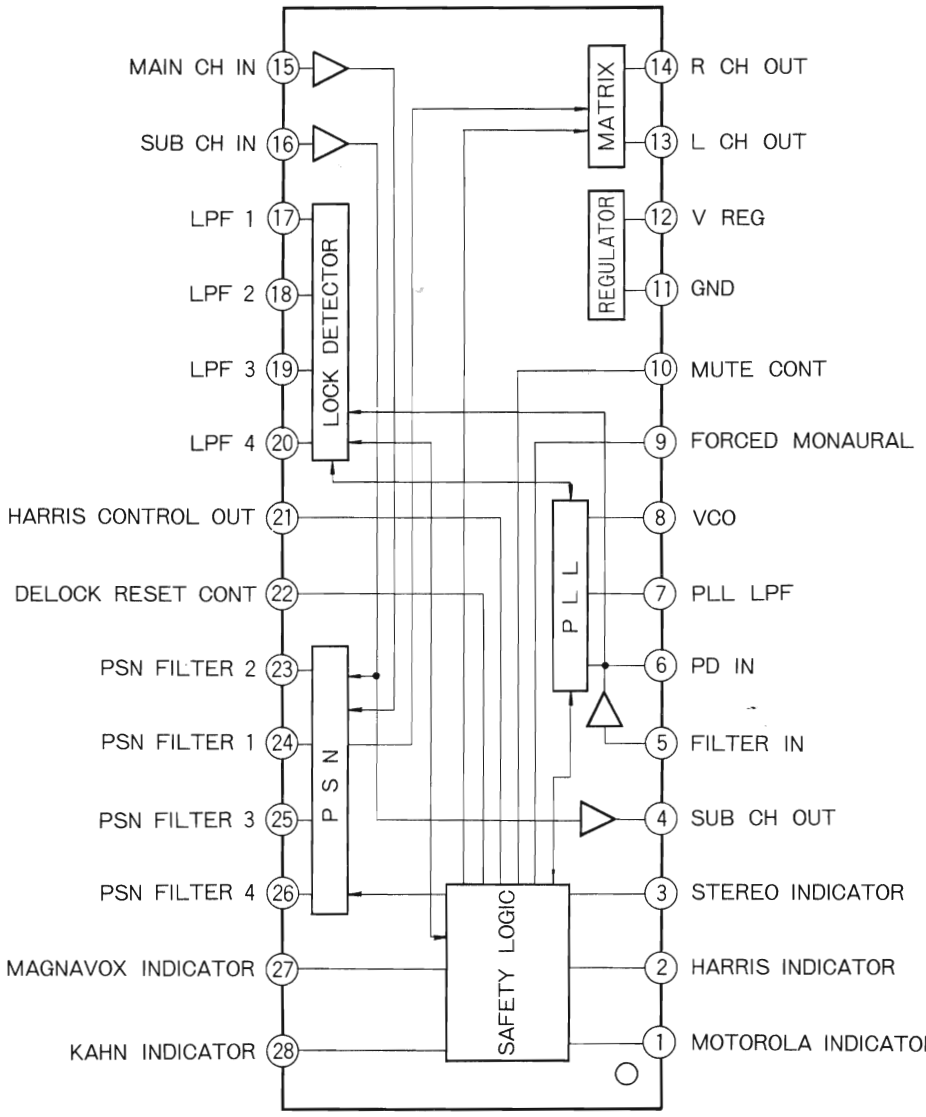
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	9	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	582	mW

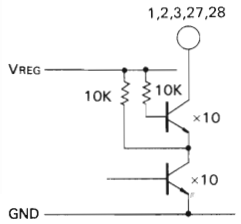
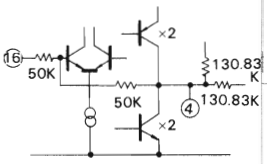
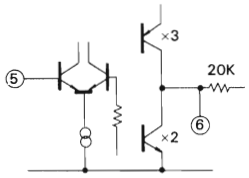
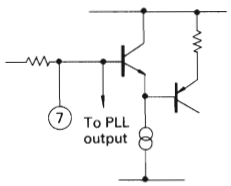
Recommended Operating Condition

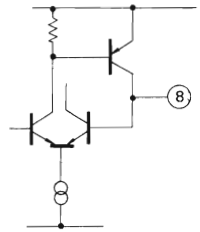
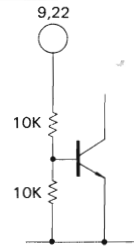
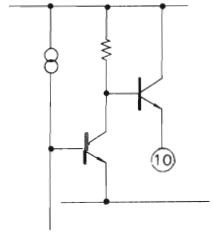
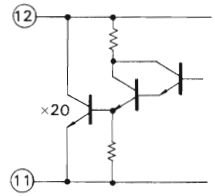
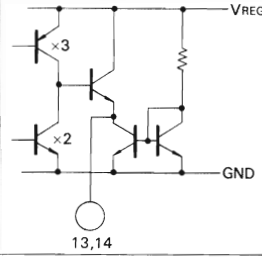
• Supply voltage	Vcc	5 to 8.5	V

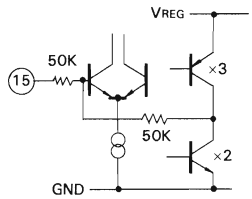
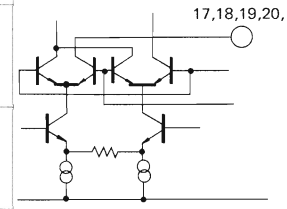
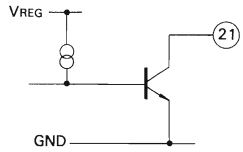
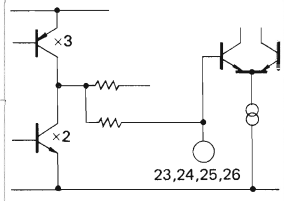
Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Symbol	Equivalent circuit	Voltage (V) (Typ.)	Description
1	MOTOROLA INDICATOR		8.0	LED drive circuit
2	HARRIS INDICATOR		8.0	LED drive circuit
3	STEREO INDICATOR		8.0	LED drive circuit
27	MAGNAVOX INDICATOR		8.0	LED drive circuit
28	KAHN INDICATOR		8.0	LED drive circuit
4	SUB CH OUT		1.5	Buffer (0dB) output from Pin 16 (Sub ch IN)
16	SUB CH IN		1.5	L−R+ pilot signal input circuit
5	FILTER IN		1.5	For pilot detection Op amp input for LPF
6	PD IN		1.5	OP amp output for LPF
7	PLL LPF		2.7	LPF for multi-PLL

No.	Symbol	Equivalent circuit	Voltage (V) (Typ.)	Description
8	VCO		2.8	For time constant of VCO for PLL
9	FORCED MONAURAL		0	Forced monaural reception with Hi-level pin input
22	LOCK OFF RESET CONT		0	Forced monaural reception with Low-level pin input
10	MUTE CONT		0	About ±18 ms 3.3 V pluse is generated mainly the moment matrix and PSN circuits are switched on or off.
11	GND		GND	
12	V_{REG}		4.0	4V (typ.) of a regulator output is obtained from Vcc via R_{REG}.
13	L_{CH} OUT		1.5	Lch signal output
14	R_{CH} OUT		1.5	Rch signal output

No.	Symbol	Equivalent circuit	Voltage (V) (Typ.)	Description
15	MAIN CH IN		1.5	L + R signal input circuit
17	LPF 1		3.0	LPF for Harris detection comparator
18	LPF 2		3.0	LPF for Motorola detection comparator
19	LPF 3		3.0	LPF for Kahn detection comparator
20	LPF 4		3.0	LPF for Magnavox detection comparator
21	HARRIS CONT		2.2	Current is drawn for Harris reception
23	PSN FILTER 2		1.5	Capacitor for PSN filter is connected (1000PF)
24	PSN FILTER 1		1.5	Capacitor for PSN filter is connected (10000PF)
25	PSN FILTER 3		1.5	Capacitor for PSN filter is connected (10000PF)
26	PSN FILTER 4		1.5	Capacitor for PSN filter is connected (1000PF)

Electrical Characteristics (Ta=25°C)

• Input condition MOT: Motorola HAR: Harris MAG: Magnavox KAH: Kahn

(Vcc=8V unless otherwise specified)

No.	Item	Symbol	Input condition	Switch conditions, No mark: OFF Mark: ON for the number 1	2	3	4	5	6	7	8	Measurement	Min.	Typ.	Max.	Unit
1	V_{REG} Voltage (L)	M9			A	B	A	B	B	A	B	Measure with Vcc at 5V during no signal	3.5	4.0	4.5	V
2	V_{REG} Voltage (H)	M9			B							Measure with Vcc at 10V during no signal	3.5	4.0	4.5	V
3	V_{REG} Voltage (M)	M9			C							Measure with Vcc at 8V during no signal	3.5	4.0	4.5	V
4	OFF CHECK1 (MOT)	M3											7.9	8.0	8.1	V
5	OFF CHECK1 (MAG)	M2											7.9	8.0	8.1	V
6	OFF CHECK1 (HAR)	M4											7.9	8.0	8.1	V
7	OFF CHECK1 (KAH)	M1											7.9	8.0	8.1	V
8	OFF CHECK1 (ST)	M5											7.9	8.0	8.1	V
9	OFF CHECK1 (HAR)	M6											3.9	4.0	4.1	V
10	OFF CHECK1 (MUTE)	M8											−0.1	0	0.1	V
11	Check VCO operation	M7										Measure with Vcof=33kHz by changing V_f with V_H=2.75V, V_L=2.55V, V_M=2.65V	33.0 32.0		34.0 33.0	kHz
12	VCO oscillation level check	M7							↓		↓	Measure by controlling V_f DC so M_7 output frequency becomes 33kHz	0.5	0.7	0.9	V
13	Lock CHECK (MOT)	M3	MOT						A		A	Input −53dBm pilot signal (f=250Hz) (until measuring point DC becomes less than 0.6V)	72		110	ms
14	ST IND CHECK	M5	MOT									Input −53dBm pilot signal (f=250Hz) (until measuring point DC becomes less than 0.6V)	0		0.6	V
15	OFF CHECK2 (MAG)	M2	MOT									Input −53dBm pilot signal (f=250Hz) (until measuring point DC becomes less than 0.6V)	7.9	8.0	8.1	V
16	OFF CHECK2 (HAR)	M4	MOT									Input −53dBm pilot signal (f=250Hz) (until measuring point DC becomes less than 0.6V)	7.9	8.0	8.1	V
17	OFF CHECK2 (KAH)	M1	MOT			↓		↓				Input −53dBm pilot signal (f=250Hz) (until measuring point DC becomes less than 0.6V)	7.9	8.0	8.1	V
18	STR output level (R)	M11	MOT			A		A		↓		Rch output when −26dBm (f=1kHz) signal is input simultaneously with the pilot signal	−23	−20	−17	dBm
19	STR output level (L)	M10	MOT							B		Lch output when −26dBm (f=1kHz) signal is input simultaneously with the pilot signal	−23	−20	−17	dBm
20	STR separation (R)	M11	MOT							A		Rch separation when −26dBm (f=1kHz) signal is input simultaneously with the pilot signal	23			dB
21	STR separation (L)	M10	MOT							B		Lch separation when −26dBm (f=1kHz) signal is input simultaneously with the pilot signal	23			dB
22	STR distortion factor (R)	M11	MOT							A		Rch distortion factor when −26dBm (f=1kHz) signal is input simultaneously with the pilot signal			1.1	%
23	STR distortion factor (L)	M10	MOT			↓		↓		B		Lch distortion factor when −26dBm (f=1kHz) signal is input simultaneously with the pilot signal			1.1	%
24	F-MONO operation 1 (MOT)	M3	MOT	ON		B		B		A			7.9	8.0	8.1	V
25	F-MONO operation 2 (MOT)	M5	MOT	↓									7.9	8.0	8.1	V
26	MUTE pulse check 1	M8	MOT									Check if M8 outputs pulse more than 3V	0		11	ms
27	MUTE pulse check 2	M8	MOT									Check if M8 outputs pulse more than 3V	18		55	ms
28	Lock R operation 1 (MOT)	M3	MOT									Check if M3 becomes Hi by making C1 at 3V	7.9	8.0	8.1	V
29	Lock R operation 2 (MOT)	M5	MOT									Check if M5 becomes Hi by making C1 at 3V	7.9	8.0	8.1	V
30	MUTE pulse check 3	M8	MOT									Check if M8 outputs pulse more than 3V	0		11	ms
31	Lock CHECK (MAG)	M2	MAG		↓	↓	↓	↓	↓	↓	↓	Input −39dBm (f=50Hz) pilot signal (until measuring point DC becomes less than 0.6V)	72		110	ms

Electrical Characteristics (Ta=25°C)

• Input condition MOT: Motorola MAG: Magnavox HAR: Harris KAH: Kahn

(Vcc=8V unless otherwise specified)

No.	Item	Symbol	* Input condition	Switch conditions, No mark: OFF, Mark: ON for the number								Measurement	Min.	Typ.	Max.	Unit
				1	2	3	4	5	6	7	8					
32	ST IND CHECK	M5	MAG		C	B	A	B	A	A	A	Input −39dBm (f=50Hz) pilot signal (until measuring point DC becomes less than 0.6V)	0		0.6	V
33	OFF CHECK3 (MOT)	M3	MAG									Input −39dBm (f=50Hz) pilot signal (until measuring point DC becomes less than 0.6V)	7.9	8.0	8.1	V
34	OFF CHECK3 (HAR)	M4	MAG									Input −39dBm (f=50Hz) pilot signal (until measuring point DC becomes less than 0.6V)	7.9	8.0	8.1	V
35	OFF CHECK3 (KAH)	M1	MAG			↓		↓				Input −39dBm (f=50Hz) pilot signal (until measuring point DC becomes less than 0.6V)	7.9	8.0	8.1	V
36	STR output level (R)	M11	MAG			A		A		↓		Rch output when −26dBm (f=1kHz) signal is input simultaneously with pilot signal	−23	−20	−17	dBm
37	STR output level (L)	M10	MAG							B		Lch output when −26dBm (f=1kHz) signal is input simultaneously with pilot signal	−23	−20	−17	dBm
38	STR separation (R)	M11	MAG							A		Rch separation when −26dBm (f=1kHz) signal is input simultaneously with pilot signal	23			dB
39	STR separation (L)	M10	MAG							B		Lch separation when −26dBm (f=1kHz) signal is input simultaneously with pilot signal	23			dB
40	STR distortion factor (R)	M11	MAG							A		Rch distortion factor when −26dBm (f=1kHz) signal is input simultaneously with pilot			1.1	%
41	STR distortion factor (L)	M10	MAG			↓				B		Lch distortion factor when −26dBm (f=1kHz) signal is input simultaneously with pilot			1.1	%
42	F-MONO operation 1 (MAG)	M2	MAG	ON		B				A			7.9	8.0	8.1	V
43	F-MONO operation 2 (MAG)	M5	MAG	↓									7.9	8.0	8.1	V
44	MUTE pulse check 1	M8	MAG									Check if M8 outputs pulse more than 3V	0		11	ms
45	MUTE pulse check 2	M8	MAG									Check if M8 outputs pulse more than 3V	18		55	ms
46	Lock-R operation 1 (MAG)	M2	MAG					↓				Check if M2 becomes Hi by making C1 3V	7.9	8.0	8.1	V
47	Lock-R operation 2 (MAG)	M5	MAG					B				Check if M2 becomes Hi by making C1 3V	7.9	8.0	8.1	V
48	MUTE pulse check 3	M8	MAG			↓			↓		↓	Time before pulse of more than DC=3V is output when C1 is made 3V	0		11	ms
49	MONO output level (R)	M11				A			B		B	Rch output when −26dBm (f=1kHz) signal is input	−29	−26	−23	dBm
50	MONO output level (L)	M10										Lch output when −26dBm (f=1kHz) signal is input	−29	−26	−23	dBm
51	MONO distortion factor (R)	M11										Rch distortion factor when −26dBm (f=1kHz) signal is input			1.1	%
52	MONO distortion factor (L)	M10				↓			↓		↓	Lch distortion factor when −26dBm (f=1kHz) signal is input			1.1	%
53	Lock CHECK (HAR)	M4	HAR			B			A		A	Input −38dBm (f=550Hz) pilot signal (until measuring point DC becomes less than 0.6V)	72		110	ms
54	ST IND CHECK	M5	HAR									Input −38dBm (f=550Hz) pilot signal (until measuring point DC becomes less than 0.6V)	0		0.6	V
55	OFF CHECK4 (MOT)	M3	HAR									Input −38dBm (f=550Hz) pilot signal (until measuring point DC becomes less than 0.6V)	7.9	8.0	8.1	V
56	OFF CHECK4 (KAH)	M1	HAR									Input −38dBm (f=550Hz) pilot signal (until measuring point DC becomes less than 0.6V)	7.9	8.0	8.1	V
57	OFF CHECK4 (MAG)	M2	HAR									Input −38dBm (f=550Hz) pilot signal (until measuring point DC becomes less than 0.6V)	7.9	8.0	8.1	V
58	HAR CONT operation	M6	HAR			↓		↓				Input −38dBm (f=550Hz) pilot signal until measuring point DC becomes less than 0.6V)	0		0.6	V
59	STR output level (R)	M11	HAR			A		A		↓		Rch output when −26dBm (f=1kHz) signal is input (until similar condition as above met)	−23	−20	−17	dBm
60	STR output level (L)	M10	HAR							B		Lch output when −26dBm (f=1kHz) signal is input (until similar condition as above met)	−23	−20	−17	dBm
61	STR separation (R)	M11	HAR							A		Rch separation when −26dBm (f=1kHz) signal is input with similar condition as above	23			dB
62	STR separation (L)	M10	HAR		↓	↓	↓	↓	↓	B	↓	Lch separation when −26dBm (f=1kHz) signal is input with similar condition as above	23			dB

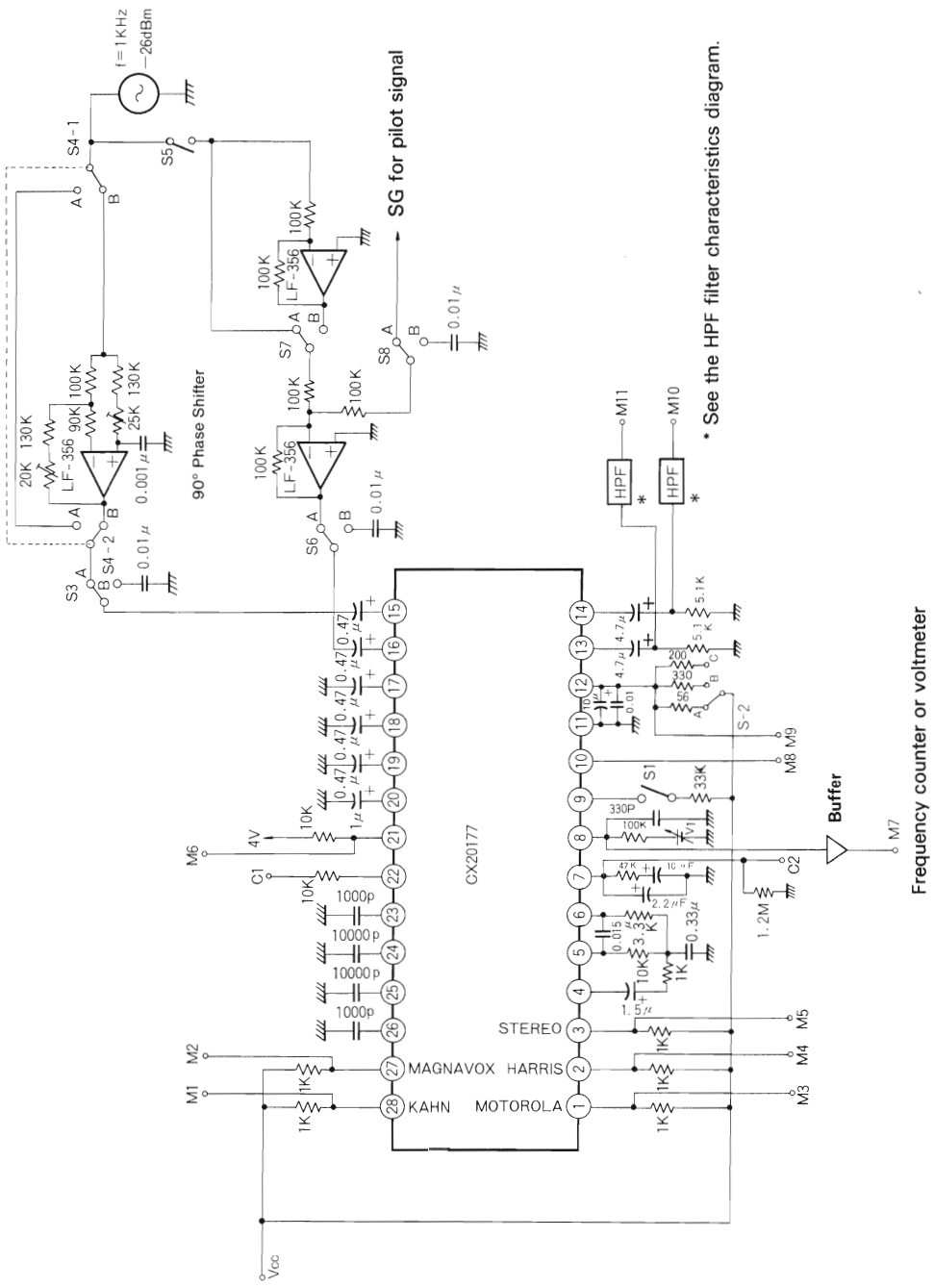
Electrical Characteristics (Ta=25°C)

• Input condition MOT: Motorola MAG: Magnavox HAR: Harris KAH: Kahn

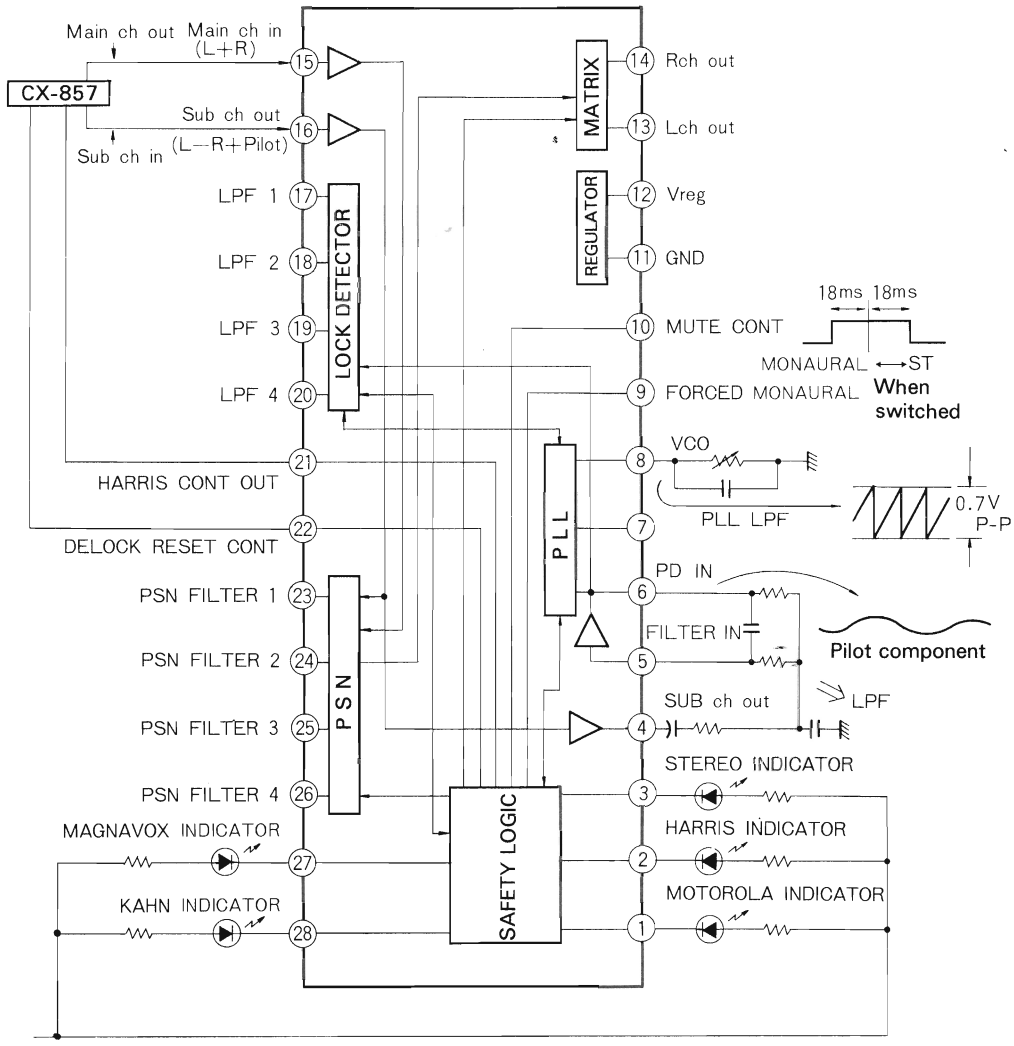
(Vcc=8V unless otherwise specified)

No.	Item	Symbol	* Input condition	Switch conditions, No mark: OFF Mark: ON for the number 1	2	3	4	5	6	7	8	Measurement	Min.	Typ.	Max.	Unit
63	STR distortion factor (R)	M11	HAR		C	A	A	A	A	A	A	Rch distortion factor with −26dBm (f=1kHz) signal is input with similar condition as above			1.1	%
64	STR distortion factor (L)	M10	HAR			↓		↓		B		Lch distortion factor with −26dBm (f=1kHz) signal is input with similar condition as above			1.1	%
65	F-MONO operation 1 (HAR)	M4	HAR			B		B		A		Check if M4 becomes Hi when S1 is set to ON	7.9	8.0	8.1	V
66	F-MONO operation 2 (HAR)	M5	HAR									Check if M5 becomes Hi when S1 is set to ON	7.9	8.0	8.1	V
67	MUTE pulse check 1	M8	HAR									Time before pulse more than DC=3V is output right after S1 is set to ON	0		11	ms
68	MUTE pulse check 2	M8	HAR									Time before pulse more than DC=3V is output right after S1 is set to OFF	18		55	ms
69	Lock-R operation 1 (HAR)	M4	HAR									Check if M4 becomes Hi by making C1 3V	7.9	8.0	8.1	V
70	Lock-R operation 2 (HAR)	M5	HAR									Check if M4 becomes Hi by making C1 3V	7.9	8.0	8.1	V
71	MUTE pulse check 3	M8	HAR									Time before pulse more than DC=3V is output right after C1 is set to 3V	0		11	ms
72	Lock CHECK (KAH)	M1	KAH									Input −52dBm (f=150Hz) pilot signal (until measuring point DC becomes less than 0.6V)	72		110	ms
73	ST IND CHECK	M5	KAH									Input −52dBm (f=150Hz) pilot signal (until measuring point DC becomes less than 0.6V)	0		0.6	V
74	OFF CHECKS (MOT)	M3	KAH									Input −52dBm (f=150Hz) pilot signal (until measuring point DC becomes less than 0.6V)	7.9	8.0	8.1	V
75	OFF CHECKS (HAR)	M4	KAH									Input −52dBm (f=150Hz) pilot signal (until measuring point DC becomes less than 0.6V)	7.9	8.0	8.1	V
76	OFF CHECKS (MAG)	M2	KAH			↓	↓	↓				Input −52dBm (f=150Hz) pilot signal (until measuring point DC becomes less than 0.6V)	7.9	8.0	8.1	V
77	KAH output level (R)	M11	KAH			A	B	A		↓		Rch output when −26dBm (f=1kHz) signal is input until condition as above is met	−23	20	17	dBm
78	KAH output level (L)	M10	KAH							B		Lch output when −26dBm (f=1kHz) signal is input until condition as above is met	−23	20	17	dBm
79	KAH separation (R)	M11	KAH							A		Rch output when −26dBm (f=1kHz) signal is input until condition as above is met	23			dB
80	KAH separation (L)	M10	KAH							B		Lch output when −26dBm (f=1kHz) signal is input until condition as above is met	23			dB
81	KAH distortion factor (R)	M11	KAH							A		Rch distortion factor when −26dBm (f=1kHz) signal is input until condition as above is met.			1.1	%
82	KAH distortion factor (L)	M10	KAH			↓	↓	↓		B		Lch distortion factor when −26dBm (f=1kHz) signal is input until condition as above is met.			1.1	%
83	F-MONO operation 1 (KAH)	M1	KAH			B	A	B		A		Check if M1 becomes Hi when S1 is set to ON	7.9	8.0	8.1	V
84	F-MONO operation 2 (KAH)	M5	KAH									Check if M5 becomes Hi when S1 is set to ON	7.9	8.0	8.1	V
85	MUTE pulse check 1	M8	KAH									Time before pulse more than DC=3V is output when S1 is set to ON	0		11	ms
86	MUTE pulse check 2	M8	KAH									Time before pulse more than DC=3V is output when S1 is set to OFF	18		55	ms
87	Lock-R operation 1 (KAH)	M1	KAH									Check if M1 becomes Hi when C1 is set to 3V	7.9	8.0	8.1	V
88	Lock-R operation 2 (KAH)	M5	KAH									Check if M5 becomes Hi when C1 is set to 3V	7.9	8.0	8.1	V
89	MUTE pulse check 3	M8	KAH		↓	↓	↓	↓	↓	↓	↓	Time before pulse more than DC=3V is output right after C1 is set to 3V	0		11	ms

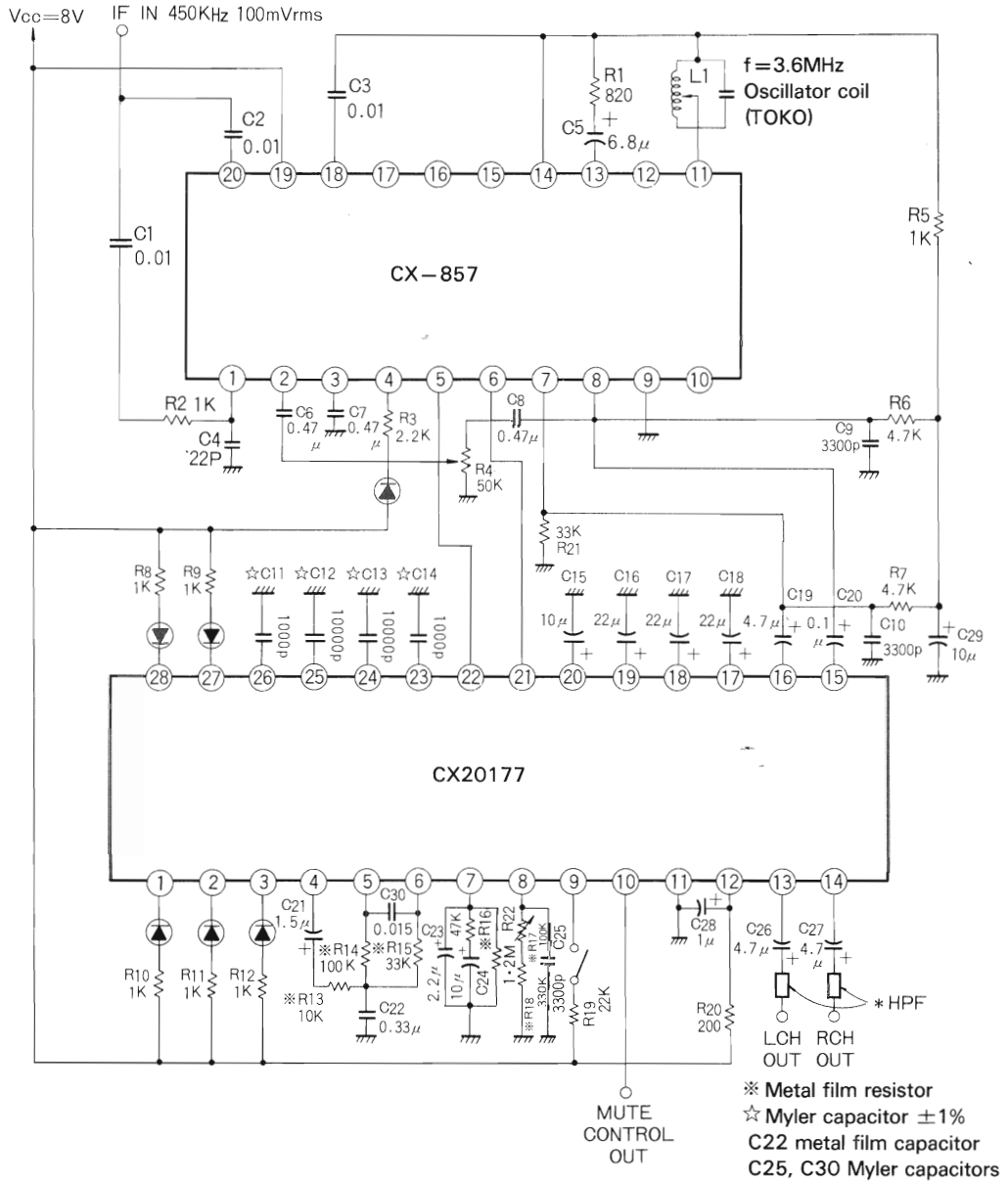
Electrical Characteristics Test Circuit



Description of Operation



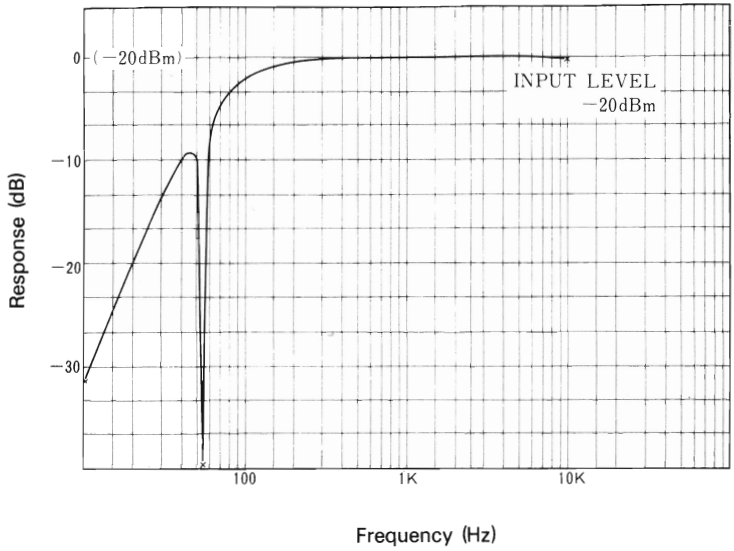
Application Circuit



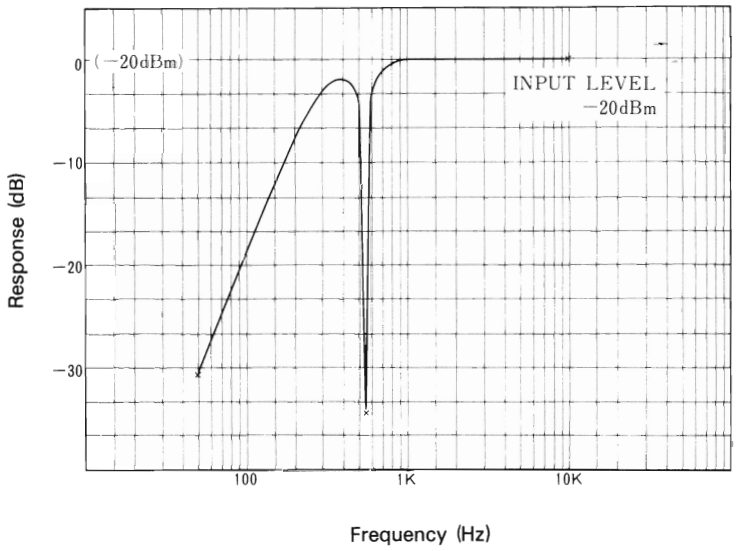
※ Metal film resistor
☆ Myler capacitor ±1%
C22 metal film capacitor
C25, C30 Myler capacitors

* See the HPF filter characteristics.

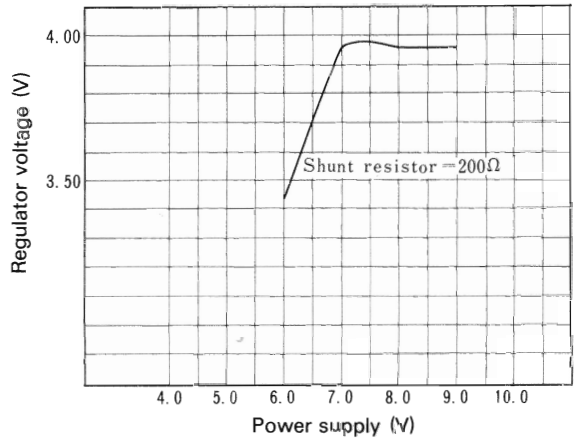
HPF Filter characteristics



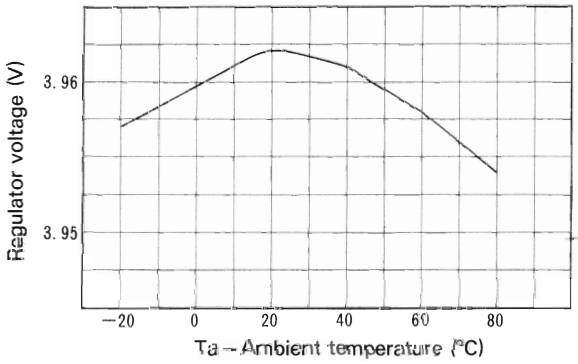
Filter frequency for characteristics evaluation



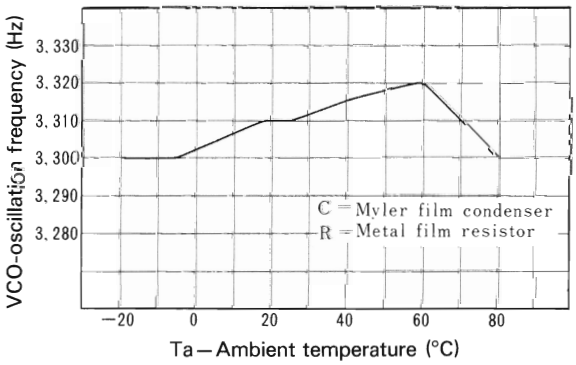
Shunt regulator characteristics



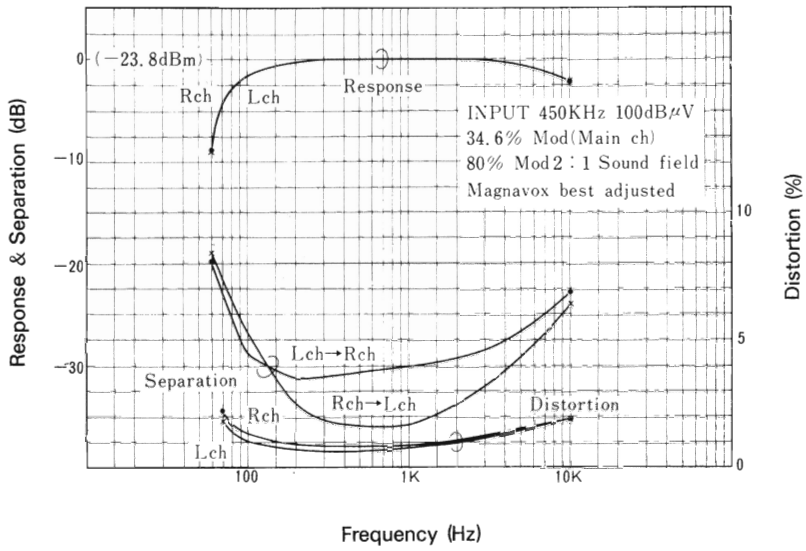
Regulator temperature characteristics



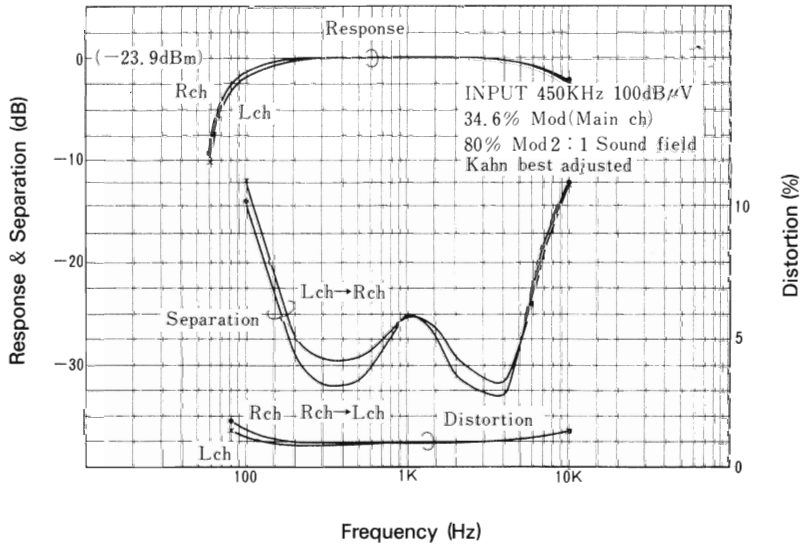
VCO Oscillation frequency temperature characteristics



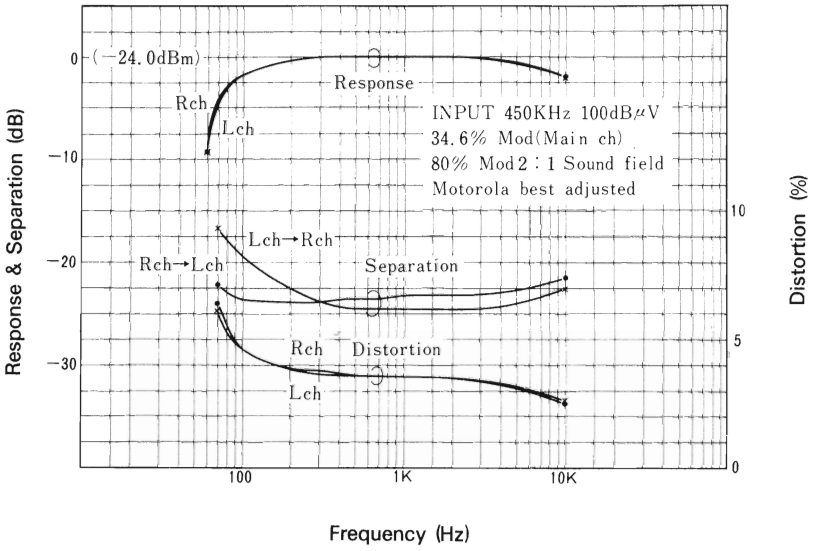
CX-857 + CX20177 (Magnavox mode)



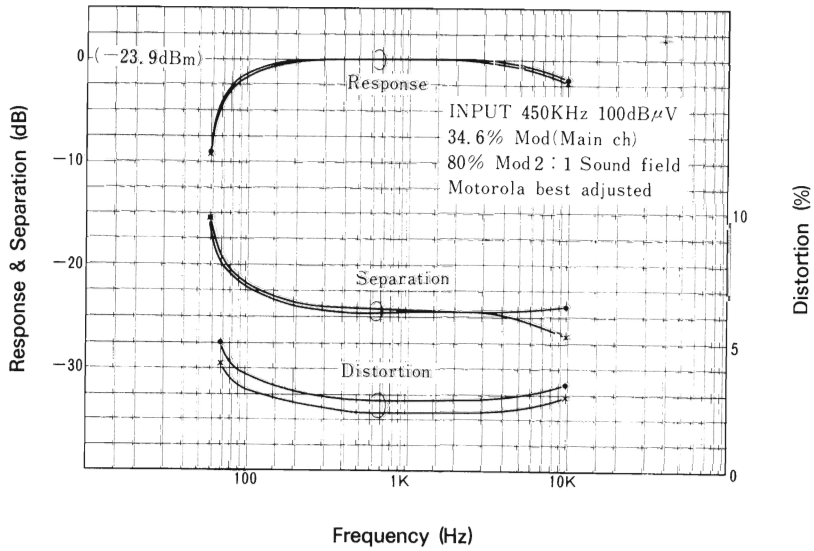
CX-857 + CX20177 (Kahn mode)



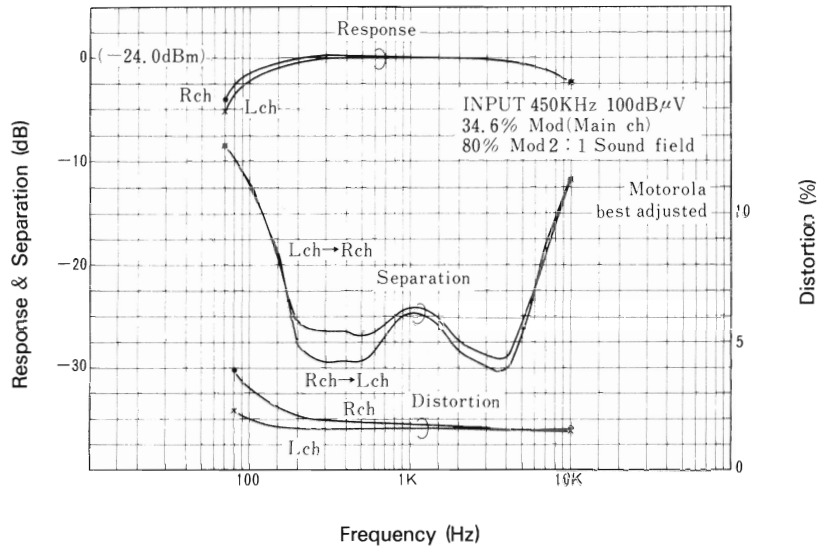
CX-857 + CX20177 (Motorola mode)



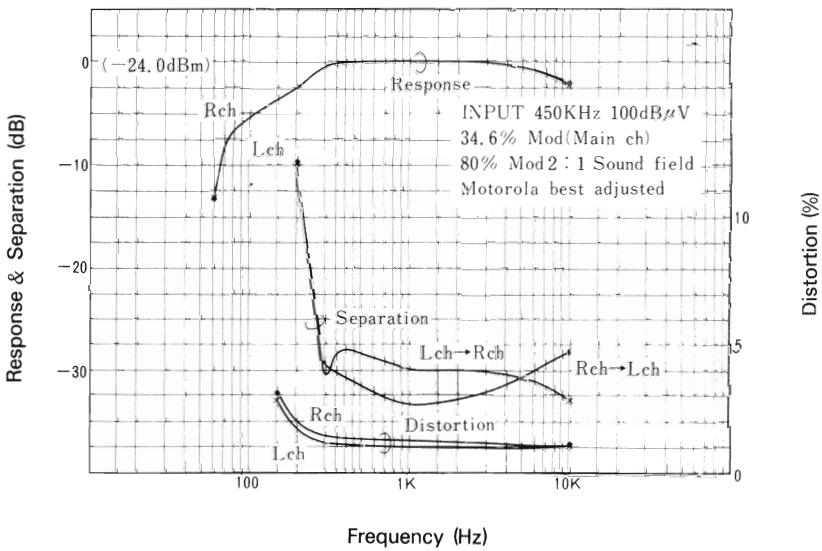
CX-857 + CX20177 (Magnavox mode)



CX-857 + CX20177 (Kahn mode)



CX-857 + CX20177 (Harris mode)



Pin Description of the PCB

IF IN : IF INPUT pin for the input of 450 kHz 100mVrms signal.

GND : Ground

Vcc : 8 V. Vary the R20 value of CX20177 (CXA1017M) in accordance with the shunt regulator. Since the shunt regulator output voltage (CX20177: Pin 12, CXA1017M: Pin 10) has been set at 4 V, set the R20 to satisfy the following.

$$\frac{Vcc - 4\ V}{R20} \geqq 15\ mA$$

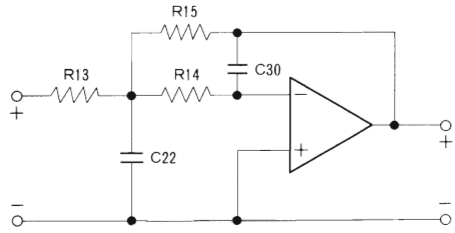
Rch, Lch : Rch, Lch output pin for the stereo signal. It is possible to drive up to about 0 dB_{10} with $R_L = 5\ k\Omega$.

MUTE : If generates a pulse (about 3.3 V) with the width of ±20 ms mainly at the time of switching between Monaural and Stereo and PSN switching between ON and OFF.

Forced Monaural Switch : Switching to ON enables reception of the monaural mode forcibly.

Operation of Main Parts

R1,C5 : CX-857 PLL LPF constant
R4 : Input level setting to the divider
C11 – C14 : Capacitor for PSN
C15 – C18 : Capacitor for Pilot lock detector
C21, 22, 30, R13 – R15 } Secondary Low pass active filter



C23, 24, R16, 22 } For PLL LPF of the CX20177
R17, 18, C25 } For VCO of the CX20177
R20 : Resistor for the shunt regulator

Adjustment and Check Methods of the AM Stereo Evaluation PCB

1) Adjustment method

Only three points are to be adjusted for the evaluation PCB.

1-1 Adjustment of the CX-857 VCO oscillation frequency
Input the non-modulated signal 450kHz 100mVrms (100 dBμ) through the IF IN pin printed on the PCB and turn the oscillation coil so the CX-857 Pin 13 DC voltage becomes 1.7 V.

1-2 Input level adjustment of the divider
Input the 450kHz 100mVrms with 45% modulation (Motorola mode) through IF and adjust R4 (VOL) so the Lch or Rch output distortion factor is minimized.

1-3 Adjustment of the CX20177 (CXA1017M) VCO oscillation frequency
Monitor the Vcc oscillation frequency and adjust R17 (VOL) so the frequency becomes 3,300Hz at the time of free run.

2) Operation check method of the CX20177 (CXA1017M)

The following is a simple check method to identify the system using the pilot signal.

2-1 Identification confirmation using the pilot signal
Input the pilot frequency signal through Pin 16 (Pin 14) via a capacitor. The frequency and signal level are as follows:

Note) When CX-857 is not locked (when the CX-857 lock LED is not lit with the input of a 450 kHz carrier to IF), the forcible monaural signal is output from CX-857 to CX-20177 (CXA1017M) (Pin 22 and 20 has entered low level). At this time, do not use the IF input but apply 3 V to Pin 22 and 20, in checking the above use CX20177 (CXA1017M) alone.

Parts List of the AM Stereo Standard Circuit

L1, 3.6 MHz, Oscillator coil (TOKO) 1-406-070-11

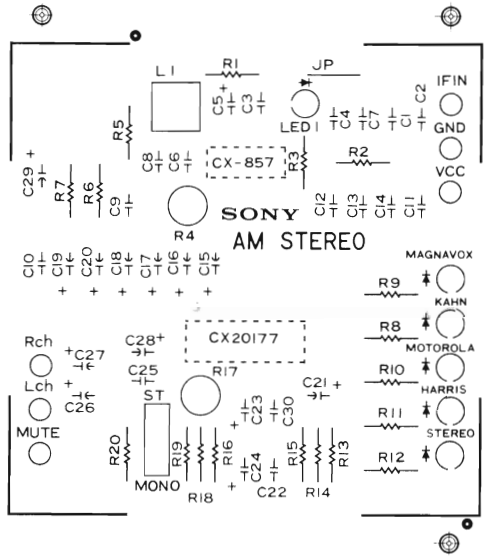
1 Resistor

R1	820Ω	Carbon	R12	1kΩ	Carbon
R2	1kΩ	Carbon	R13	10kΩ	Metal film
R3	2.2kΩ	Carbon	R14	100kΩ	Metal film
R4	50kΩ	Semi-fixed	R15	33kΩ	Metal film
R5	1kΩ	Carbon	R16	47kΩ	Metal film
R6	4.7kΩ	Carbon	R17	100kΩ	Metal film semi-fixed
R7	4.7kΩ	Carbon	R18	330kΩ	Metal film semi-fixed
R8	1kΩ	Carbon	R19	22kΩ	Carbon
R9	1kΩ	Carbon	R20	200Ω	Carbon
R10	1kΩ	Carbon	R21	33kΩ	Carbon
R11	1kΩ	Carbon	R22	1.2MΩ	Carbon

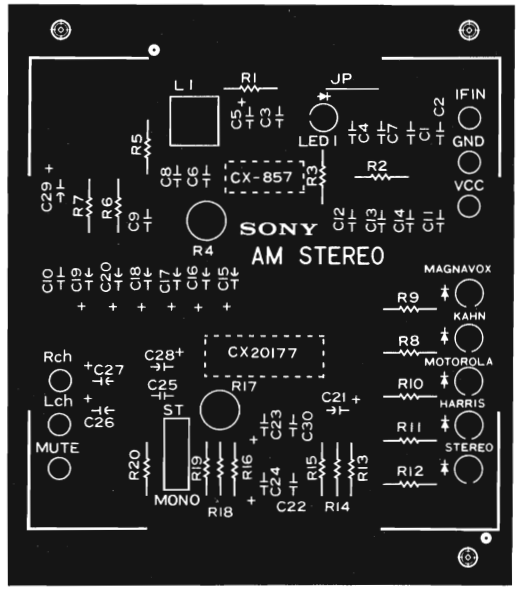
2 Capacitor

C1	0.01μF	Ceramic	C21	1.5μF	Electrolytic
C2	0.01μF	Ceramic	C22	0.33μF	Metal film
C3	0.01μF	Ceramic	C23	2.2μF	Tantalum
C4	22pF	Ceramic	C24	10μF	Tantalum
C5	6.8μF	Tantalum	C25	3300pF	Myler
C6	0.47μF	Electrolytic	C26	4.7μF	Electrolytic
C7	0.47μF	Electrolytic	C27	4.7μF	Electrolytic
C8	0.47μF	Electrolytic	C28	1μF	Electrolytic
C9	3300pF	Ceramic	C29	10μF	Electrolytic
C10	3300pF	Ceramic	C30	0.015μF	Myler
C11	1000pF	Myler ±1%			
C12	10000pF	Myler ±1%			
C13	10000pF	Myler ±1%			
C14	1000pF	Myler ±1%			
C15	10μF	Electrolytic			
C16	22μF	Electrolytic			
C17	22μF	Electrolytic			
C18	22μF	Electrolytic			
C19	4.7μF	Electrolytic			
C20	0.1μF	Electrolytic			

Silk Diagram



Pattern Diagram



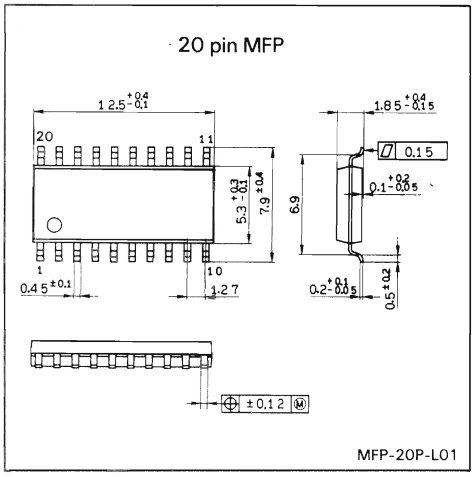
AM Radio

Description

The CXA1015M is one-chip bipolar IC designed for an AM radio set. All functions required for a radio, AM front-end, AM IF amplifier (AM AGC, DET, LED drive circuit) and audio power amplifier (with electronic volume), are integrated into this high performance IC.

Package Outline

Unit: mm



Features

- Contains all necessary functions from the front end to final audio stage.
- Minimum operating supply voltage is at 1.8V typically.
- Low current consumption (I_D = 2.7 mA typically for V_{CC} = 3V)
- Built-in LED drive circuit for tuning
- Built-in electronic volume
- Few peripheral parts.
- Large output (EIAJ output = 540 mW typically for V_{CC} = 6V with 8Ω load)

Structure

Bipolar silicon monolithic IC

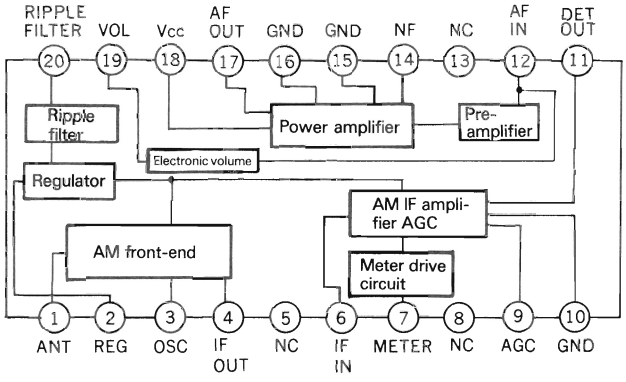
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	9	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−50 to +125	°C
• Junction temperature	Tj	125	°C
• Allowable power dissipation	P_D	500	mW

Recommended Operating Condition

• Supply voltage	V_{CC}	2 to 7	V

Block Diagram



Electrical Characteristics

(Ta = 25°C, V_{CC} = 6V unless otherwise specified: See the test circuit.)

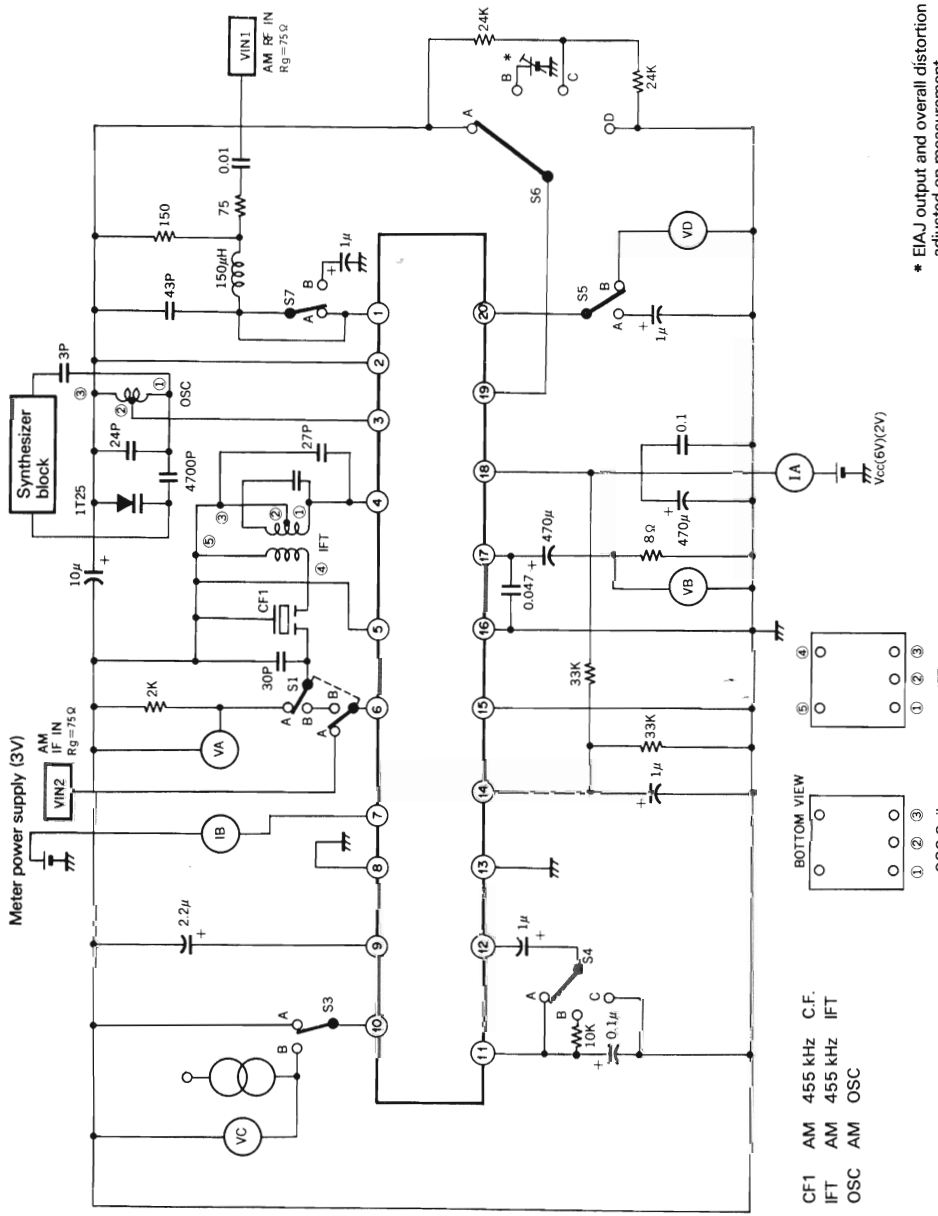
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Circuit current	I_A	No signal	2.07	3.0	4.95	mA
IF + AF (reduced voltage) Output level	V_{B1}	V_{IN2} = 455 kHz (1 kHz, 30% MOD) Output level V_{CC} = 2V	−6	−1		dBs
IF + AF Voltage gain	G_{V1}	V_{IN2} = 455 kHz (1 kHz, 30% MOD) Level at V_{IN2} for output level −4 dBs		23	29	dBμ
Meter current	I_B	V_{IN2} = 85 dBμ, 455 kHz (1 kHz, 30% MOD)	1.35	2.5	4.4	mA
Front-end voltage gain	G_{V2}	V_{IN1} = 60 dBμ, 1635 kHz	19	24	29	dB
EIAJ output	V_E	V_{IN1} = 85 dBμ, 1635 kHz (1 kHz, 30% MOD) R_L = 8Ω THD10%	1.67 (350)	2.08 (540)		V (mW)
Attenuation (1)	AT1	V_{IN1} = 85 dBμ, 1635 kHz (1 kHz, 30% MOD) Difference in output levels between VOL MAX and center	5	12	17	dB
Overall distortion factor	THD	V_{IN1} = 95 dBμ, 1635 kHz (1 kHz, 30% MOD) V_E = 0.63V		0.6	2.75	%
Attenuation (2)	AT2	V_{IN1} = 85 dBμ, 1635 kHz (1 kHz, 30% MOD)		−80	−69	dBs
Overall noise level	AN	RF input shortcircuited, noise level for VOL MAX, V_{IN1} = OFF		−35	−9	dBs
Residual noise	N	AF input shortcircuited		−56	−49	dBs

Test Conditions

(Ta = 25°C, V_{CC} = 6V unless otherwise specified: See the test circuits.)

Item	Symbol	SW condition							Condition	Test point
		S1	S2	S3	S4	S5	S6	S7		
Circuit current	I_A	A	A	A	C	A	A	A	No signal	I_A
IF + AF (reduced voltage) Output level	V_{B1}	A	A	A	A	A	D	A	V_{IN2} = 29 dBμ, 455 kHz (1 kHz, 30% MOD) V_{CC} = 2V	V_B
IF + AF Voltage gain	G_{V1}	A	A	A	A	A	D	A	V_{IN2} = 29 dBμ, 455 kHz (1 kHz, 30% MOD)	V_B
Meter current	I_B	A	A	A	A	A	A	A	V_{IN2} = 85 dBμ, 455 kHz (1 kHz, 30% MOD)	I_B
Front-end voltage gain	G_{V2}	A	A	A	A	A	A	A	V_{IN1} = 60 dBμ, 1635 kHz	V_A
EIAJ output	V_E	B	B	A	A	A	B	A	V_{IN1} = 85 dBμ, 1635 kHz (1 kHz, 30% MOD) THD10%	V_B
Attenuation (1)	AT1	B	B	A	B	A	D C	A	V_{IN1} = 85 dBμ, 1635 kHz (1 kHz, 30% MOD)	V_B
Overall distortion factor	THD	B	B	A	A	A	B	A	V_{IN1} = 95 dBμ, 1635 kHz (1 kHz, 30% MOD) V_E = 0.63V	V_B
Attenuation (2)	AT2	B	B	A	A	A	A	A	V_{IN1} = 85 dBμ, 1635 kHz (1 kHz, 30% MOD)	V_B
Overall noise level	AN	B	B	A	A	A	C	B	Shortcircuited with an RF input-capacitor, V_{IN1} = OFF	V_B
Residual noise	N	B	B	A	C	A	D	B	Shortcircuited with an AF input capacitor	V_B

Test Circuit



* EIAJ output and overall distortion factor are adjusted on measurement.

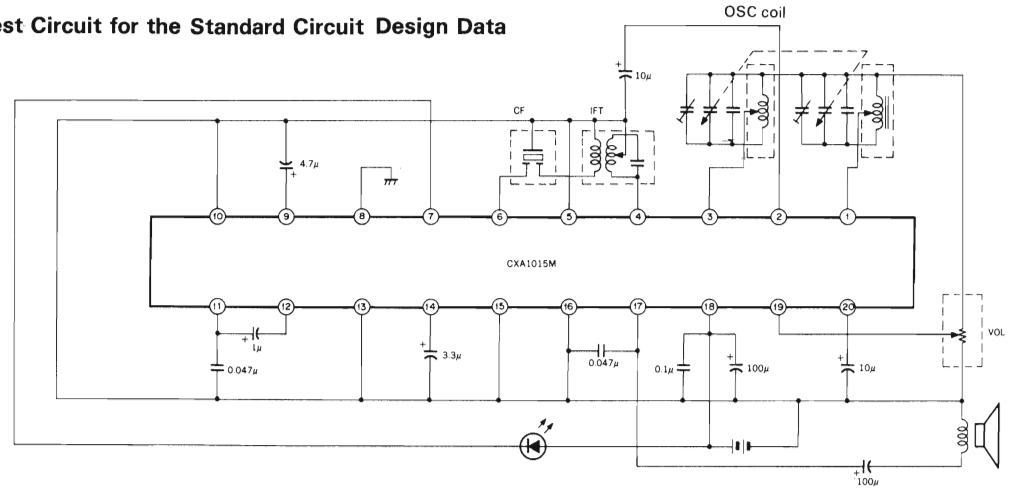
Standard Circuit Design Data

- Pin voltage

No.	3V	6V	No.	3V	6V
1	1.25	1.25	11	1.35	1.35
2	1.25	1.25	12	0.69	0.69
3	1.25	1.25	13	GND	GND
4	0	0	14	1.5	3.0
5	0	0	15	GND	GND
6	0	0	16	GND	GND
7	1.6	4.5	17	1.5	3.0
8	GND	GND	18	Vcc	Vcc
9	1.35	1.35	19	1.25	1.25
10	GND	GND	20	2.7	5.4

Note) 1. All values are given as standard values.
2. Measurement was carried out at the no-signal and VOL MIN state using the synthesizer circuit.

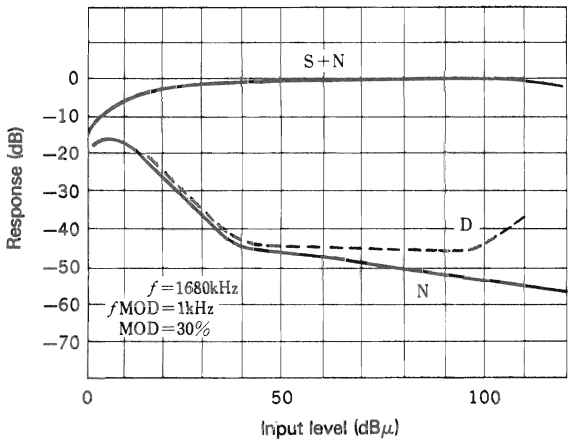
Test Circuit for the Standard Circuit Design Data



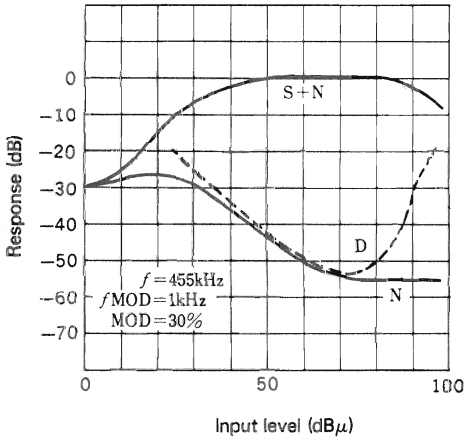
Note) Pin 8 and 13 are grounded.

CF AM 455 kHz CF
IFT AM 455 kHz IFT
OSC AM OSC

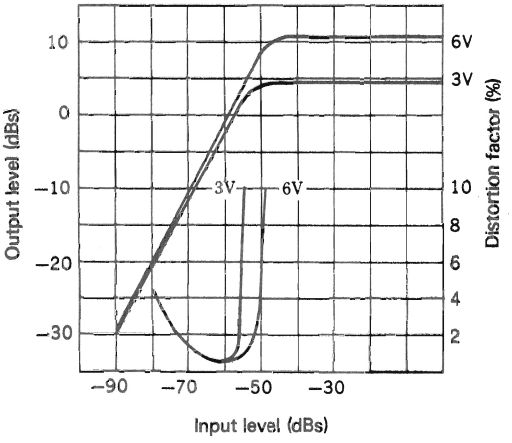
AM I/O Characteristics



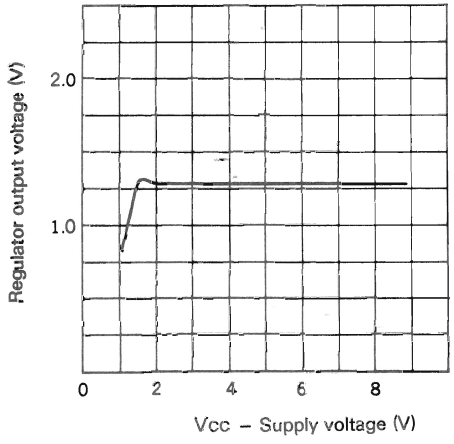
AM IF I/O Characteristics



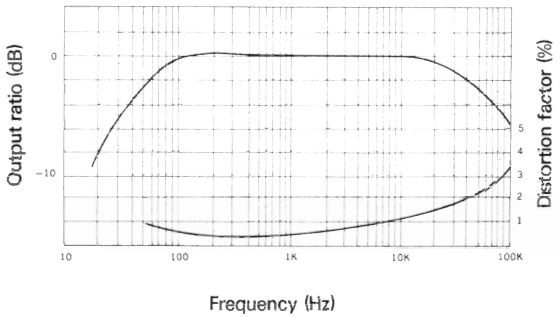
AF I/O Characteristics



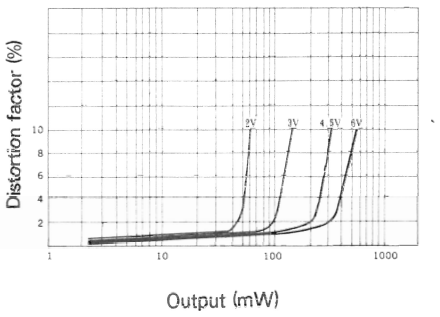
Regulator output vs. Supply voltage



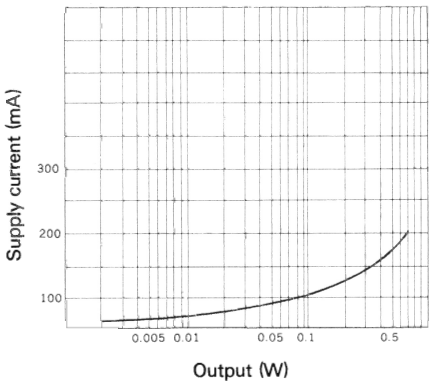
AF Stage frequency characteristics



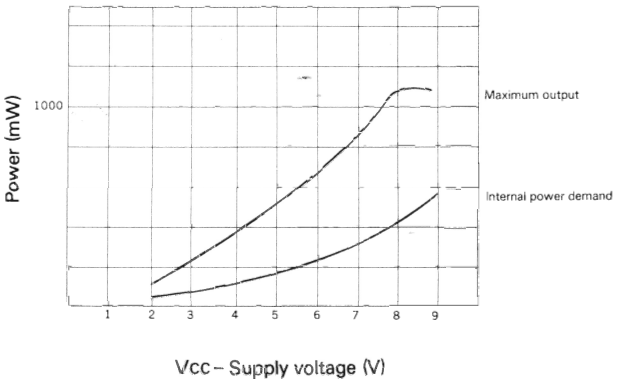
Distortion factor vs. AF Stage output



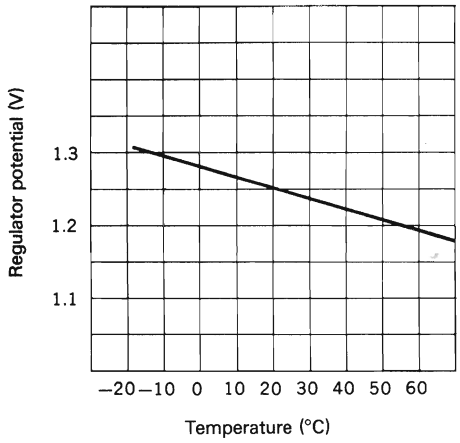
Supply current vs. Output



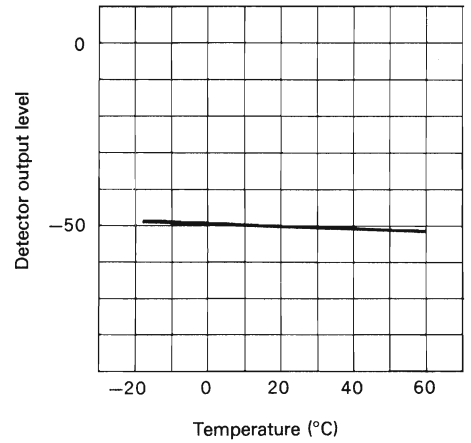
Maximum output and Internal power demand vs. Supply voltage



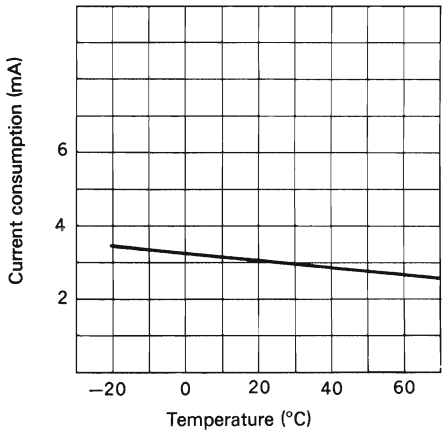
Temperature characteristics of regulator



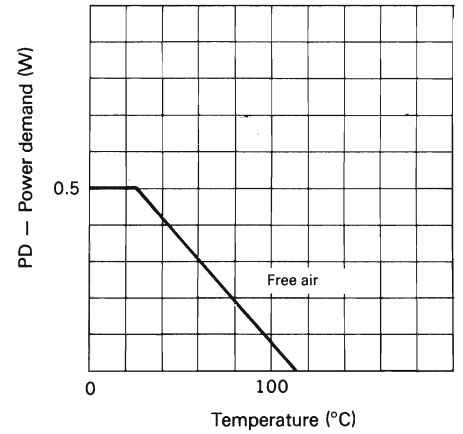
Temperature characteristics of detector output



Temperature characteristics of current consumption



Declining curve of maximum power demand



AM Stereo Radio

Description

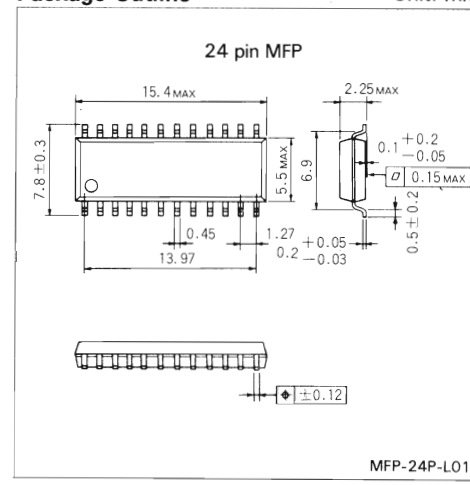
The CXA1017M is an IC for use with AM stereo radio, with an AM stereo system identification and audio signal processing functions integrated.

Features

- It identifies all AM stereo broadcasting systems (Magnavox, Kahn, Motorola and Harris) and switching the reception mode automatically.
- By employing a PLL (Phase Locked Loop) pilot detection circuit and safety logic circuit, single channel interference or malfunction due to I.P.M. (Incidental Phase Modulation) is eliminated.
- System identification time is minimized to about one second.
- Single adjustment (using a semi-fixed resistor for VCO).
- Few peripheral parts required.
- High S/N ratio and low distortion factor.

Package Outline

Unit: mm



Functions

- PLL pilot detection circuit
- PSN (90° Phase Shift Network)
- Matrix circuit
- Malfunction preventive circuit
- Mute control output
- LED driver

Structure

Bipolar silicon monolithic IC

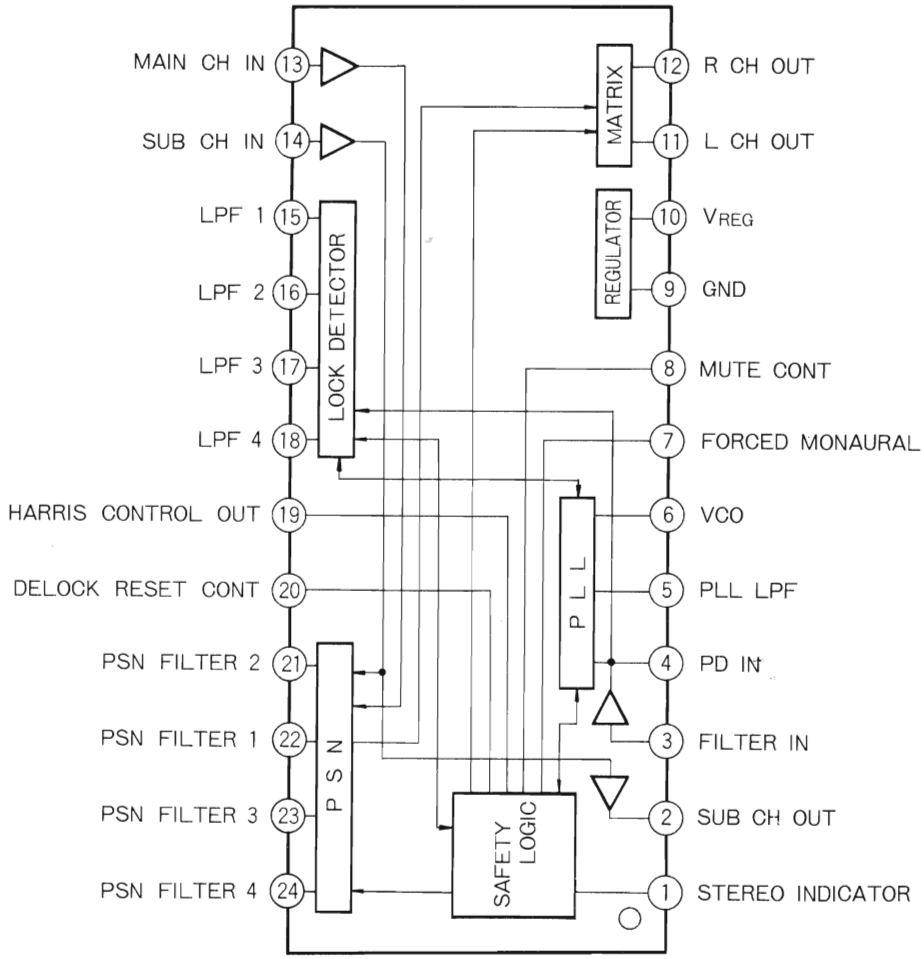
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	9	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	524	mW

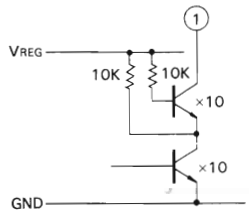
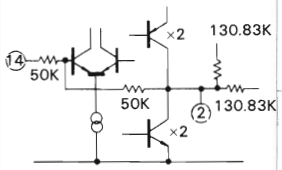
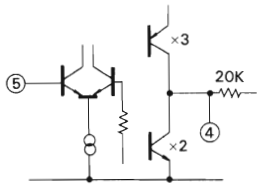
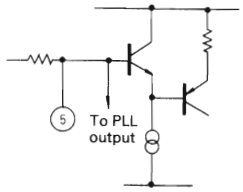
Recommended Operating Condition

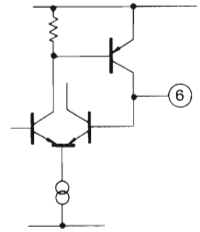
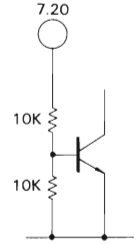
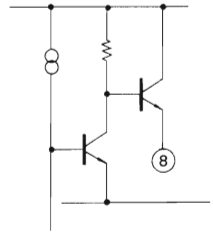
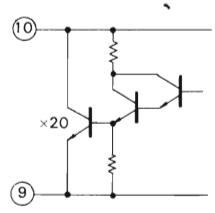
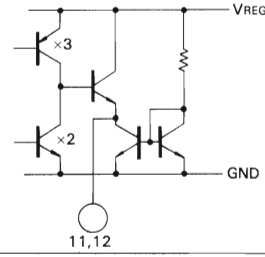
• Supply voltage	Vcc	5 to 8.5	V

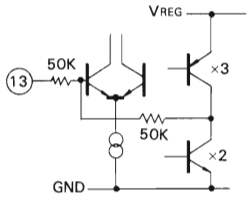
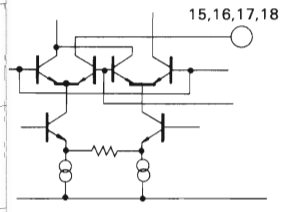
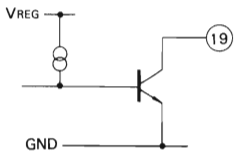
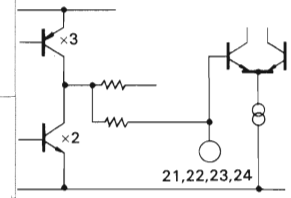
Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Symbol	Equivalent circuit	Voltage (V) (Typ.)	Description
1	STEREO INDICATOR		8.0	LED drive circuit
2	SUB CH OUT		1.5	Buffer (0dB) output from Pin 16 (Sub ch IN)
14	SUB CH IN		1.5	L−R+ pilot signal input circuit
3	FILTER IN		1.5	For pilot detection OP amplifier input for LPF
4	PD IN		1.5	OP amplifier output for LPF
5	PLL LPF		2.7	LPF for multi-PLL

No.	Symbol	Equivalent circuit	Voltage (V) (Typ.)	Description
6	VCO		2.8	For time constant of VCO for PLL
7	FORCED MONAURAL		0	Forced monaural reception with Hi-level pin input
20	LOCK OFF RESET CONT		0	Forced monaural reception with Low-level pin input
8	MUTE CONT		0	About ±18 ms 3.3 V pulse is generated mainly the moment matrix and PSN circuits are switched on or off.
9	GND		GND	
10	VREG		4.0	4V (typ.) of a regulator output is obtained from Vcc via RREG.
11	LCH OUT		1.5	Lch signal output
12	RCH OUT		1.5	Rch signal output

No.	Symbol	Equivalent circuit	Voltage (V) (Typ.)	Description
13	MAIN CH IN		1.5	L + R signal input circuit
15	LPF 1		3.0	LPF for Harris detection comparator
16	LPF 2		3.0	LPF for Motorola detection comparator
17	LPF 3		3.0	LPF for Kahn detection comparator
18	LPF 4		3.0	LPF for Magnavox detection comparator
19	HARRIS CONT		2.2	Current is drawn for Harris reception
21	PSN FILTER 2		1.5	Capacitor for PSN filter is connected (1000PF)
22	PSN FILTER 1		1.5	Capacitor for PSN filter is connected (10000PF)
23	PSN FILTER 3		1.5	Capacitor for PSN filter is connected (10000PF)
24	PSN FILTER 4		1.5	Capacitor for PSN filter is connected (1000PF)

Electrical Characteristics (Ta = 25°C)

* Input systems MOT: Motorola HAR: Harris
MAG: Magnavox KAH: Kahn

(Vcc = 8V unless otherwise specified)

No.	Item	Symbol	* Input system	Switch conditions, Mark: ON for the number								Test	Min.	Typ.	Max.	Unit
				1	2	3	4	5	6	7	8					
1	VREG Voltage (L)	M9			A	B	A	B	B	A	B	Measure with Vcc at 5V during no signal	3.5	4.0	4.5	V
2	VREG Voltage (H)	M9			B							Measure with Vcc at 10V during no signal	3.5	4.0	4.5	V
3	VREG Voltage (M)	M9			C							Measure with Vcc at 8V during no signal	3.5	4.0	4.5	V
4	OFF CHECK1 (ST)	M5											7.9	8.0	8.1	V
5	OFF CHECK1 ($\overline{\text{HAR}}$)	M6											3.9	4.0	4.1	V
6	OFF CHECK1 (MUTE)	M8											−0.1	0	0.1	V
7	Check VCO operation	M7										Measure with Vcof = 33kHz by changing V↑ with VH = 2.75V, VL = 2.55V, VM = 2.65V	33.0 32.0		34.0 33.0	kHz
8	VCO oscillation level check	M7							↓		↓	Measure by controlling V↑ DC so M7 output frequency becomes 33kHz	0.5	0.7	0.9	V
9	ST IND CHECK	M5	MOT			↓		↓	A		A	Input −53dBm pilot signal (f = 250Hz) (until measuring point DC becomes less than 0.6V)	0		0.6	V
10	STR output level (R)	M11	MOT			A		A		↓		Rch output when −26dBm (f = 1kHz) signal is input simultaneously with the pilot signal	−23	−20	−17	dBm
11	STR output level (L)	M10	MOT							B		Lch output when −26dBm (f = 1kHz) signal is input simultaneously with the pilot signal	−23	−20	−17	dBm
12	STR separation (R)	M11	MOT							A		Rch separation when −26dBm (f = 1kHz) signal is input simultaneously with the pilot signal	23			dB
13	STR separation (L)	M10	MOT							B		Lch separation when −26dBm (f = 1kHz) signal is input simultaneously with the pilot signal	23			dB
14	STR distortion factor (R)	M11	MOT							A		Rch distortion factor when −26dBm (f = 1kHz) signal is input simultaneously with the pilot signal			1.1	%
15	STR distortion factor (L)	M10	MOT			↓		↓		B		Lch distortion factor when −26dBm (f = 1kHz) signal is input simultaneously with the pilot signal			1.1	%
16	F-MONO operation 1 (MOT)	M3	MOT	ON		B		B		A			7.9	8.0	8.1	V
17	F-MONO operation 2 (MOT)	M5	MOT	↓									7.9	8.0	8.1	V
18	MUTE pulse check 1	M8	MOT									Check if M8 outputs pulse more than 3V	0		11	ms
19	MUTE pulse check 2	M8	MOT									Check if M8 outputs pulse more than 3V	18		55	ms
20	Lock R operation 1	M3	MOT									Check if M3 becomes Hi by making C1 at 3V	7.9	8.0	8.1	V
21	Lock R operation 2	M5	MOT									Check if M5 becomes Hi by making C1 at 3V	7.9	8.0	8.1	V
22	MUTE pulse check 3	M8	MOT									Check if M8 outputs pulse more than 3V	0		11	ms
23	ST IND CHECK	M5	MAG			↓		↓				Input −39dBm (f = 50Hz) pilot signal (until test point DC becomes less than 0.6V)	0		0.6	V
24	STR output level (R)	M11	MAG			A		A		↓		Rch output when −26dBm (f = 1kHz) signal is input simultaneously with pilot signal	−23	−20	−17	dBm
25	STR output level (L)	M10	MAG							B		Lch output when −26dBm (f = 1kHz) signal is input simultaneously with pilot signal	−23	−20	−17	dBm
26	STR separation (R)	M11	MAG							A		Rch separation when −26dBm (f = 1kHz) signal is input simultaneously with pilot signal	23			dB
27	STR separation (L)	M10	MAG							B		Lch separation when −26dBm (f = 1kHz) signal is input simultaneously with pilot signal	23			dB
28	STR distortion factor (R)	M11	MAG							A		Rch distortion factor when −26dBm (f = 1kHz) signal is input simultaneously with pilot			1.1	%
29	STR distortion factor (L)	M10	MAG			↓				B		Lch distortion factor when −26dBm (f = 1kHz) signal is input simultaneously with pilot			1.1	%
30	F-MONO operation 1 (MAG)	M2	MAG	ON		B				A			7.9	8.0	8.1	V
31	F-MONO operation 2 (MAG)	M5	MAG	↓	↓	↓	↓	↓	↓	↓	↓		7.9	8.0	8.1	V

Electrical Characteristics (Ta=25°C)

* Input systems MOT: Motorola HAR: Harris
MAG: Magnavox KAH: Kahn

(Vcc = 8V unless otherwise specified)

No.	Item	Symbol	* Input system	Switch conditions, Mark: ON for the number								Test	Min.	Typ.	Max.	Unit
				1	2	3	4	5	6	7	8					
32	MUTE pulse check 1	M8	MAG		C	B	A	A	A	A	A	Check if M8 outputs pulse more than 3V	0		11	ms
33	MUTE pulse check 2	M8	MAG		↓	↓	↓	↓	↓	↓	↓	Check if M8 outputs pulse more than 3V	18		55	ms
34	Lock-R operation 1 (MAG)	M2	MAG		↓	↓	↓	↓	↓	↓	↓	Check if M2 becomes Hi by making C1 3V	7.9	8.0	8.1	V
35	Lock-R operation 2 (MAG)	M5	MAG		↓	↓	↓	B	↓	↓	↓	Check if M2 becomes Hi by making C1 3V	7.9	8.0	8.1	V
36	MUTE pulse check 3	M8	MAG		↓	↓	↓	↓	↓	↓	↓	Time before pulse of more than DC=3V is output when C1 is made 3V	0		11	ms
37	MONO output level (R)	M11			↓	A	↓	↓	B	↓	B	Rch output when −26dBm (f=1kHz) signal is input	−29	−26	−23	dBm
38	MONO output level (L)	M10			↓	↓	↓	↓	↓	↓	↓	Lch output when −26dBm (f=1kHz) signal is input	29	−26	−23	dBm
39	MONO distortion factor (R)	M11			↓	↓	↓	↓	↓	↓	↓	Rch distortion factor when −26dBm (f=1kHz) signal is input			1.1	%
40	MONO distortion factor (L)	M10			↓	↓	↓	↓	↓	↓	↓	Lch distortion factor when −26dBm (f=1kHz) signal is input			1.1	%
41	ST IND CHECK	M5	HAR		↓	B	↓	↓	A	↓	A	Input −38dBm (f=550Hz) pilot signal (until measuring point DC becomes less than 0.6V)	0		0.6	V
42	HAR CONT operation	M6	HAR		↓	↓	↓	↓	↓	↓	↓	Input −38dBm (f=550Hz) pilot signal (until measuring point DC becomes less than 0.6V)	0		0.6	V
43	STR output level (R)	M11	HAR		↓	A	↓	A	↓	↓	↓	Rch output when −26dBm (f=1kHz) signal is input (until similar condition as above met)	−23	−20	−17	dBm
44	STR output level (L)	M10	HAR		↓	↓	↓	↓	↓	↓	B	Lch output when −26dBm (f=1kHz) signal is input (until similar condition as above met)	−23	−20	−17	dBm
45	STR separation (R)	M11	HAR		↓	↓	↓	↓	↓	↓	A	Rch separation when −26dBm (f=1kHz) signal is input with similar condition as above	23			dB
46	STR separation (L)	M10	HAR		↓	↓	↓	↓	↓	↓	B	Lch separation when −26dBm (f=1kHz) signal is input with similar condition as above	23			dB
47	STR distortion factor (R)	M11	HAR		↓	↓	↓	↓	↓	↓	A	Rch distortion factor with −26dBm (f=1kHz) signal is input with similar condition as above			1.1	%
48	STR distortion factor (L)	M10	HAR		↓	↓	↓	↓	↓	↓	B	Lch distortion factor with −26dBm (f=1kHz) signal is input with similar condition as above			1.1	%
49	F-MONO operation 1 (HAR)	M4	HAR		↓	B	↓	B	↓	↓	A	Check if M4 becomes Hi when S1 is set to ON	7.9	8.0	8.1	V
50	F-MONO operation 2 (HAR)	M5	HAR		↓	↓	↓	↓	↓	↓	↓	Check if M5 becomes Hi when S1 is set to ON	7.9	8.0	8.1	V
51	MUTE pulse check 1	M8	HAR		↓	↓	↓	↓	↓	↓	↓	Time before pulse more than DC=3V is output right after S1 is set to ON	0		11	ms
52	MUTE pulse check 2	M8	HAR		↓	↓	↓	↓	↓	↓	↓	Time before pulse more than DC=3V is output right after S1 is set to OFF	18		55	ms
53	Lock-R operation 1 (HAR)	M4	HAR		↓	↓	↓	↓	↓	↓	↓	Check if M4 becomes Hi by making C1 3V	7.9	8.0	8.1	V
54	Lock-R operation 2 (HAR)	M5	HAR		↓	↓	↓	↓	↓	↓	↓	Check if M4 becomes Hi by making C1 3V	7.9	8.0	8.1	V
55	MUTE pulse check 3	M8	HAR		↓	↓	↓	↓	↓	↓	↓	Time before pulse more than DC=3V is output right after C1 is set to 3V	0		11	ms
56	ST IND CHECK	M5	KAH		↓	↓	↓	↓	↓	↓	↓	Input −52dBm (f=150Hz) pilot signal (until measuring point DC becomes less than 0.6V)	0		0.6	V
57	KAH output level (R)	M11	KAH		↓	A	B	A	↓	↓	↓	Rch output when −26dBm (f=1kHz) signal is input until condition as above is met	−23	20	17	dBm
58	KAH output level (L)	M10	KAH		↓	↓	↓	↓	↓	↓	B	Lch output when −26dBm (f=1kHz) signal is input until condition as above is met	−23	20	17	dBm
59	KAH separation (R)	M11	KAH		↓	↓	↓	↓	↓	↓	A	Rch output when −26dBm (f=1kHz) signal is input until condition as above is met	23			dB
60	KAH separation (L)	M10	KAH		↓	↓	↓	↓	↓	↓	B	Lch output when −26dBm (f=1kHz) signal is input until condition as above is met	23			dB
61	KAH distortion factor (R)	M11	KAH		↓	↓	↓	↓	↓	↓	A	Rch distortion factor when −26dBm (f=1kHz) signal is input until condition as above is met			1.1	%
62	KAH distortion factor (L)	M10	KAH		↓	↓	↓	↓	↓	↓	B	Lch distortion factor when −26dBm (f=1kHz) signal is input until condition as above is met			1.1	%

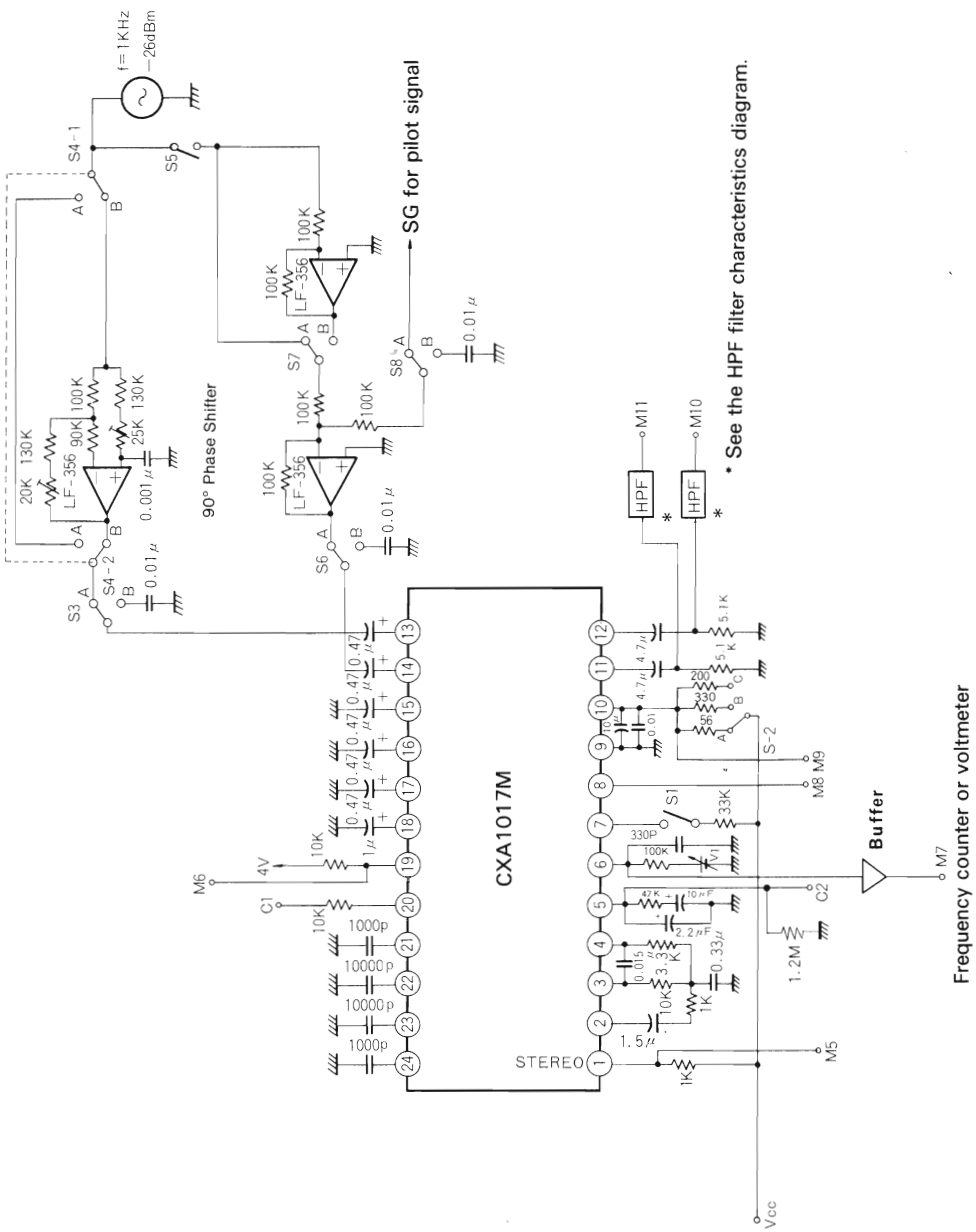
Electrical Characteristics (Ta=25°C)

* Input systems MOT: Motorola HAR: Harris
MAG: Magnavox KAH: Kahn

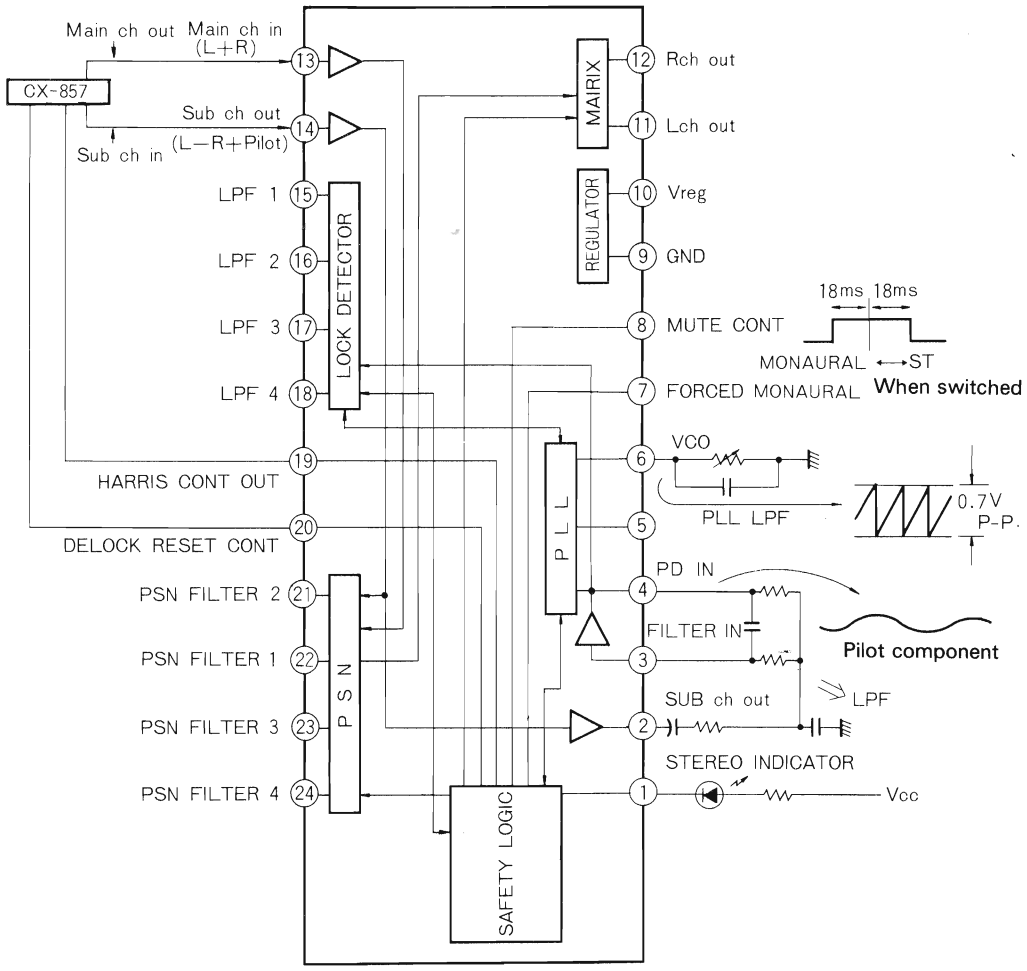
(Vcc = 8V unless otherwise specified)

No.	Item	Symbol	* Input system	Switch conditions, Mark: ON for the number								Test	Min.	Typ.	Max.	Unit
				1	2	3	4	5	6	7	8					
63	F-MONO operation 1 (KAH)	M1	KAH		C	B	A	B	A	A	A	Check if M1 becomes Hi when S1 is set to ON	7.9	8.0	8.1	V
64	F-MONO operation 2 (KAH)	M5	KAH		↓	↓	↓	↓	↓	↓	↓	Check if M5 becomes Hi when S1 is set to ON	7.9	8.0	8.1	V
65	MUTE pulse check 1	M8	KAH		↓	↓	↓	↓	↓	↓	↓	Time before pulse more than DC=3V is output when S1 is set to ON	0		11	ms
66	MUTE pulse check 2	M8	KAH		↓	↓	↓	↓	↓	↓	↓	Time before pulse more than DC=3V is output when S1 is set to OFF	18		55	ms
67	Lock-R operation 1 (KAH)	M1	KAH		↓	↓	↓	↓	↓	↓	↓	Check if M1 becomes Hi when C1 is set to 3V	7.9	8.0	8.1	V
68	Lock-R operation 2 (KAH)	M5	KAH		↓	↓	↓	↓	↓	↓	↓	Check if M5 becomes Hi when C1 is set to 3V	7.9	8.0	8.1	V
69	MUTE pulse check 3	M8	KAH		↓	↓	↓	↓	↓	↓	↓	Time before pulse more than DC=3V is output right after C1 is set to 3V	0		11	ms

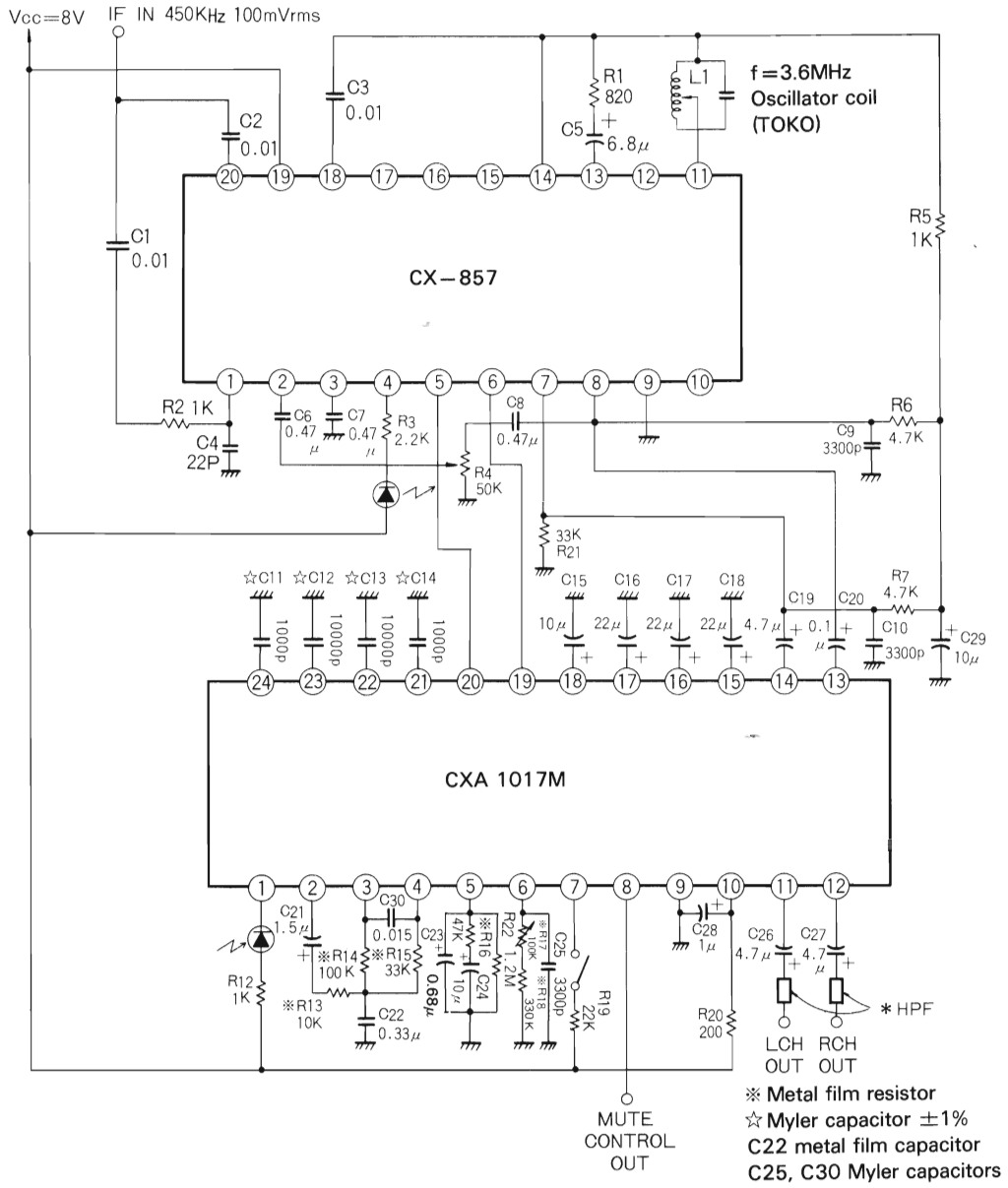
Electrical Characteristics Test Circuit



Application Circuit (1)

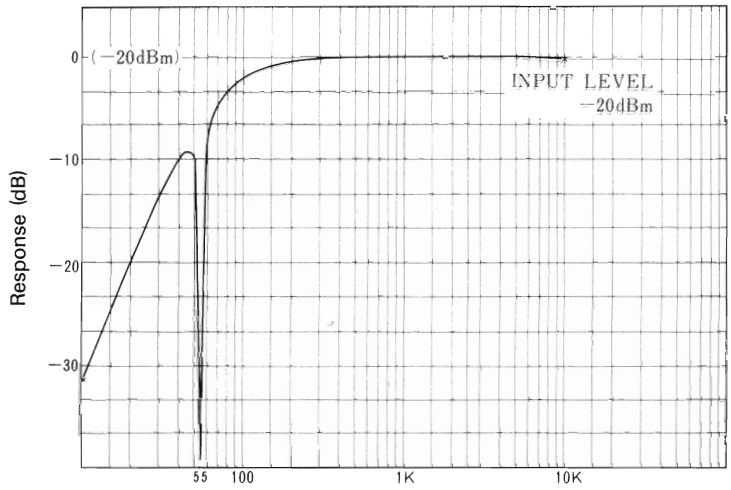


Application Circuit (2)

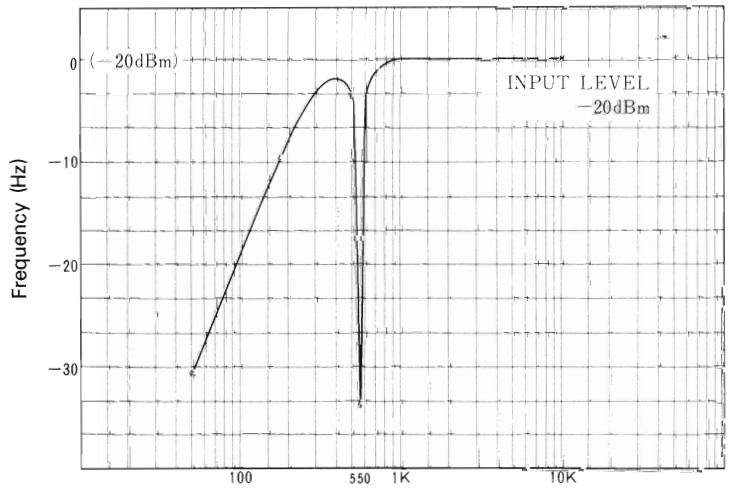


* See the HPF filter characteristics

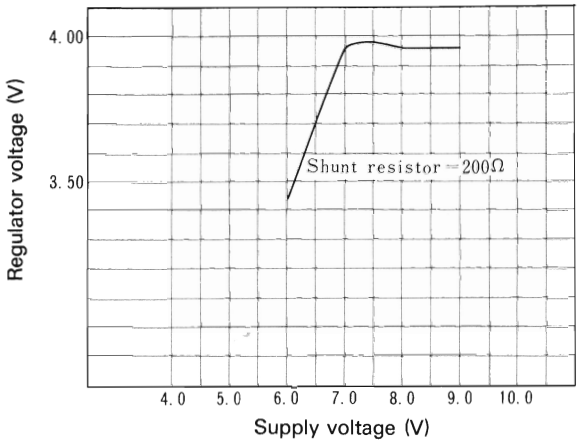
HPF filter characteristics



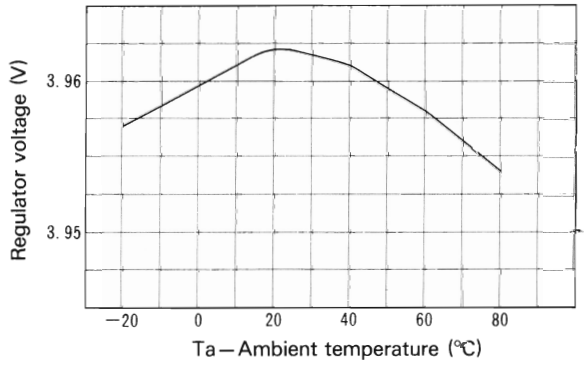
Filter frequency for characteristics evaluation



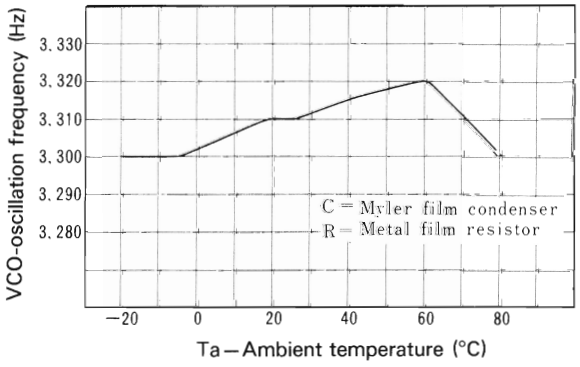
Shunt regulator characteristics



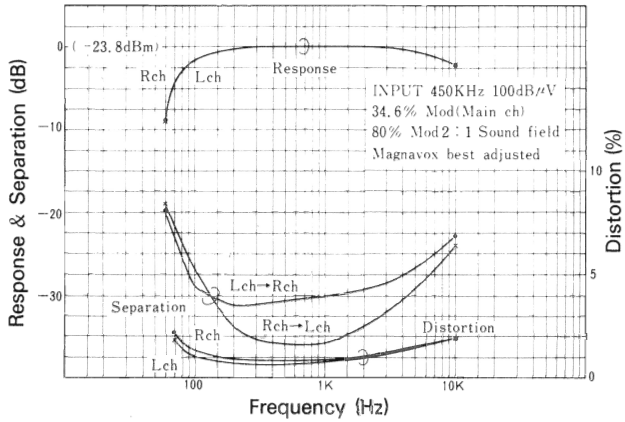
Regulator temperature characteristics



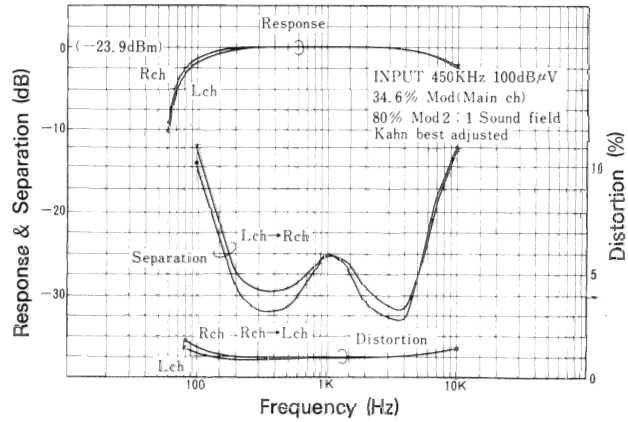
VCO Oscillation frequency temperature characteristics



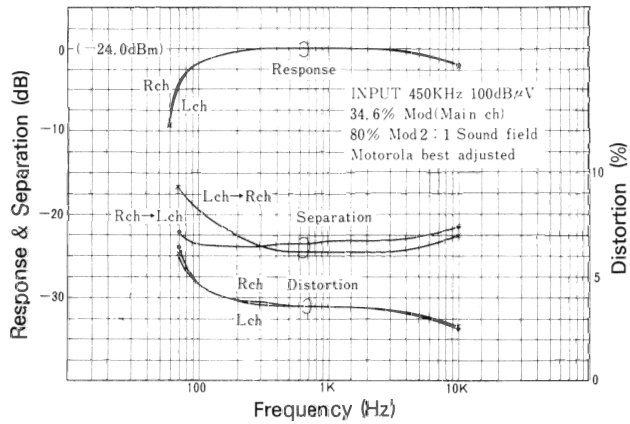
CX-857+CXA1017M (Magnavox mode)



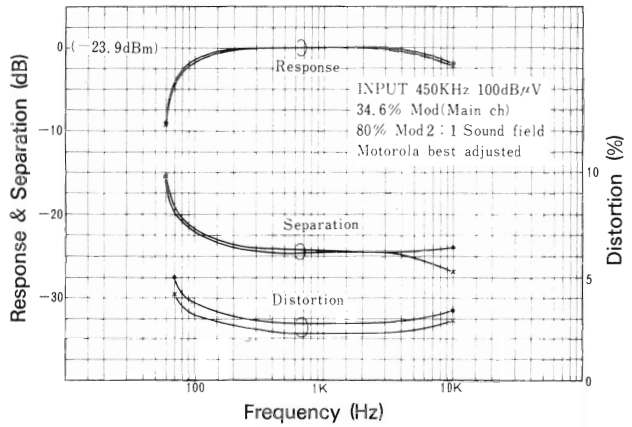
CX-857+CXA1017M (Kahn mode)



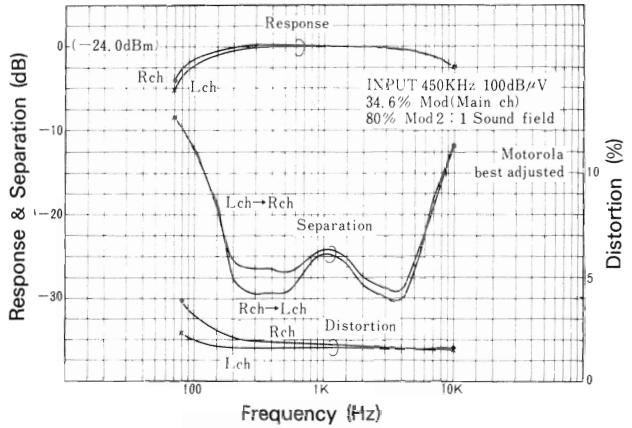
CX-857+CXA1017M (Motorola mode)



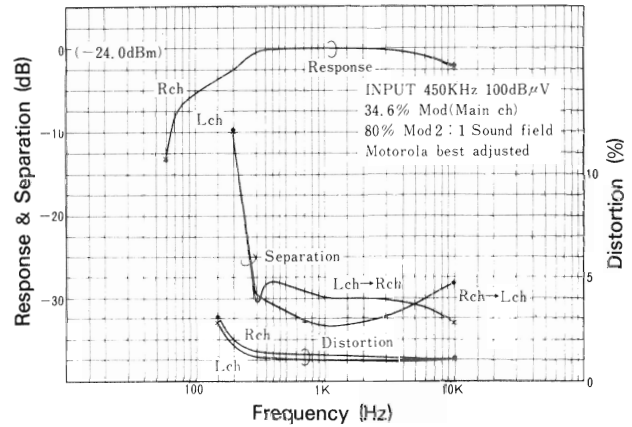
CX-857+CXA1017M (Magnavox mode)



CX-857+CXA1017M (Kahn mode)



CX-857+CXA1017M (Harris mode)



Pin Description of the Printed Circuit Board

IF IN : IF INPUT pin for the input of 450 kHz 100mVrms signal.

GND : Ground

Vcc : 8 V. Vary the R20 value of CX20177 (CXA1017M) in accordance with the shunt regulator. Since the shunt regulator output voltage (CX20177: Pin 12, CXA1017M: Pin 10) has been set at 4 V, set the R20 to satisfy the following.

$$\frac{Vcc - 4\ V}{R20} \geqq 15\ mA$$

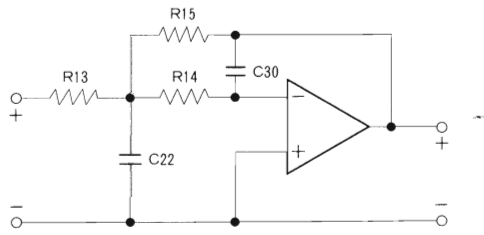
Rch, Lch : Rch, Lch output pin for the stereo signal. It is possible to drive up to about 0 dB_{10} with $R_L = 5\ k\Omega$.

MUTE : If generates a pulse (about 3.3 V) with the width of ±20 ms mainly at the time of switching between Monaural and Stereo and PSN switching between ON and OFF.

Forced Monaural Switch : Switching to ON enables reception of the monaural mode forcibly.

Operation of Main Parts

R1,C5 : CX-857 PLL LPF constant
R4 : Input level setting to the divider
C11 to C14 : Capacitor for PSN
C15 to C18 : Capacitor for Pilot lock detector
C21, 22, 30, R13 to R15 } Secondary Low pass active filter



C23, 24, R16, 22 } For PLL LPF of the CX20177
R17, 18, C25 } For VCO of the CX20177
R20 : Resistor for the shunt regulator

Adjustment and Check Methods of the AM Stereo Evaluation PCB

1. Adjustment method

Only three points are to be adjusted for the evaluation PCB.

1-1 Adjustment of the CX-857 VCO oscillation frequency
Input the non-modulated signal 450kHz 100mVrms (100 dBμ) through the IF IN pin printed on the PCB and turn the oscillation coil so the CX-857 Pin 13 DC voltage becomes 1.7 V.

1-2 Input level adjustment of the divider
Input the 450kHz 100mVrms with 45% modulation (Motorola mode) through IF and adjust R4 (VOL) so the Lch or Rch output distortion factor is minimized.

1-3 Adjustment of the CX20177 (CXA1017M) VCO oscillation frequency
Monitor the Vcc oscillation frequency and adjust R17 (VOL) so the frequency becomes 3,300Hz at the time of free run.

2. Operation check method of the CX20177 (CXA1017M)

The following is a simple check method to identify the system using the pilot signal.

2-1 Identification confirmation using the pilot signal
Input the pilot frequency signal through Pin 16 (Pin 14) via a capacitor. The frequency and signal level are as follows:

MAGNAVOX	5 Hz	−38 dBm
KAHN	15 Hz	−53 dBm
MOTOROLA	25 Hz	−52 dBm
HARRIS	55 Hz	−38 dBm

With input of the above signal, the LED indicator lights after a delay of about 1 sec. Simultaneously, about 40ms pulse (about 3.3 V) is output from the MUTE pin centering around the time when the audio block is switched.

In the HARRIS mode, Pin 21 (Pin 19) draws current and the CX-857 Pin 6 voltage enters Low level.

Note) When CX-857 is not locked (when the CX-857 lock LED is not lit with the input of a 450 kHz carrier to IF), the forcible monaural signal is output from CX-857 to CX-20177 (CXA1017M) (Pin 22 and 20 has entered low level). At this time, do not use the IF input but apply 3 V to Pin 22 and 20, in checking the above use CX20177 (CXA1017M) alone.

Parts List of the AM Stereo Standard Circuit

L1, 3.6 MHz, Oscillator coil (TOKO) 1-406-070-11

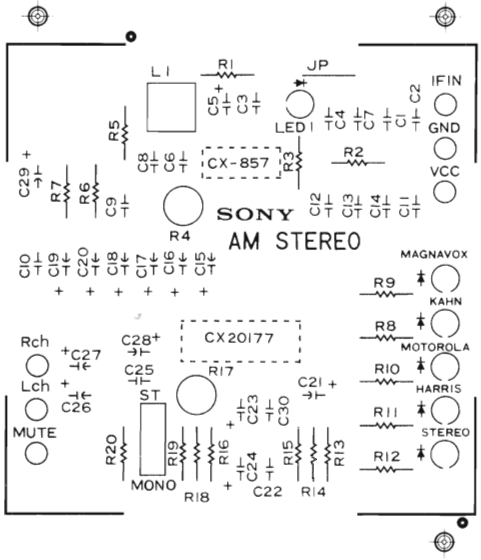
1) Resistor

R1	820Ω	Carbon	R12	1kΩ	Carbon
R2	1kΩ	Carbon	R13	10kΩ	Metal film
R3	2.2kΩ	Carbon	R14	100kΩ	Metal film
R4	50kΩ	Semi-fixed	R15	33kΩ	Metal film
R5	1kΩ	Carbon	R16	47kΩ	Metal film
R6	4.7kΩ	Carbon	R17	100kΩ	Metal film semi-fixed
R7	4.7kΩ	Carbon	R18	330kΩ	Metal film semi-fixed
R8	1kΩ	Carbon	R19	22kΩ	Carbon
R9	1kΩ	Carbon	R20	200Ω	Carbon
R10	1kΩ	Carbon	R21	33kΩ	Carbon
R11	1kΩ	Carbon	R22	1.2MΩ	Carbon

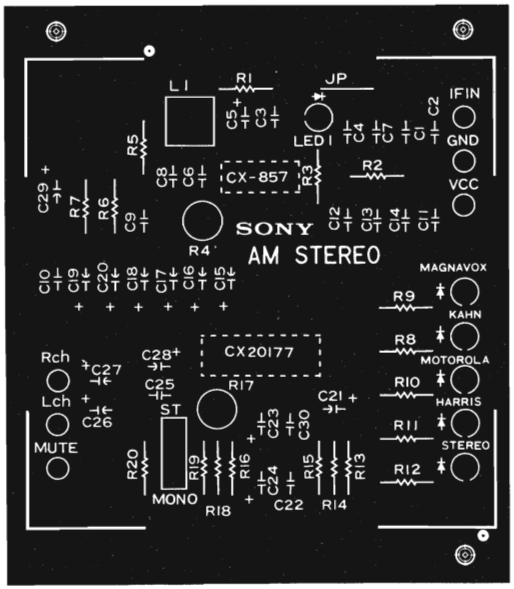
2) Capacitor

C1	0.01μF	Ceramic	C21	1.5μF	Electrolytic
C2	0.01μF	Ceramic	C22	0.33μF	Metal film
C3	0.01μF	Ceramic	C23	2.2μF	Tantalum
C4	22pF	Ceramic	C24	10μF	Tantalum
C5	6.8μF	Tantalum	C25	3300pF	Myler
C6	0.47μF	Electrolytic	C26	4.7μF	Electrolytic
C7	0.47μF	Electrolytic	C27	4.7μF	Electrolytic
C8	0.47μF	Electrolytic	C28	1μF	Electrolytic
C9	3300pF	Ceramic	C29	10μF	Electrolytic
C10	3300pF	Ceramic	C30	0.015μF	Myler
C11	1000pF	Myler ±1%			
C12	10000pF	Myler ±1%			
C13	10000pF	Myler ±1%			
C14	1000pF	Myler ±1%			
C15	10μF	Electrolytic			
C16	22μF	Electrolytic			
C17	22μF	Electrolytic			
C18	22μF	Electrolytic			
C19	4.7μF	Electrolytic			
C20	0.1μF	Electrolytic			

Silk Diagram



Pattern Diagram



SONY CXA1019M/CXA1019P

FM/AM Radio

Description

CXA1019M/1019P is a one-chip FM/AM Radio IC designed for radio-cassette tape recorders and headphone tape recorders, and has the following functions.

Features

- Small number of peripheral components
- Low current consumption (V_{CC}=3V)
  For FM: I_D=53 mA (typ.)
  For AM: I_D=3.4 mA (typ.)
- Built-in FM/AM select switch
- Large output of AF amplifier
  V_{CC}=6V, EIAJ output=500 mW (typ.) when V_{CC}=6V. load impedance 8Ω

Functions

FM section

- RF amplifier, Mixer, OSC (incorporating AFC variable capacitor)
- IF amplifier
- Quadrature detection
- Tuning LED driver

AM section

- RF amplifier, Mixer OSC (with RF AGC)
- IF amplifier (with IF AGC)
- Detector
- Tuning LED driver

AF section

- Electronic volume control

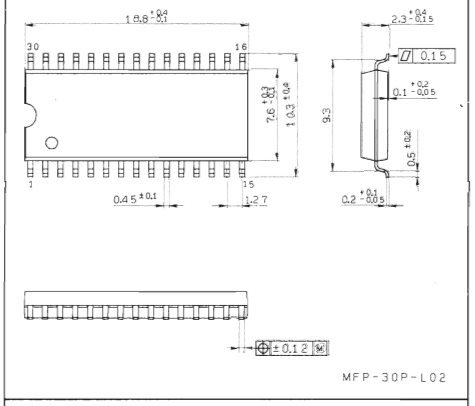
Structure

Bipolar silicon monolithic IC

Package Outline

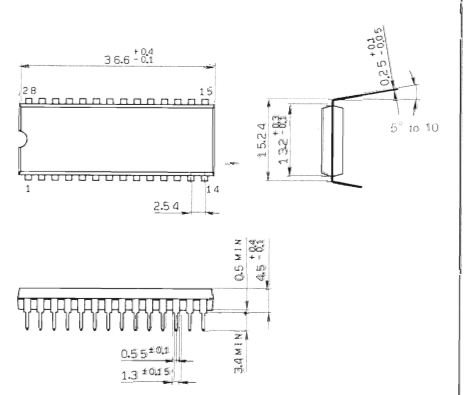
Unit: mm

CXA1019M 28 pin MFP



MFP-30P-L02

CXA1019P 28 pin DIP



DIP-28P-02

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}		9	V
• Operating temperature	Topr		−10 to +60	°C
• Storage temperature	Tstg		−50 to +125	°C
• Junction temperature	Tjmax		150	°C
• Allowable Power dissipation	P_D	CXA1019M	700	mW
		CXA1019P	1000	mW

Recommended Operating Conditions

• Supply voltage	V_{CC}	2 to 7.5	V (CXA1019M)
	V_{CC}	2 to 8.5	V (CXA1019P)

Block Diagram

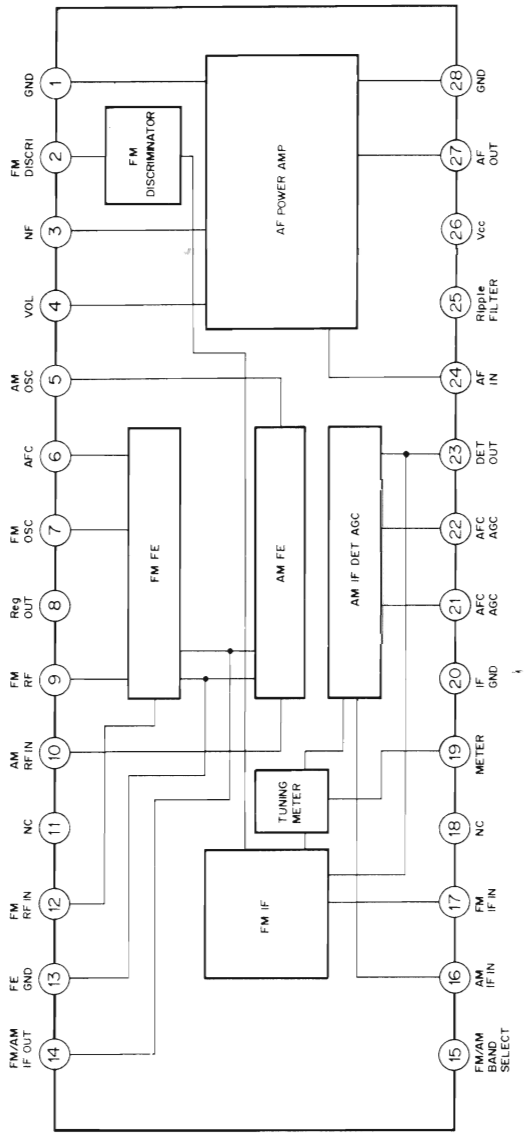
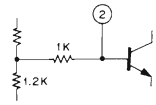
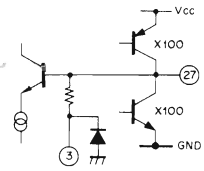
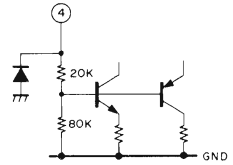
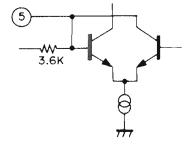
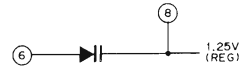
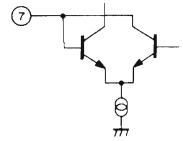
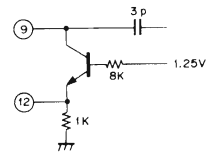
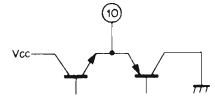
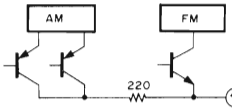
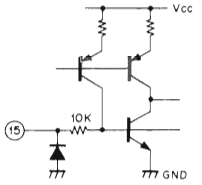
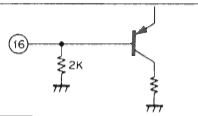
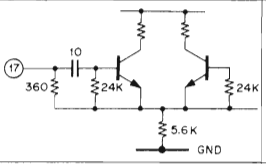
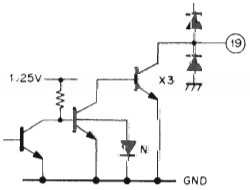
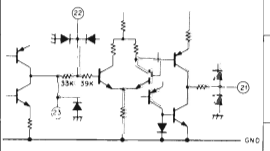
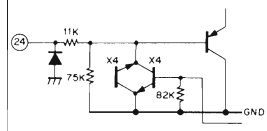
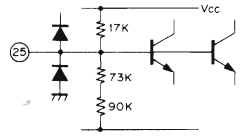


Fig. 1

Standard Circuit Design Data

No.	Symbol	Voltage (V)				Equivalent circuit	Description
		V_{CC}=3V		V_{CC}=6V			
		FM	AM	FM	AM		
1	GND	0	0	0	0		
2	FM DISCRI	2.18	2.70	4.88	5.43		Phase-shift circuit Connect ceramic discriminator
3	NF	1.5	1.5	3.0	3.0		Negative feedback pin
27	AF OUT	1.5	1.5	3.0	3.0		Power amplifier output pin
4	VOL CONT	1.25	1.25	1.25	1.25		Connect variable resistor for electronic volume control
5	AM OSC	1.25	1.25	1.25	1.25		AM local oscillation circuit
6	AFC	1.25	*	1.25	*		AFC variable capacitor pin
8	REG OUT	1.25	1.25	1.25	1.25		Regulator pin 1.25V (typ)
7	FM OSC	1.25	1.25	1.25	1.25		FM local oscillation circuit
9	FM RF	1.25	1.25	1.25	1.25		Connect FM RF tuning coil
12	FM RF IN	0.3	0	0.3	0		FM RF input pin
10	AM RF IN	1.25	1.25	1.25	1.25		AM RF input pin

No.	Symbol	Voltage (V)				Equivalent circuit	Description
		Vcc=3V		Vcc=6V			
		FM	AM	FM	AM		
11	NC	0	0	0	0		
13	GND (FE GND)	0	0	0	0		
14	FM/AM FE OUT	0.36	0.2	0.36	0.2		IF output pin of FM and AM Connect IF filter
15	BAND SELECT	0.84	0	0.88	0		FM and AM bands selection switch pin. During GND it becomes AM and during open it becomes FM.
16	AM IF IN	0	0	0	0		Input pin of AM IF
17	FM IF IN	0.34	0	0.88	0		Input pin of FM IF
18	NC	0	0	0	0		
19	METER	1.6	1.8	4.5	4.5		Meter drive circuit (For tuning indicator)
20	GND	0	0	0	0		
21	AFC/AGC	1.25	1.49	1.25	1.49		AFC pin of W band. During AM, it determines time constant of AGC.
22	AFC/AGC	1.25	1.12	1.25	1.15		AFC pin of J band. During AM, it determines time constant of AGC.
23	DET OUT	1.25	1.0	1.25	1.0		Detection output pin

No.	Symbol	Voltage (V)				Equivalent circuit	Description
		V_{CC}=3V		V_{CC}=6V			
		FM	AM	FM	AM		
24	AF IN	0	0	0	0		Power amplifier input pin
25	RIPPLE FILTER	2.71	2.71	5.4	5.4		Ripple filter
26	V_{CC}	3.0	3.0	6.0	6.0		Power supply pin
28	GND	0	0	0	0		Power GND

***Note)** The pin voltage of pin 6 during AM, it is the same pin voltage of pin 22 during J BAND and is the same pin voltage of pin 21 during W BAND.

Electrical Characteristics

(Ta=25°C, V_{CC}=6V)

No.	Characteristic	Symbol	SW Status						Test Point	Condition	Min.	Typ.	Max.	Unit
			1	2	3	4	5	6						
1	AM Circuit Current	ID1	A	B	A	A	A	A	IA	No signal, AM	—	3.5	10.0	mA
2	FM Circuit Current	ID2	A	B	A	A	B	A	IA	No signal, FM	—	7.0	14.0	mA
3	FM Front End Voltage Gain	GV1	A	B	A	A	B	A	VA	V_{IN1}=40dBu, 100MHz	32	39	46	dB
4	FM Detection Output Level	VD1	A	—	—	A	B	A	VD	V_{IN3}=90dBu, 10.7MHz (1kHz, 22.5kDEV)	−26.0	−20	−14.0	dBm
5	FM IF Knee Level	VD2	A	—	—	A	B	A	VD	V_{IN3} level at a point 3dB down from V_{IN3}=90dBμ, 10.7MHz (1kHz, 22.5kDEV)	—	24	32	dBμ
6	FM Detection Output Distortion Factor	THD1	A	—	—	A	B	A	VD	V_{IN3}=90dBu, 10.7MHz (1kHz 75kHz DEV)	—	0.3	2.0	%
7	FM Meter Current	IB1	A	—	—	A	B	A	IM	V_{IN3}=60dBu, 10.7MHz	1.8	3.5	7.0	mA
8	AM Front End Voltage Gain	GV2	A	A	A	A	A	A	VB	V_{IN2}=60dBu, 1660kHz	15	22	29	dB
9	AM IF Voltage Gain	GV3	A	A	—	A	A	A	VD	V_{IN4} when 455kHz (1kHz 30% MOD) output is −34dBm	14	20	27	dBμ
10	AM Detection Output Level	VD3	A	A	—	A	A	A	VD	V_{IN4}=85dBu, 455kHz (1kHz, 30% MOD)	−26	−20	−14	dBm
11	AM Meter Current	IB2	A	A	—	A	A	A	IM	V_{IN4}=85dBu, 455kHz (1kHz, 30% MOD)	1.3	3.0	7.0	mA
12	AM Detection Output Distortion Factor	THD2	A	A	B	B	A	A	VD	V_{IN2}=95dBu, 1660kHz (1kHz, 30% MOD) V_{CC}=7.8V	—	0.6	2.0	%
13	Audio Voltage Gain	GV4	A	—	—	—	—	B	VE	$V_{IN54Z110}$=−0dBm, 1kHz	27	31.5	36	dB
14	Audio Distortion Factor	THD3	A	—	—	—	—	B	VE	Distortion factor for output of 50mW V_{IN5}=20dBm, 1kHz	—	0.3	2.5	%

0 dBm=0.775V rms

SONY®

Electrical Characteristic Test Circuit

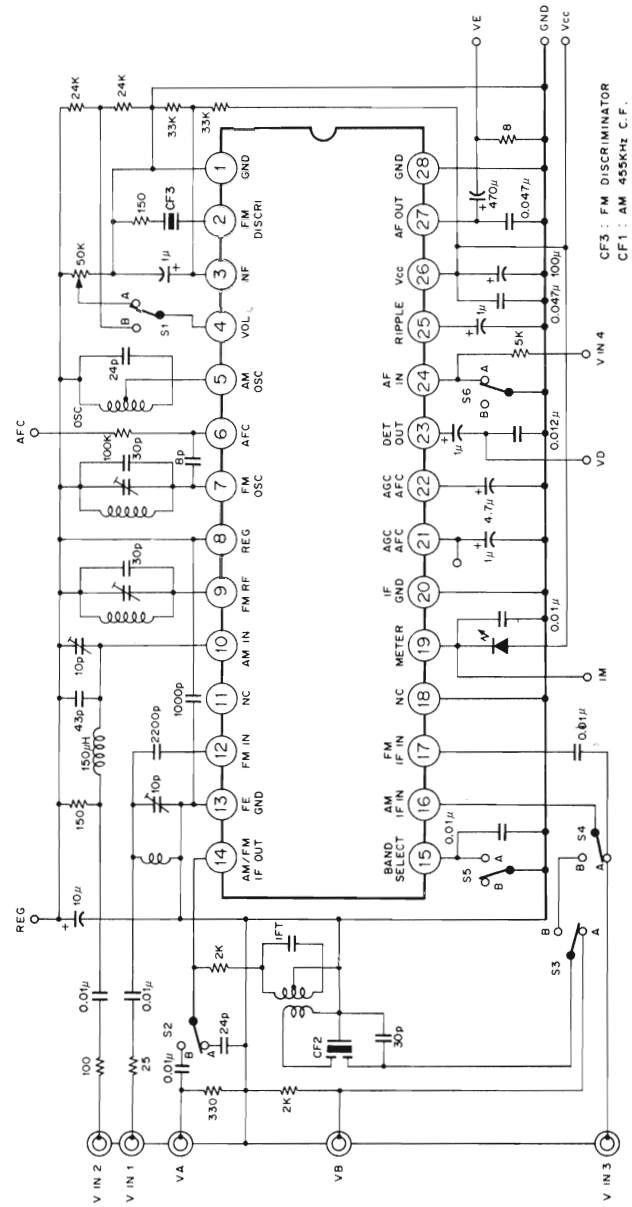
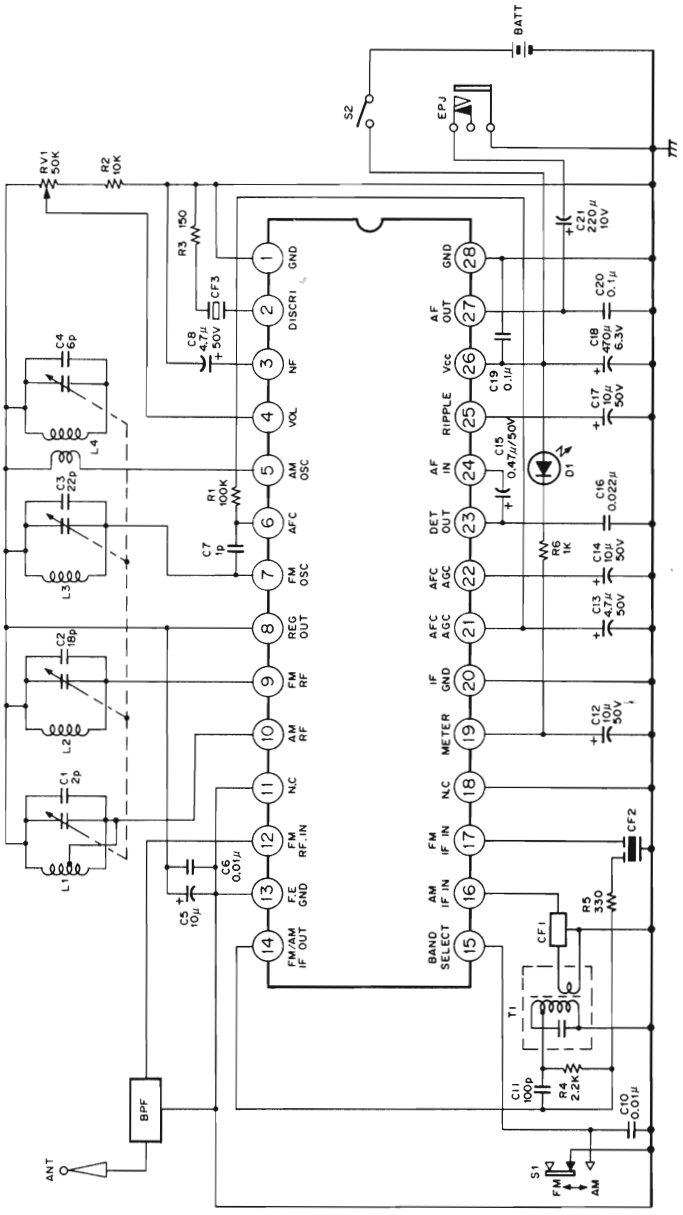


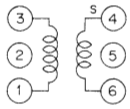
Fig. 2

Application Circuit



Coil data

AM OSC

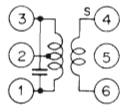


Core diameter ϕ0.06 mm 2UEW

f(kHz)	L(μH) 1 to 3	Qo 1 to 3	Number of windings t	
			1 to 3	4 to 6
796	270	125	107	29

Equivalent to L-5K7-H5 Mitsumi Electric Co., Ltd.
or 7TRS-8441 TOKO Co., Ltd.

AM IFT

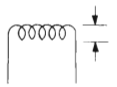


Core diameter ϕ0.07 mm UEW

Co(pF) 1 to 3	Qo 1 to 3	Number of windings t		
		1 to 2	2 to 3	4 to 6
180	90	111	35	7

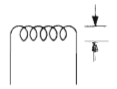
Equivalent to 21K7-H5 Mitsumi Electric Co., Ltd.
or 7MC-7789N TOKO Co., Ltd.

FM RF



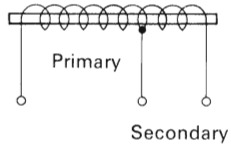
ϕ4 mm
ϕ0.6 mm 4.5t

FM OSC



ϕ4 mm
ϕ0.6 mm 3.5t

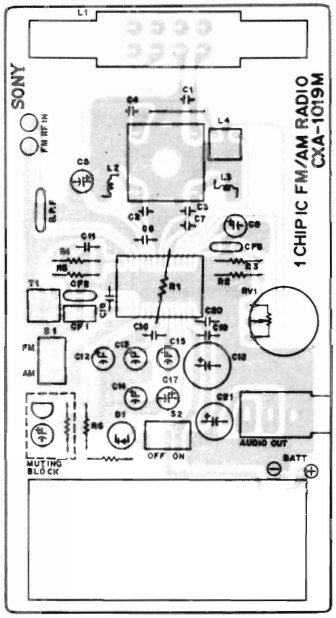
AM bar antenna



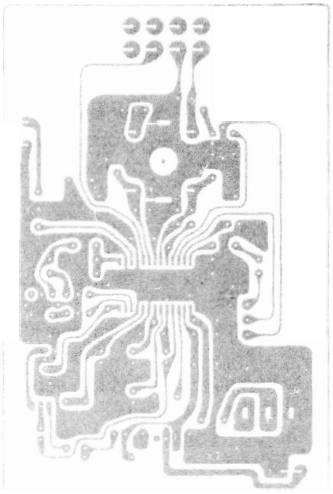
f(kHz)	L(μH)	Primary	Secondary
796	650	91t	20t

BPF	PFWE8 (88 to 108 MHz)	Soshin Electric Co., Ltd.
CF1	SFU-455B	Murata Mfg. Co., Ltd. or BFCFL-455 TOKO Co., Ltd.
CF2	SFE10.7MA5	Murata Mfg. Co., Ltd.
CF3	CDA10.7MC1	Murata Mfg. Co., Ltd.

CXA1019M Evaluation Board

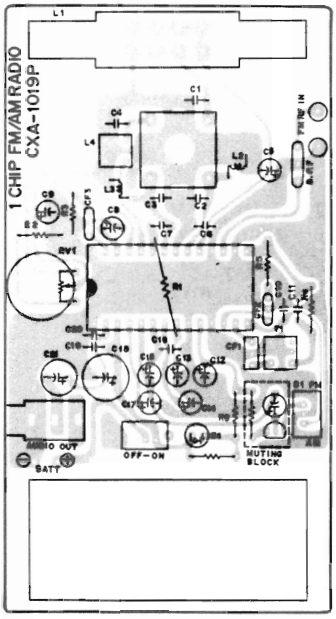


Parts arrangement diagram

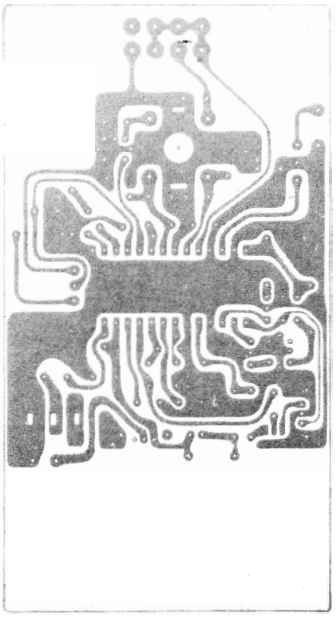


Pattern diagram

CXA1019P Evaluation Board



Parts arrangement diagram



Pattern diagram

FM/AM Tuner

Description

The CXA1030P is an IC designed for FM/AM hi-fi tuners. It combines the functions from the FM/AM front end to the detection output stage.

Features

- Few peripheral components
- The FM front end suits for the FTZ '85 standard.
- A ceramic resonator is used for the FM discriminator.
- The AM mixer has particularly high sensitivity and good input characteristics.
- The AGC characteristics are excellent. (FOM = 90 dB typ.)

Functions

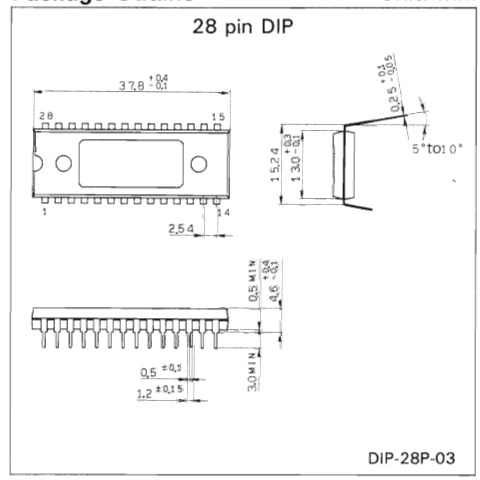
- FM front end (double valanced mixer, FM oscillator, and FM oscillator buffer)
- FM IF AF (FM IF limiter, quadrature detector S-meter drive circuit, band signal output circuit, and AFC drive circuit)
- AM RF, IF, AF (high frequency amplifier stage, AM double balance mixer attached with AGC, balance mixer, AM oscillator, AM-IF amplifier attached with AGC, and AM detector)

Structure

Silicon monolithic IC

Package Outline

Unit: mm



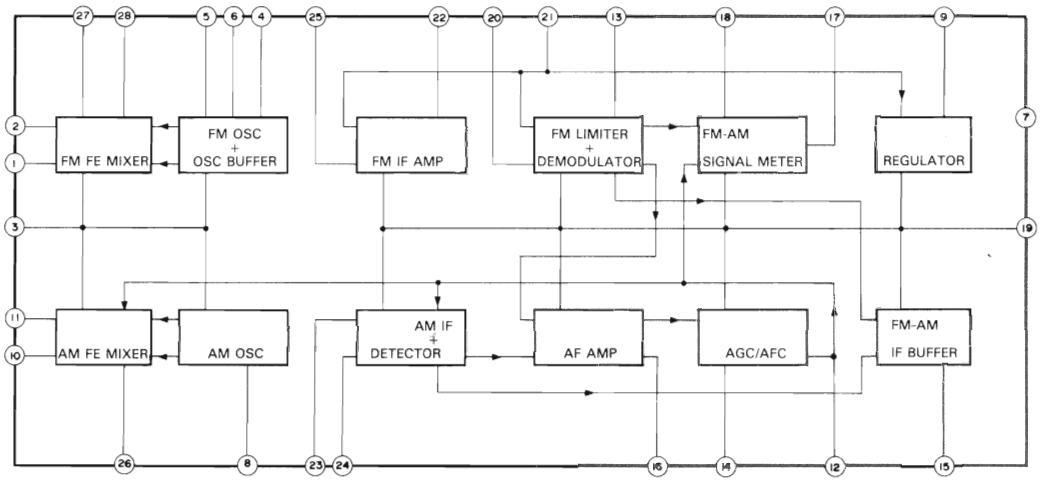
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	10	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−50 to +150	°C
• Allowable power dissipation	PD	876	mW

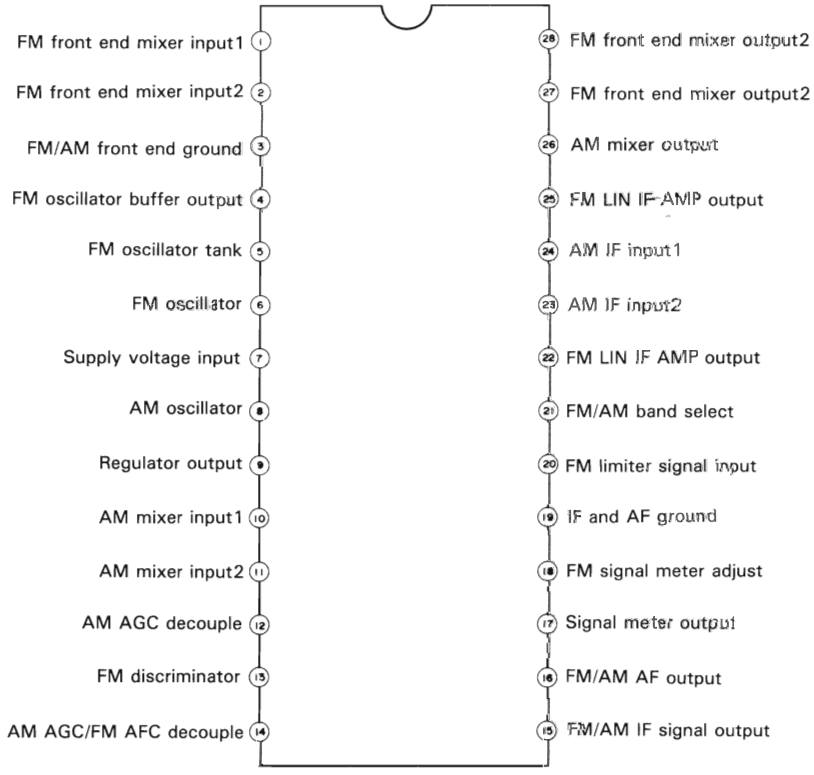
Recommended Operating Condition

• Supply voltage	Vcc	5 to 9	V

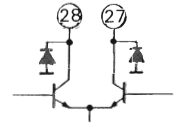
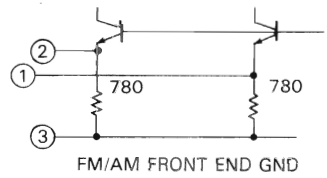
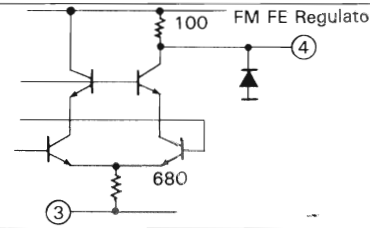
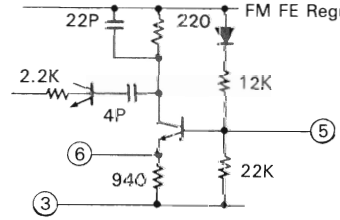
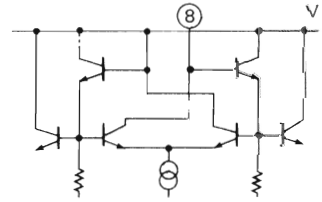
Block Diagram

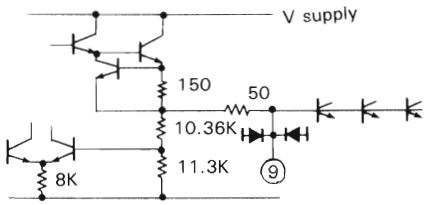
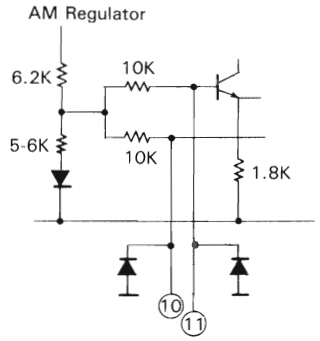
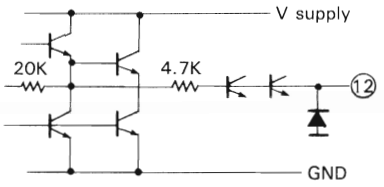
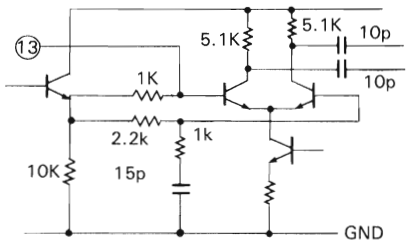


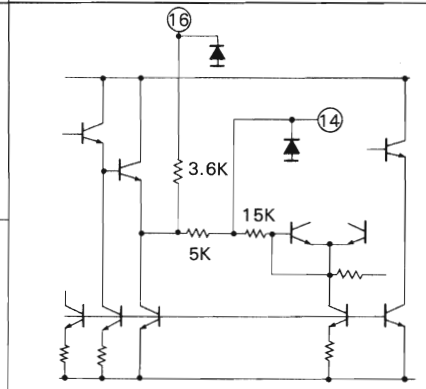
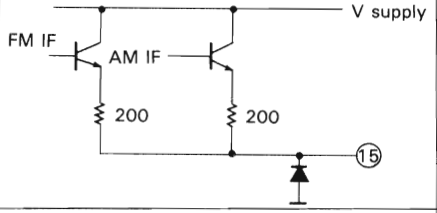
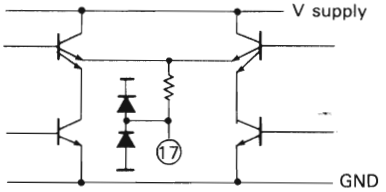
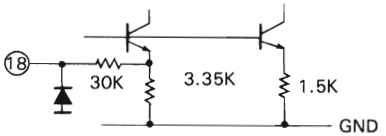
Pin Configuration (Top View)

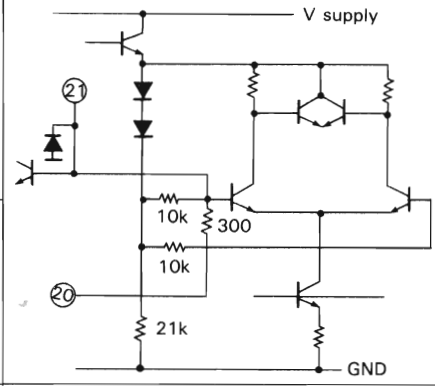
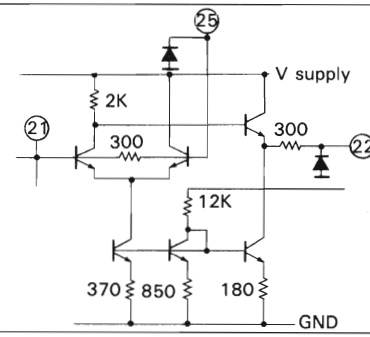
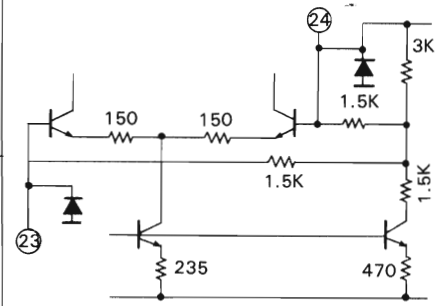
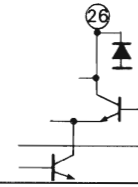

1 FM front end mixer input1
2 FM front end mixer input2
3 FM/AM front end ground
4 FM oscillator buffer output
5 FM oscillator tank
6 FM oscillator
7 Supply voltage input
8 AM oscillator
9 Regulator output
10 AM mixer input1
11 AM mixer input2
12 AM AGC decouple
13 FM discriminator
14 AM AGC/FM AFC decouple
28 FM front end mixer output2
27 FM front end mixer output2
26 AM mixer output
25 FM LIN IF AMP output
24 AM IF input1
23 AM IF input2
22 FM LIN IF AMP output
21 FM/AM band select
20 FM limiter signal input
19 IF and AF ground
18 FM signal meter adjust
17 Signal meter output
16 FM/AM AF output
15 FM/AM IF signal output

Pin Description

No.	Name	Voltage (V) FM	Voltage (V) AM	Equivalent circuit	Description
1 2	FM front end Mixer input	0.97	0		FM front end Input pin
27 28	FM front end Mixer output	7.26	7.30		FM front end Output pin 10.7 MHz signal is output
3	AM/FM Front end ground	0	0		FM/AM Ground of the FM/AM front end
4	FM oscillator buffer output	3.65	0		The oscillator is buffer output approx. 30 mVrms.
5	FM oscillator tank circuit input	2.00	0		The oscillation tank is attached
6	FM oscillator	1.34	0		The oscillation capacitor is attached
7	Supply voltage input	7.30	7.30	V supply	Power supply pin
8	AM oscillator	7.30	7.30		The coil for AM OSC is attached and oscillation voltage level is approx. 225 mVrms

No.	Name	Voltage (V) FM	Voltage (V) AM	Equivalent circuit	Description
9	Regulator output	2.24	2.24		The regulator output is attached with C for decoupling (approx. 2.3V)
10	AM mixer input	0	2.30		The AM RF input is connected to the bar antenna
11	AM mixer input	0	2.30		
12	AM AGC decouple	2.00	0		The decoupling capacitor (1.5μF) is attached
13	FM discriminator	2.00	0		A ceramic discriminator is attached with a 240 Ω series resistor.

No.	Name	Voltage (V)		Equivalent circuit	Description
		FM	AM		
14	AM AGC/FM AFC decouple	2.60	2.30		A decoupling capacitor (68 μF) is attached.
16	Detector output	2.70	2.30		Detection output pin
15	AM/FM IF signal out	2.70	1.70		IF output pin of FM/AM
17	Signal meter output	0	0		Output pin of the S-meter
18	FM signal meter adjust	0.30	0		The starting point of the S-meter can be changed in FM mode.
19	IF and AF ground	0	0	GND (IF, AF)	GND of FM/AM IF and AF

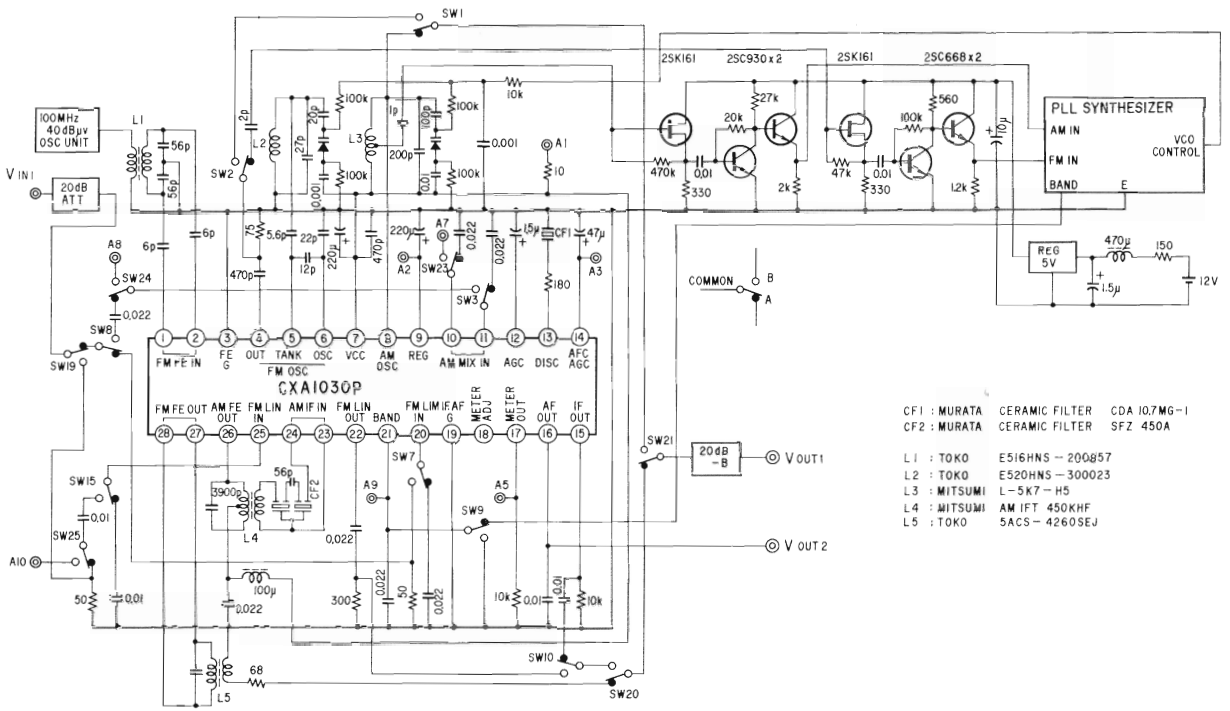
No.	Name	Voltage (V)		Equivalent circuit	Description
		FM	AM		
20	FM limiter signal input	2.60	0		Input pin of FM Limiter amp
21	FM IF decouple and FM/AM switching	2.26	0		FM and AM are selected for "OPEN" and "GND Short", respectively.
22	FM LIN IF AMP output	6.00	6.75		FM linear amplifier output pin
25	FM LIN IF AMP input	2.26	0		FM linear amplifier input pin
23	AM IF input	0	2.16		AM IF input pin
24	AM IF input	0	2.16		
26	AM mixer output	7.26	7.30		AM IF output

Electrical Characteristics

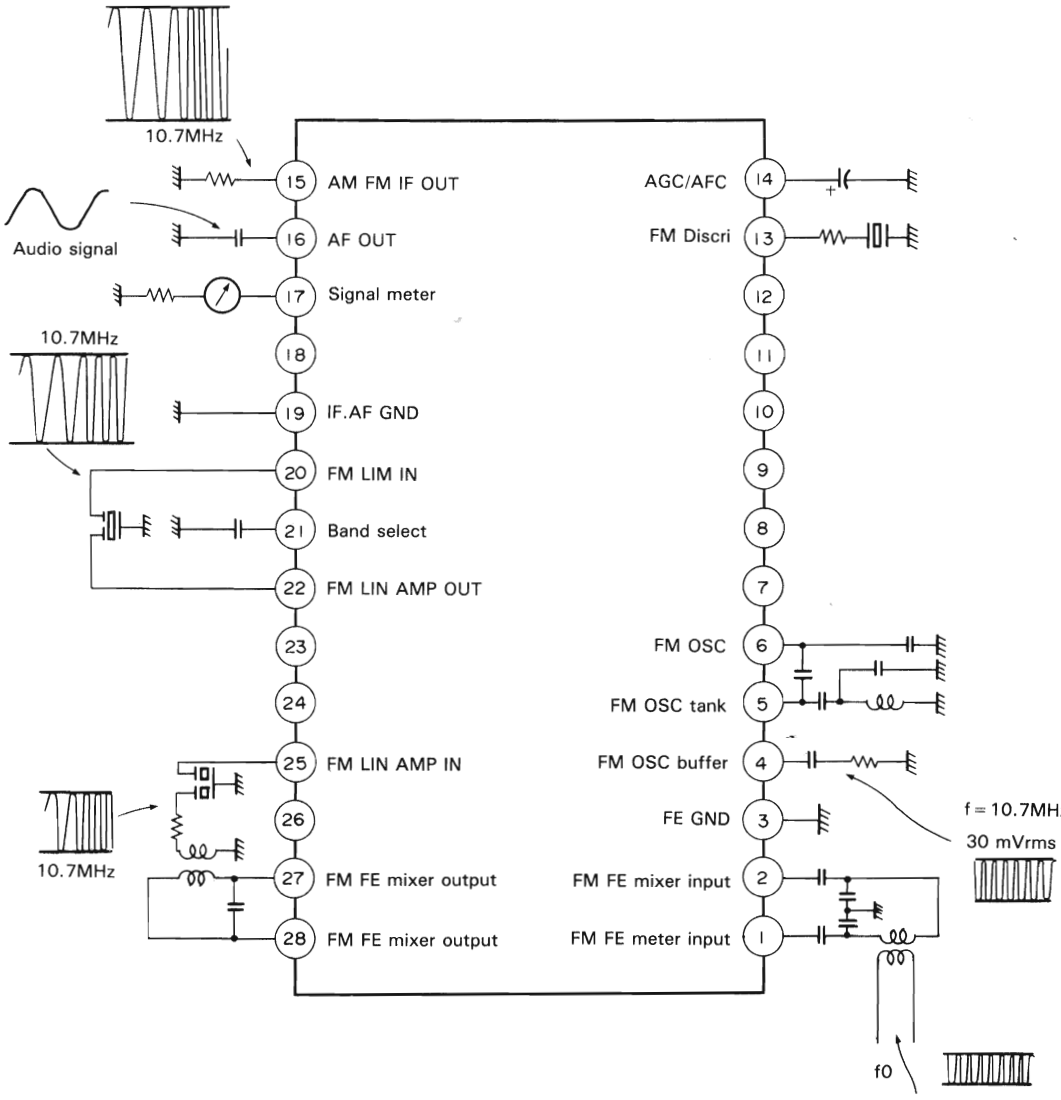
Ta = 25°C (unless otherwise specified, Vcc = 7.5 V)

Test No.	Test item	Symbol	SW condition 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	Bias condition V_{IN1}	Test point	Output waveform and explanation of test method	Min.	Typ.	Max.	Unit
1	AM circuit current	Iam	A	A	A	A	A	A	A	A	B	A	A	A	A	A	A	A	A	A	A	A	A	A	OFF	A1		17	22	27	mA
2	FM circuit current	Ifm	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	OFF	A1	No signal	21	26	31	mA
3	Reference voltage	Vref	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	OFF	A2		2.1	2.3	2.5	V
4	FM front end voltage gain (1)	Vg1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	OFF	V_{OUT1}	V_{IN} = 100 MHz, 40 dBμV, CW V_{OUT1} = 10.7 MHz, CW	11	13	15	dB
5	FM osc. buffer voltage gain (1)	Vo1	B	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	B	A	OFF	V_{OUT1}	V_{OUT1} = 110.7 MHz, CW	20	25	30	mV
6	FM IF amplifier voltage gain (2)	Vg2	A	A	A	A	A	A	A	A	A	B	A	A	A	A	B	A	A	A	B	B	A	A	ON	V_{OUT1}	V_{IN1} = 10.7 MHz, 40 dBμV, CW V_{OUT1} = 10.7 MHz, CW	8	10	12	dB
7	FM detection output voltage (1)	Vd1	A	A	A	A	A	A	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	ON	V_{OUT2}	V_{IN1} = 10.7 MHz, 80 dBμV, 1 KHz, 22.5 KHz dev V_{OUT2} = 1 KHz sine wave	90	100	110	mV
8	FM detection output voltage (2)	Vd2	A	A	A	A	A	A	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	ON	V_{OUT2}	Level difference when V supply = 9V in the same condition as above.	−10	0	10	mV
9	FM IF knee level	Vif	A	A	A	A	A	A	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	ON	V_{IN1}	Level of V_{IN1} when V_{d1} is reduced by 3 dB	—	25	30	dBμV
10	FM IF output level (3)	Vo3	A	A	A	A	A	B	A	A	A	A	A	A	A	A	A	A	A	A	A	B	A	A	ON	V_{OUT1}	V_{IN1} = 10.7 MHz, 100 dBμV, CW V_{OUT1} = 10.7 MHz CW	200	240	280	mV
11	FM detection output distortion (1)	THD1	A	A	A	A	A	A	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	ON	V_{OUT2}	V_{IN1} = 10.7 MHz, 80 dBμV, 1 KHz, 75 KHz dev V_{OUT2} = 1 KHz sine wave	—	0.3	1.1	%
12	FM IF offset voltage	Voff	A	A	A	A	A	A	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	ON	A3	V_{IN1} = 10.7 MHz, 80 dBμV, 1 KHz, 75 KHz dev	−100	0	100	mV
13	FM signal meter output voltage (1)	Vm1	A	A	A	A	A	A	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	ON	A5	V_{IN1} = 10.7 MHz, 100 dBμV, CW	2.5	3.0	3.5	V
14	FM freq. window width	f	A	A	A	A	A	A	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	ON	A5	V_{IN1} = 10.7 MHz, 100 dBμV, CW	65	80	100	kHz
15	FM signal meter output voltage (2)	Vm2	A	A	A	A	A	A	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	ON	A5	No signal	—	0	0.2	V
16	AM front end voltage gain (3)	Vg3	A	A	B	A	A	A	A	B	B	A	A	A	A	A	A	A	A	B	A	B	A	A	ON	V_{OUT1}	V_{IN1} = 1665 KHz, 60 dBμV, CW V_{OUT1} = 450 KHz, CW	18	20	22	dB
17	AM IF voltage gain (4)	Vg4	A	A	A	A	A	B	A	A	B	A	A	A	A	A	A	A	A	A	A	B	A	A	ON	V_{OUT1}	V_{IN1} = 450 KHz, 26 dBμV, CW V_{OUT1} = 450 KHz, CW	110	130	150	mV
18	AM detection output voltage (3)	Vd3	A	A	B	A	A	A	A	B	B	A	B	B	A	B	A	B	B	A	A	A	A	A	ON	V_{OUT2}	V_{IN1} = 1665 KHz, 60 dBμV, 1 KHz, 30%, V_{OUT2} = 1 KHz sine wave	90	100	110	mV
19	AM detection output voltage (4)	Vd4	A	A	B	A	A	A	A	B	B	A	B	B	A	B	A	B	B	A	A	A	A	A	ON	V_{OUT2}	Level difference when Vsupply = 9V under the same conditions as above.	−10	0	−10	mV
20	AM signal meter output voltage (3)	Vm3	A	A	B	A	A	A	A	B	B	A	B	B	A	B	A	B	B	A	A	A	A	A	ON	A5	V_{IN1} = 1665 KHz, 100 dBμV, CW	2.5	3.0	3.5	V
21	AM signal meter output voltage (1)	Vm4	A	A	B	A	A	A	A	B	B	A	B	B	A	B	A	B	B	A	A	A	A	A	ON	A5	V_{IN1} = 1665 KHz, 30 dBμV, CW	—	0	0.2	V
22	AM detection output distortion (2)	THD2	A	A	B	A	A	A	A	B	B	A	B	B	A	B	A	B	B	A	A	A	A	A	ON	V_{OUT2}	V_{IN1} = 1665 KHz, 60 dBμV, 1 KHz, 30%, V_{OUT2} = 1 KHz sine wave	—	1.0	2.0	%
23	AM detection output distortion (3)	THD3	A	A	B	A	A	A	A	B	B	A	B	B	A	B	A	B	B	A	A	A	A	A	ON	V_{OUT2}	V_{IN1} = 1665 KHz, 106 dBμV, 1 KHz, 80%, V_{OUT2} = 1 KHz sine wave	—	—	2.5	%
24	AM osc. voltage	VO2	A	A	A	A	A	A	A	A	B	A	A	A	A	A	A	A	A	A	A	A	B	B	OFF	V_{OUT1}		180	200	220	mV

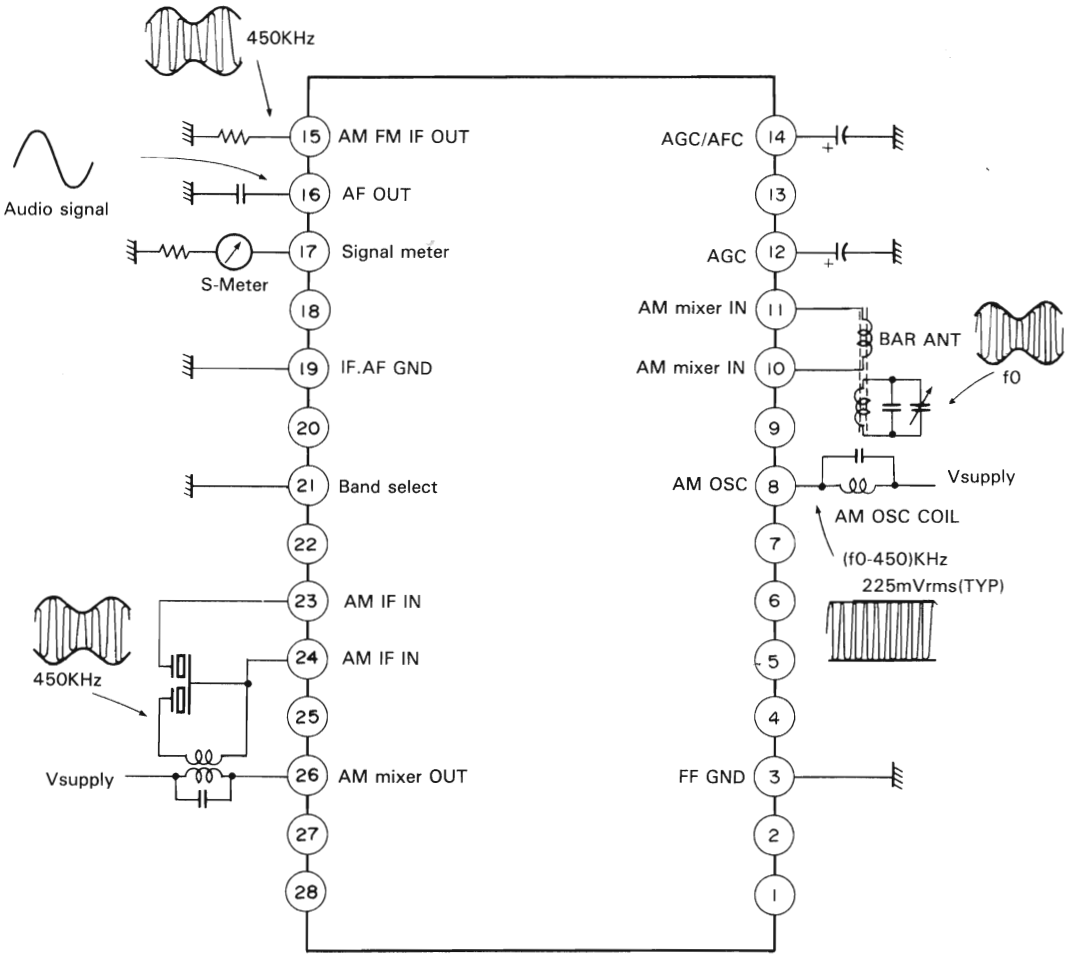
Electrical Characteristic Test Circuit



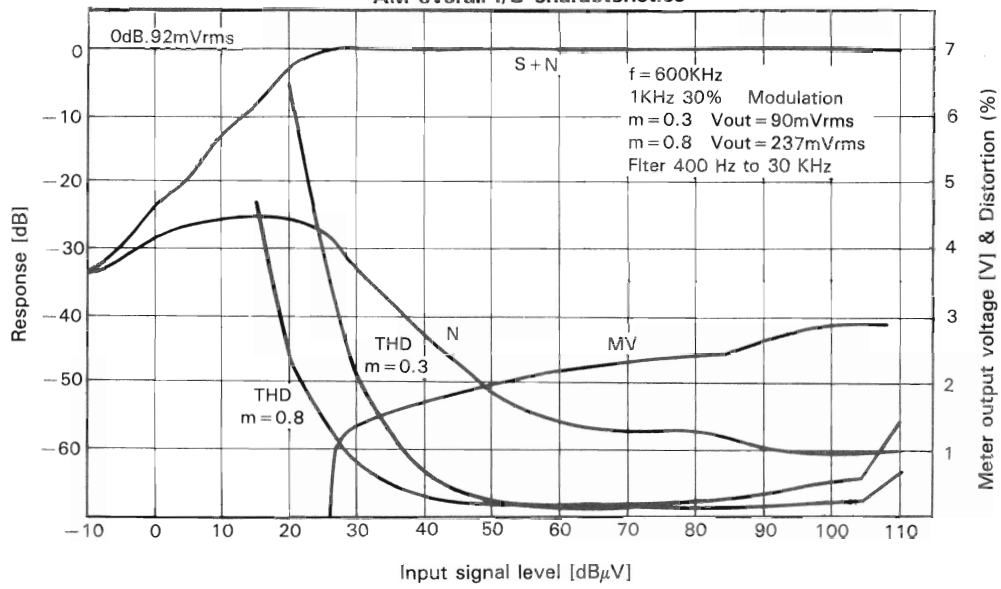
Description of Operation (FM Mode)



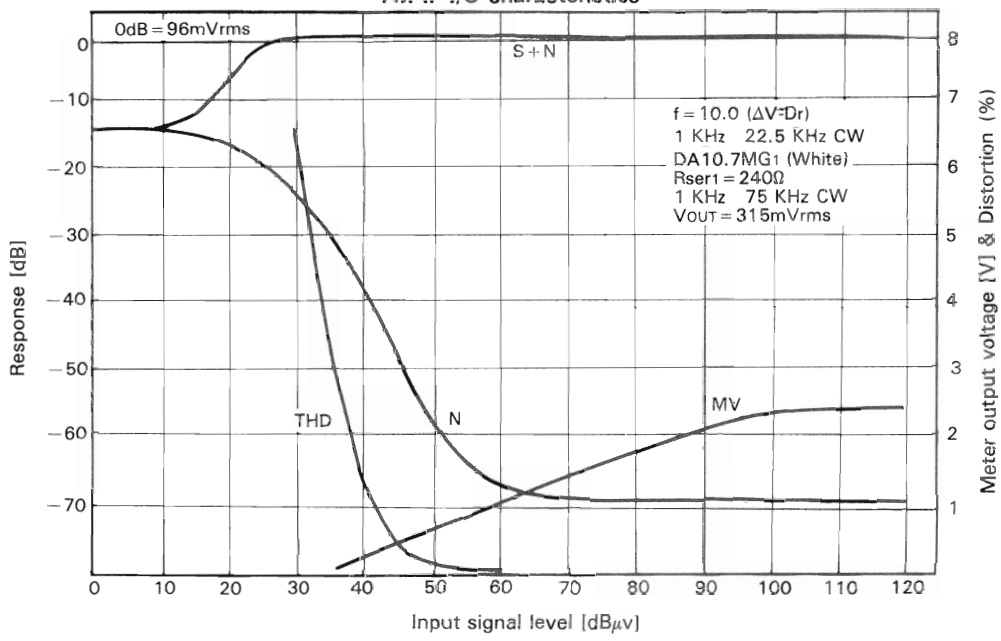
Description of Operation (AM Mode)



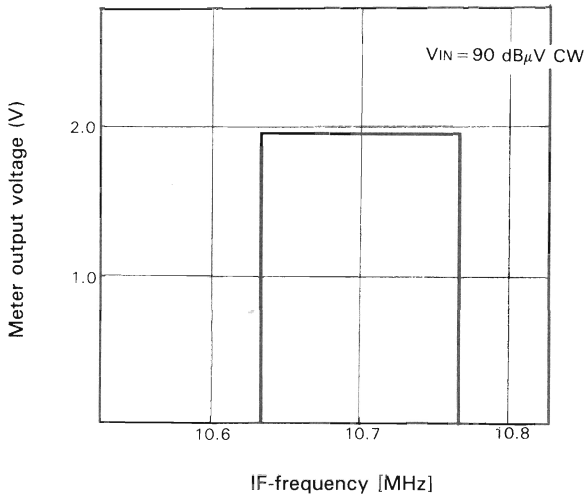
AM overall I/O characteristics



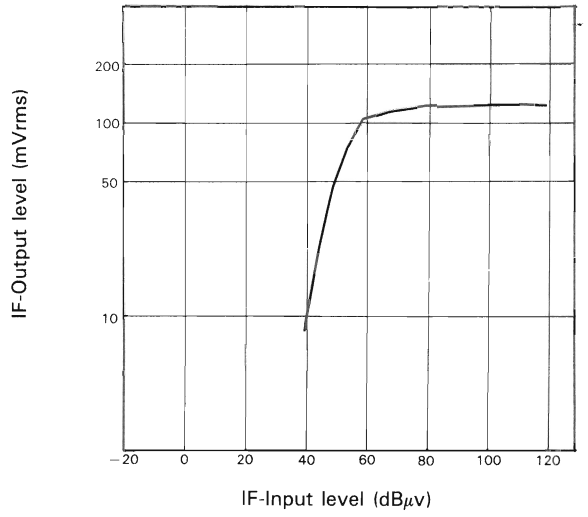
FM IF I/O characteristics



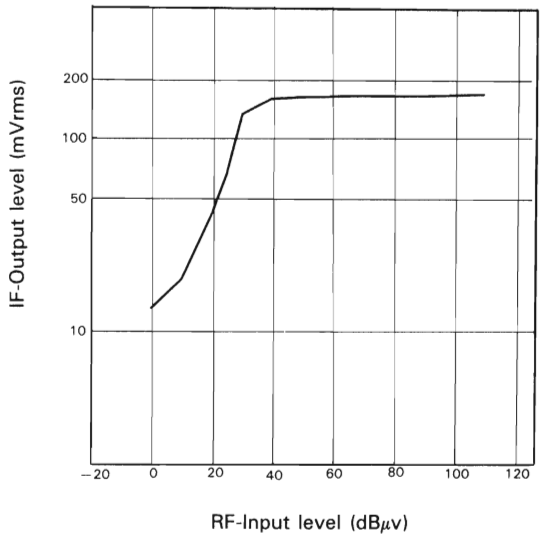
FM band signal output characterisitcs



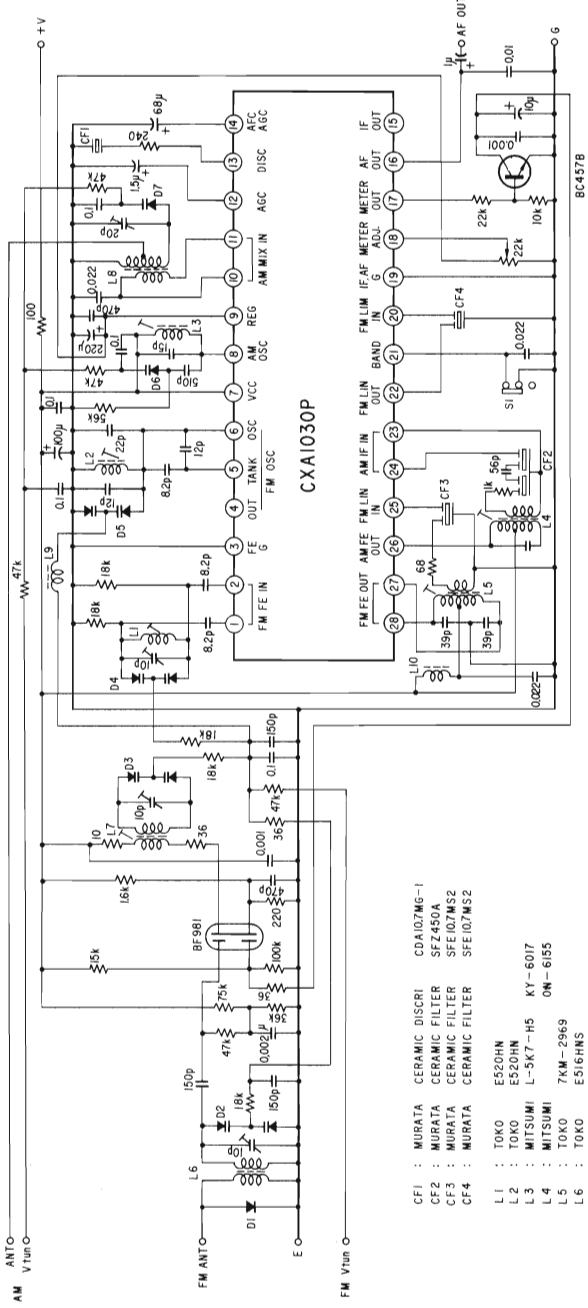
FM/AM IF out I/O characteristics (FM)



FM/AM IF out I/O characteristics (AM)



Application Circuit



CF1 : MURATA CERAMIC DISCRI CDA10.7MG-I
CF2 : MURATA CERAMIC FILTER SFZ450A
CF3 : MURATA CERAMIC FILTER SFE10.7MS2
CF4 : MURATA CERAMIC FILTER SFE10.7MS2

L1 : TOKO E520HN
L2 : TOKO E520HN
L3 : MITSUMI L-5K7-H5 KY-6017
L4 : MITSUMI ON-6155
L5 : TOKO 7KM-2969
L6 : TOKO E516HNS
L7 : TOKO E516HNS
L8 : AM ANT COIL

L9 : CHOKE 100μH
L10 : CHOKE 100μH

FM/AM Radio

Description

The CXA1031M is a 28-pin miniature flat-type one-chip IC designed for an FM/AM radio, incorporating every function required for a radio set.

Features

- All functions from front end to the final audio stage
- Low power consumption
  (I_D = 5.3 mA for FM, I_D = 3.4 mA for AM, V_{CC} = 3V)
- Built-in LED drive circuit for tuning
- Variable capacitor for FM automatic frequency control
- Electronic volume
- A few external component

Functions

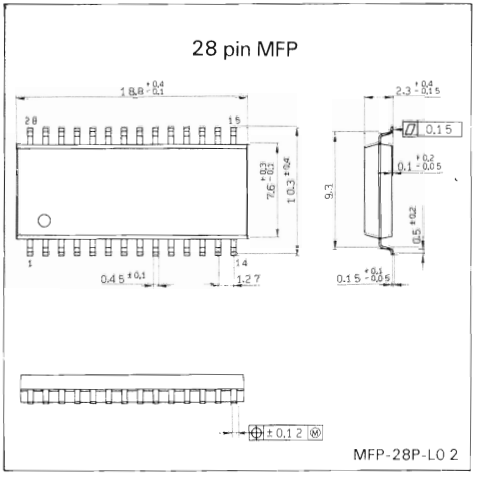
- FM/AM front end (variable capacitor for FM AFC)
- FM/AM IF amplifier (AM AGC, AM/FM LED drive circuit)
- FM/AM detector circuit
- Audio power amplifier (with electronic volume)

Structure

Bipolar silicon monolithic IC

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	9	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−50 to +125	°C
• Junction temperature	Tjmax	+125	°C
• Allowable power dissipation	PD	800	mW

Recommended Operating Condition

• Supply voltage	V_{CC}	2 to 4.5	V

Electrical Characteristics

0 dBm = 0.775 Vrms at 600Ω (Ta = 25°C, V_{CC} = 6V)

Item	Symbol	SW condition						Condition	Test point	Min.	Typ.	Max.	Unit
		S1	S2	S3	S4	S5	S6						
Circuit current 1	ID1	B	B	A	B	B	ON	No signal AM	IA	1.8	3.5	7.15	mA
Circuit current 2	ID2	A	B	A	B	B	ON	No signal FM	IA	4.1	7.0	10.5	mA
FM front end voltage gain 1	GV1	A	B	A	B	B	ON	V_{IN1} = 40 dBμV 100 MHz	VA	33	39	45	dB
FM detector output level 1	VD1	A	B	A	B	B	ON	V_{IN3} = 90 dBμV 10.7 MHz	VD	−25.5	−20	−15.5	dBm
FM detector output level 2	△VD	A	B	A	B	B	ON	V_{IN3} = 90 dBμV 10.7 MHz (1 kHz 22.5 KDEV) Level gap between V_{CC} (9V) and VD1	VD	−3.5	0	3.5	dB
FM IF knee level	VD2	A	B	A	B	B	ON	V_{IN3} = 90 dBμV 10.7 MHz (1K, 22.5 KDEV) V_{IN3} level at the point where the output level is 3 dB lower than limiting level.	VD		24	31	dBμV
FM detector output distortion factor 1	THD1	A	B	A	B	B	ON	V_{IN3} = 90 dBμV 10.7 MHz (1 kHz, 75 kHzDEV)	VD		0.3	1.1	%
FM IF center frequency offset	F	A	B	A	B	B	ON	V_{IN3} = 90 dBμV 10.7 MHz Frequency to set the voltage between Pin 8 and 21 to 0V.	VF	−55	0	55	kHz
FM meter current 1	IB1	A	B	A	B	B	ON	V_{IN3} = 60 dBμV 10.7 MHz	IB	1.8	3.5	6.1	mA
AM front end voltage gain 2	GV2	B	B	A	A	B	ON	V_{IN2} = 60 dBμV 1635 kHz	VB	16	22	28	dB
AM IF voltage gain 3	GV3	B	B	A	A	B	ON	V_{IN4} = 455 kHz (1 kHz, 30% MOD) V_{IN4} level for an output level of −34 dBm	VD	15	20	26	dBμV
AM detector output level 3	VD3	B	B	A	A	B	ON	V_{IN4} = 85 dBμV 455 kHz (1 kHz, 30% MOD)	VD	−25	−20	−15	dBm
AM meter current 2	IB2	B	B	A	A	B	ON	V_{IN4} = 85 kBμV 455 kHz (1 kHz, 30% MOD)	IB	1.35	3.0	5.5	mA

SONY

Electrical Characteristics

0 dBm = 0.775 Vrms at 600 Ω (Ta = 25°C, V_{CC} = 6V)

Item	Symbol	SW condition						Condition	Test point	Min.	Typ.	Max.	Unit
		S1	S2	S3	S4	S5	S6						
AM detector output distortion 2	THD2	B	A	A	A	A	ON	V_{IN2} = 95 dBμV V_{CC} = 7.8V 1635 kHz (1 kHz, 30% MOD)	VD		0.6	1.1	%
Audio voltage gain 3	GV4	B	A	C	A	A	OFF	V_{IN5} = −30 dBm 1 kHz	VE	27.5	31.5	35.5	dB
Attenuation 1	AT1	B	A	D	A	A	OFF	V_{IN5} = −30 dBm 1 kHz Output level gap between V_{OL} Max and the center	VE	11	24.5	38	dB
Attenuation 2	AT2	B	A	A	A	A	OFF	V_{IN5} = −10 dBm 1 kHz	VE		−76	−69	dBm
EIAJ output	VE	B	A	B	A	A	OFF	V_{IN5} = −20 dBm 1 kHz R_L = 8 Ω	VE	410	540		mW
Audio distortion factor 3	THD3	B	A	B	A	A	OFF	Distortion factor for an output of 50 mW V_{IN5} = −20 dBm 1 kHz	VE		0.3	2.2	%
Residual noise	N	B	A	C	A	A	ON	V_{IN} = GND	VE		−64	−57	dBm

Block Diagram

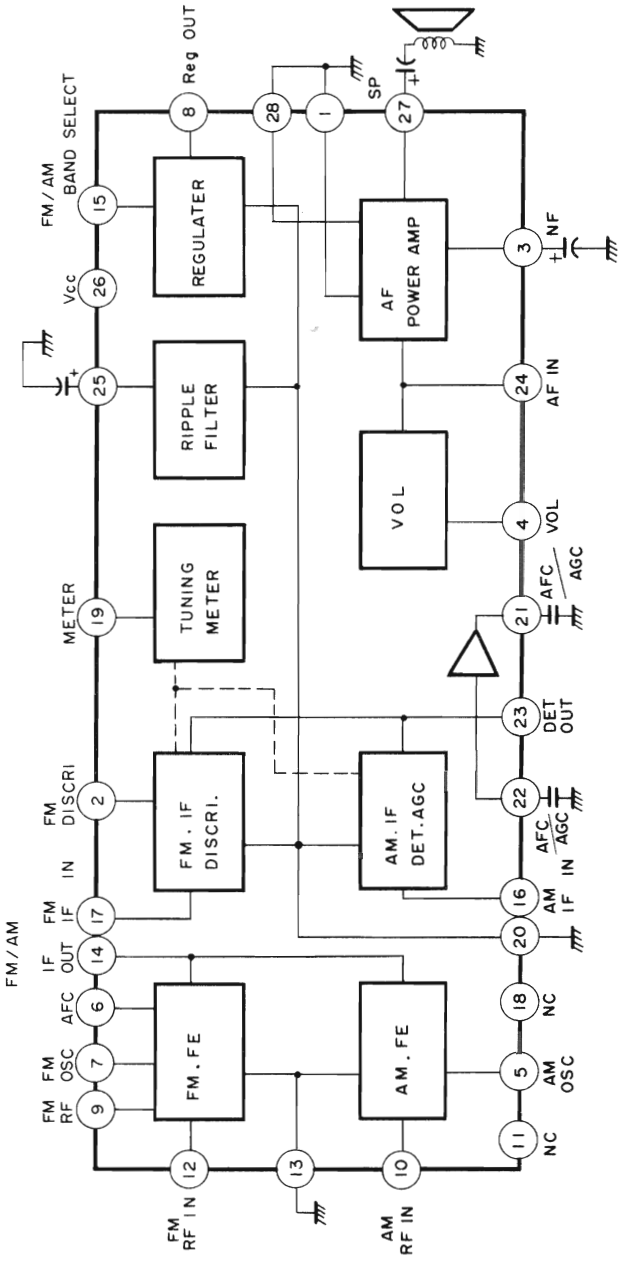


Fig. 1

Test Circuit

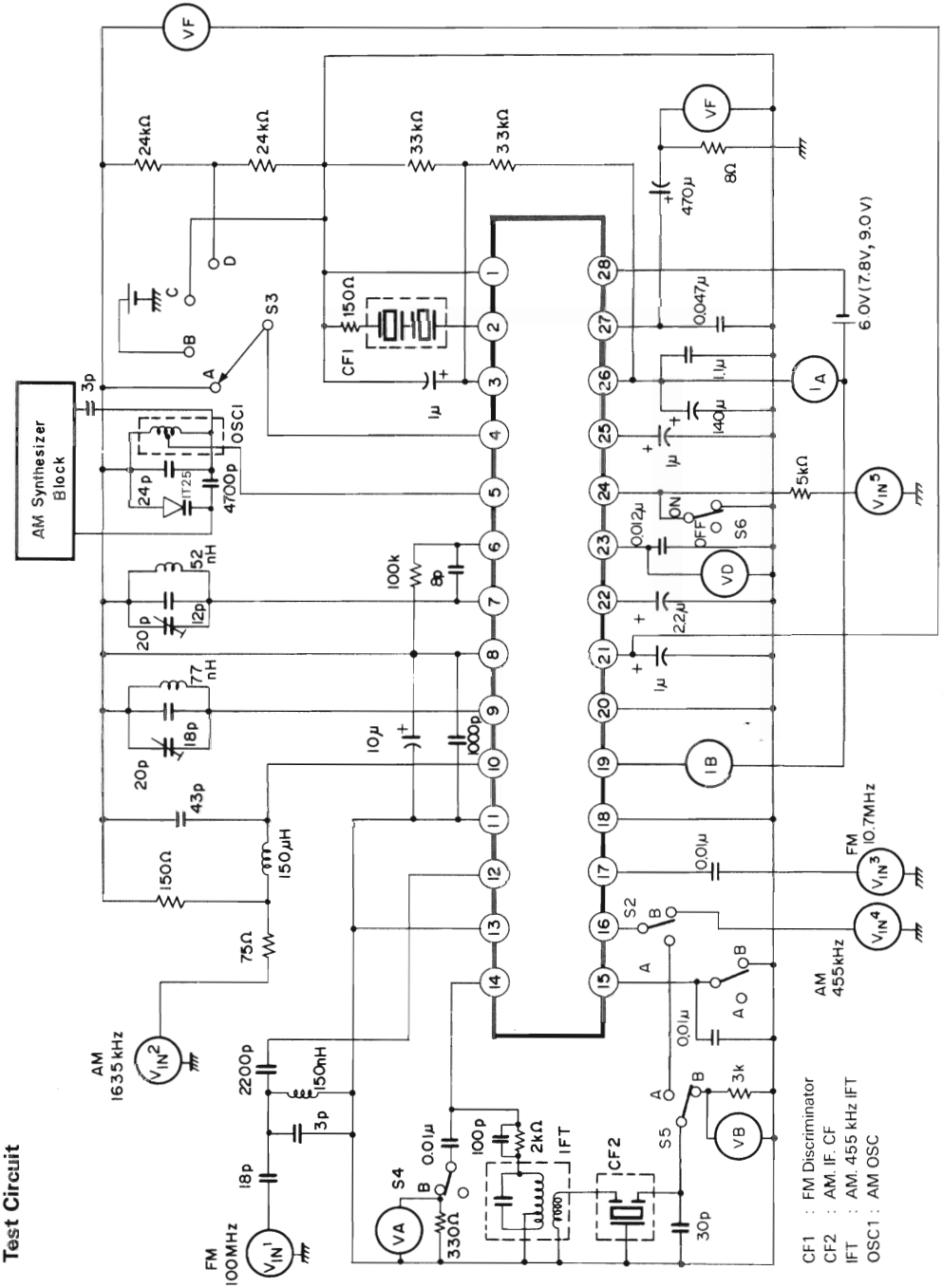


Fig. 2

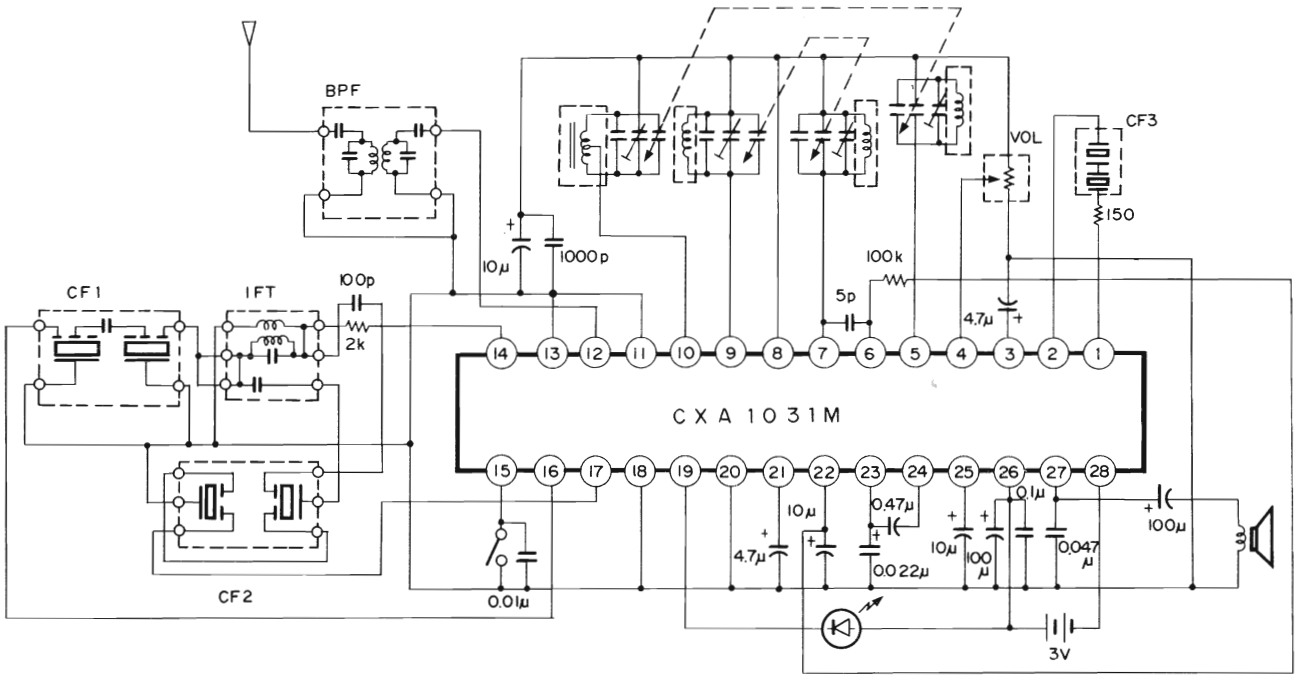
Standard Circuit Design Data

Pin voltage (Ta = 25°C)

Pin No.	3V		6V		Pin No.	3V		6V	
	FM	AM	FM	AM		FM	AM	FM	AM
1	0	0	0	0	15	0.84	0	0.88	0
2	2.18	2.70	4.88	5.43	16	0	0	0	0
3	1.5	1.5	3.0	3.0	17	0.84	0	0.88	0
4	1.25	1.25	1.25	1.25	18	0	0	0	0
5	1.25	1.25	1.25	1.25	19	1.6	1.6	4.5	4.5
6	1.25	*	1.25	*	20	0	0	0	0
7	1.25	1.25	1.25	1.25	21	1.25	1.49	1.25	1.49
8	1.25	1.25	1.25	1.25	22	1.25	1.12	1.25	1.12
9	1.25	1.25	1.25	1.25	23	1.25	1.0	1.25	1.0
10	1.25	1.25	1.25	1.25	24	0	0	0	0
11	0	0	0	0	25	2.71	2.71	5.4	5.4
12	0.3	0	0.3	0	26	3.0	3.0	6.0	6.0
13	0	0	0	0	27	1.5	1.5	3.0	3.0
14	0.36	0.2	0.36	0.2	28	0	0	0	0

Note) 1. All values are standard values (see Fig. 3).
2. All values were measured in the stage of Fig. 3 with no signal input and VOL MIN.
(The value for Pin 19 represents the voltage with LEDs mounted.)
3. * The voltage at Pin 6 in the AM mode becomes the same as that at Pin 22 in the J band and Pin 21 in the W band.

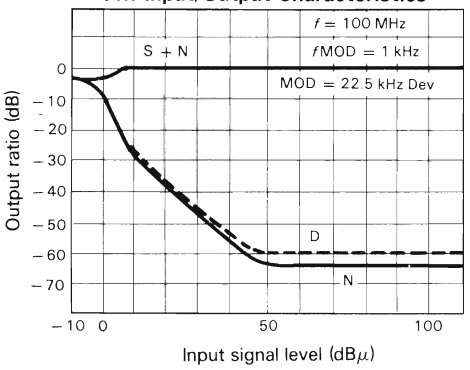
Test Circuit for Standard Circuit Design Data (for FM)



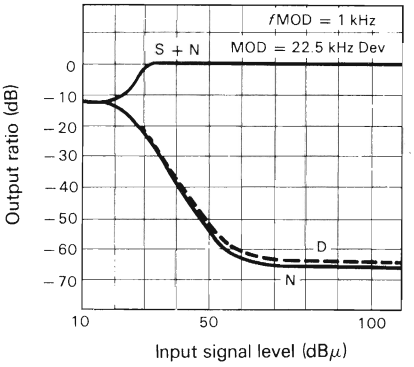
BPF : FM Band Pass Filter
CF1 : AM 455 kHz C. F
CF2 : FM-10.7 MHz C. F
CF3 : FM 10.7 MHz discriminator
IFT : AM 455 kHz IFT

Fig. 3

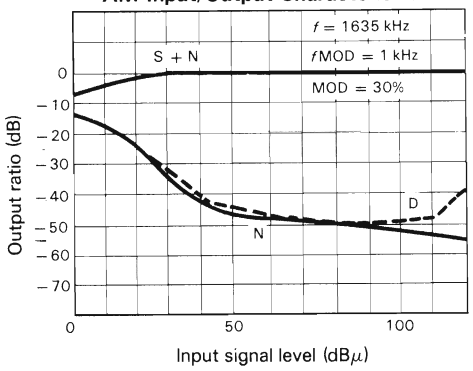
FM Input/Output Characteristics



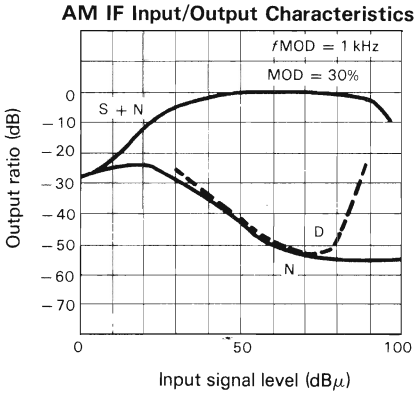
FM IF Input/Output Characteristics



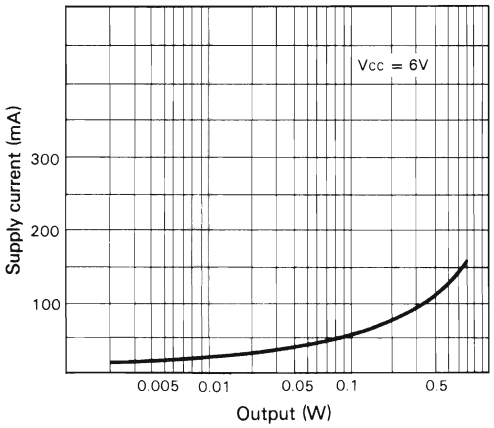
AM Input/Output Characteristics



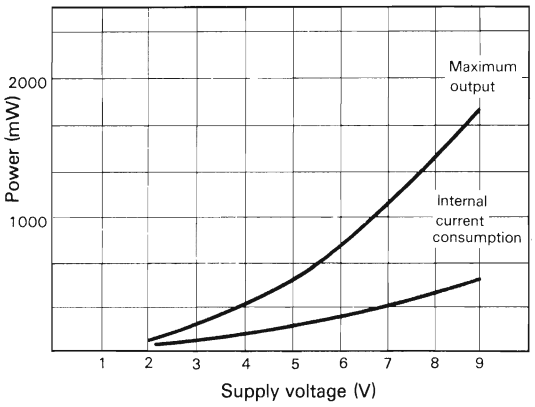
AM IF Input/Output Characteristics



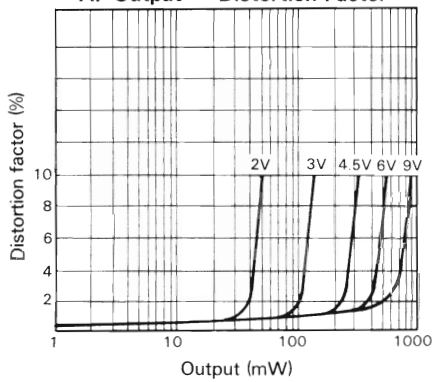
Output — Power Supply Current Characteristics



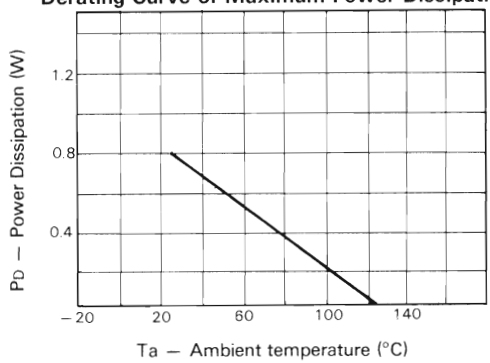
Supply Voltage — Maximum Output and Internal Consumption Characteristics



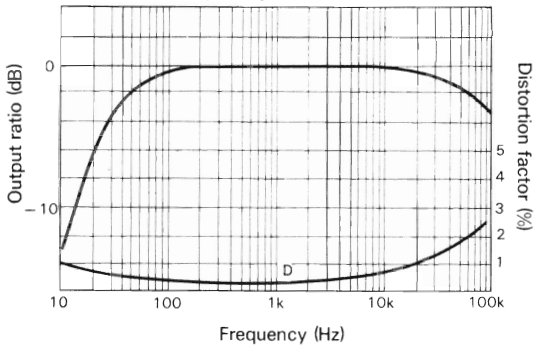
AF Output – Distortion Factor



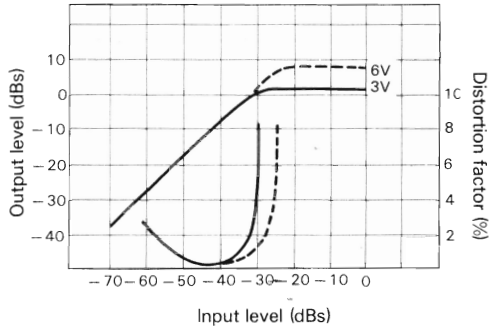
Derating Curve of Maximum Power Dissipation



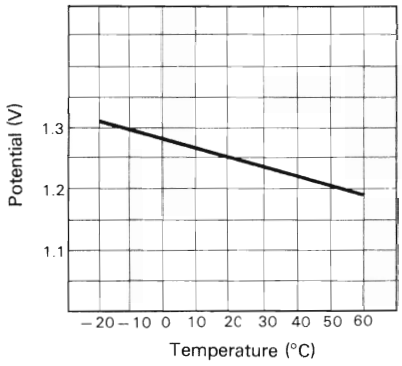
AF Frequency Characteristics



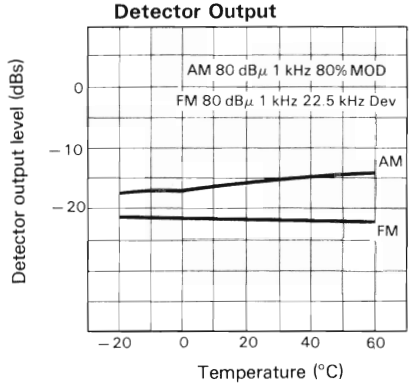
AF Input/Output Characteristics



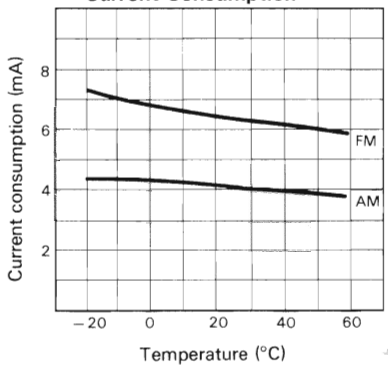
Temperature Characteristics of Regulator



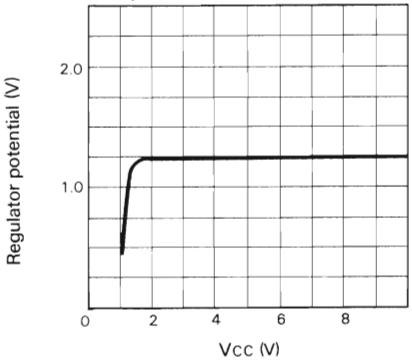
Temperature Characteristics of Detector Output



Temperature Characteristics of Current Consumption



Power Supply Voltage — Regulator Output Characteristics



AM Radio

Description

The CXA1032M, an MW/LW band AM radio IC, is designed for the use in small radio sets.

Features

- Low current consumption, 450μA (Vcc=3V static condition)
- Autodyne system

Functions

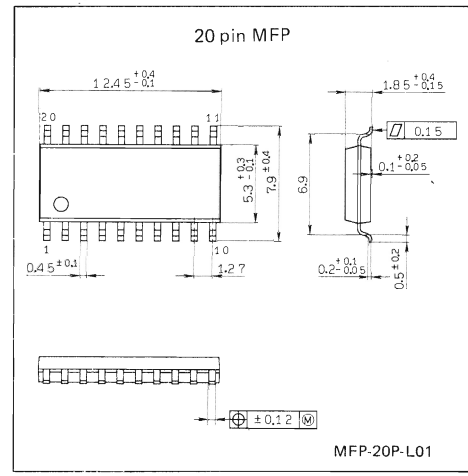
- Single-chip configuration integrates circuitory from the RF to earphone output (100mW)
- Internal DC/DC converter for VARI-CAP
- Internal automatic power-off timer

Structure

Bipolar silicon monolithic IC

Package Outline

Unit: mm



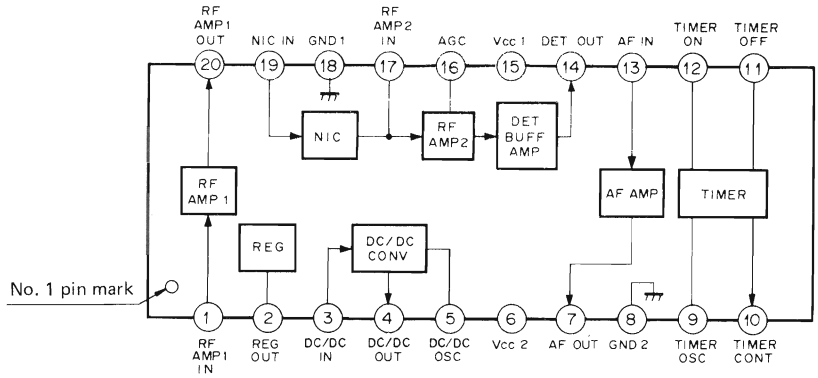
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	5	V
• Operating temperature	Topr	−15 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	200	mW

Recommended Operating Condition

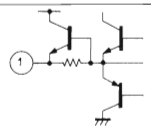
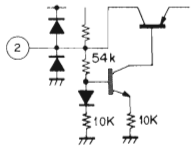
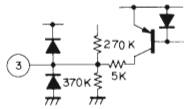
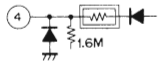
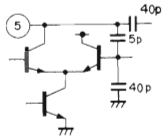
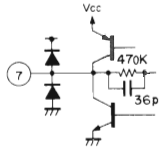
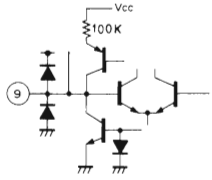
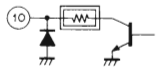
• Supply voltage	Vcc	1.8 to 4.5	V

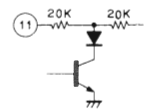
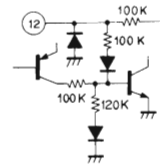
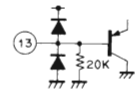
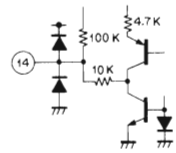
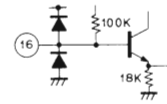
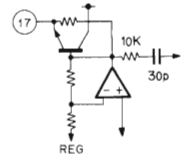
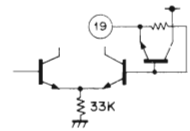
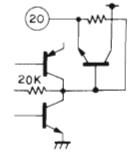
Block Diagram and Pin Configuration (Top View)



NIC : Negative Impedance Converter

Pin Description (See the Electrical Characteristics Test Circuit for pin voltage)

No.	Name	Equivalent Circuit	DC Potential (V)	Remark
1	RM AMP1 IN		1V	RF input Connect to achieve same electric potential as 2 pin.
2	REG OUT		1V	IC reference voltage
3	DC/DC IN		—	Voltage input Adjust input level to control output level.
4	DC/DC OUT		0.2 to 4.8V	DC/DC converter output pin Voltage applied to pin 3 controls level of this pin.
5	DC/DC OSC		Vcc	Oscillation, fosc ≒ 2MHz Connect via a coil to the power source (Vcc).
6	Vcc		—	Power source for audio frequency output amplifier Normally 3V
7	AF AMP OUT		Approx. 1/2 Vcc	Audio frequency output
8	GND		—	Ground pin for audio frequency output amplifier
9	TIMER OSC		—	Triangular pulse generated when a capacitor is connected between this and pin 2.
10	TIMER CONT		—	Controls of transistor, etc. using TIMER output

No.	Name	Equivalent Circuit	DC Potential (V)	Remark
11	TIMER OFF		—	Apply 3V to turn timer OFF.
12	TIMER ON		—	Apply 3V to turn timer ON.
13	AF AMP IN		0V	AF AMP input pin
14	DET OUT		0.7V (static)	Detection output
15	Vcc		—	RF amplifier power supply (Vcc)
16	AGC		0.7V	AGC voltage output
17	RF AMP2 IN		1V	Negative Impedance Converter circuit output; connected to RF AMP2 input.
18	GND		—	Small signal ground
19	NIC IN		1V	Provides REG bias; normally connected to RF AMP1 output potential pin 20
20	RF AMP1 OUT		1V	RF AMP output

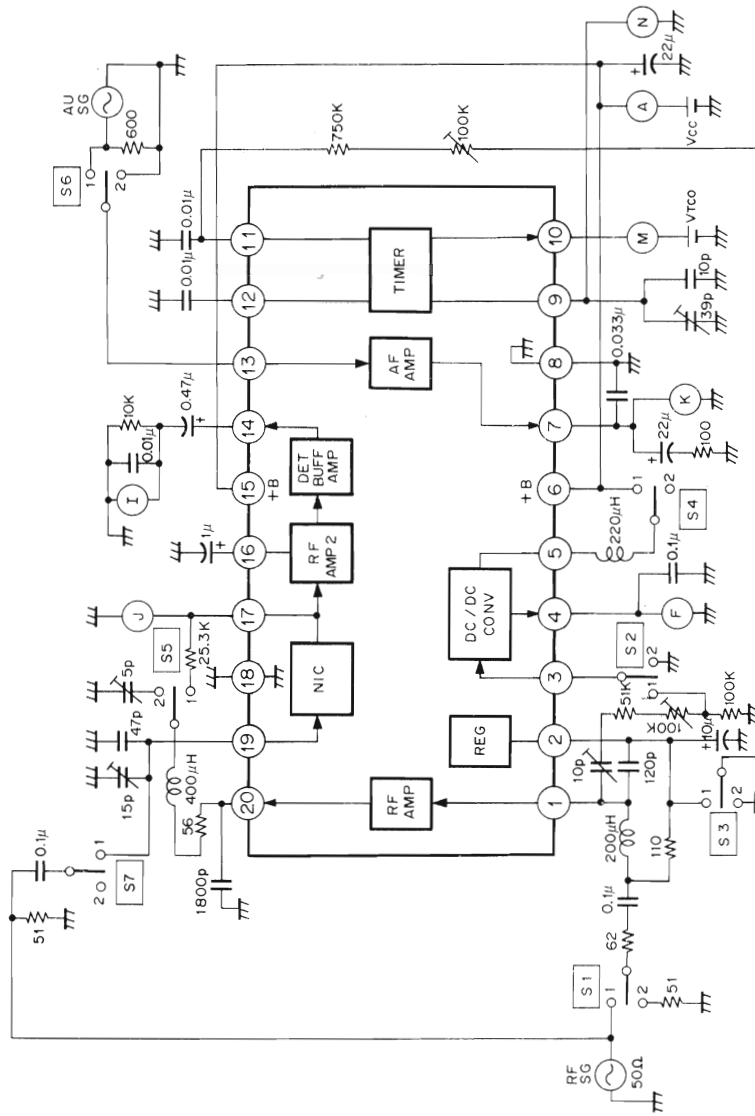
Electrical Characteristics

(See the Electrical Characteristics Test Circuit, Ta=25°C, Vcc=3V)

No.	Item	Symbol	Switch Mode							Test Condition	Bias Conditions			Min.	Typ.	Max.	Unit
			1	2	3	4	5	6	7		Vcc	VTCO	Test Points				
1	Current consumption (static condition)	ID	2	2	1	1	1	2	2	Current value at A point	3V	0V	A	300	450	700	μA
2	RF AMP 2 gain	GV2	↓	↓	↓	2	↓	↓	1	RF SG: 1MHz MOD: 30% 1kHz (+6dB) Gain with pin 14 at constant –44dBm	↓	↓	I	39	43	47	dB
3	Detection output level	VO	1	↓	↓	↓	2	↓	2	RF SG: 1MHz MOD: 30% 1kHz 95dBμV	↓	↓	I	–30	–27	–24	dBm
4	AGC characteristics	THDAGC	↓	↓	↓	↓	↓	↓	↓	Distortion factor when RF SG: 1MHz; MOD: 30% 1kHz 95dBμV (distortion)	↓	↓	I		1	6	%
5	RF AMP1 gain	GV1	↓	↓	↓	↓	↓	↓	↓	RF SG: 1MHz MOD: 30% 1kHz 30dBμV Gain at point J	↓	↓	J	35.5	39.5	43.5	dB
6	AF AMP gain	GVAF	2	1	2	1	↓	1	↓	AU SG: 1kHz-33dBm Gain at point K	↓	↓	K	30	33	36	dB
7	AF AMP distortion (10mW)	THD10	↓	↓	↓	↓	↓	↓	↓	AU SG: 1kHz Distortion rate at point K when pin 7 becomes 1Vrms	↓	↓	K	1	2.5	10	%
8	AF AMP distortion (1mW)	THD1	↓	↓	↓	↓	↓	↓	↓	AU SG: 1kHz Distortion rate at point K when pin 7 becomes 1Vrms and 316mVrms	↓	↓	K	–	0.3	1	%
9	AF AMP residual noise	NAF	↓	↓	↓	↓	↓	2	↓	Noise level of pin 7 when no signal is input	↓	↓	L	–	–75	–68	dBm
10	TIMER time	TO	↓	↓	1	↓	↓	↓	↓	Time required for pin 10 to reach 1μA after a 3V potential at pin 12 has been removed	↓	3V	M	280	338	400	ms
11	TIMER OSC frequency	t	↓	↓	↓	↓	↓	↓	↓	Frequency measurements taken during the above procedure	↓	↓	N	170	200	230	μs
12	DC/DC CONV VD (max.)	VMAX	↓	2	↓	↓	↓	↓	↓	DC voltage measurements	↓	↓	F	4.60	4.8	5.0	V
13	TIMER CONT output current (ON)	IO (ON)	↓	1	↓	↓	↓	↓	↓	DC current measurements when TIMER ON	↓	↓	M	55	120	210	μA
14	TIMER CONT output current (OFF)	IO (OFF)	↓	↓	↓	↓	↓	↓	↓	Leak current measurements when TIMER OFF	↓	↓	M	–	0	1	μA
15	NIC gain	GNIC	1	↓	↓	↓	1 ↓ 2	↓	↓	RF SG: 1MHz non-modulated 30dBμV RF OUT gain when SW1 → 2	↓	↓	J	4.0	6.0	7.0	dB

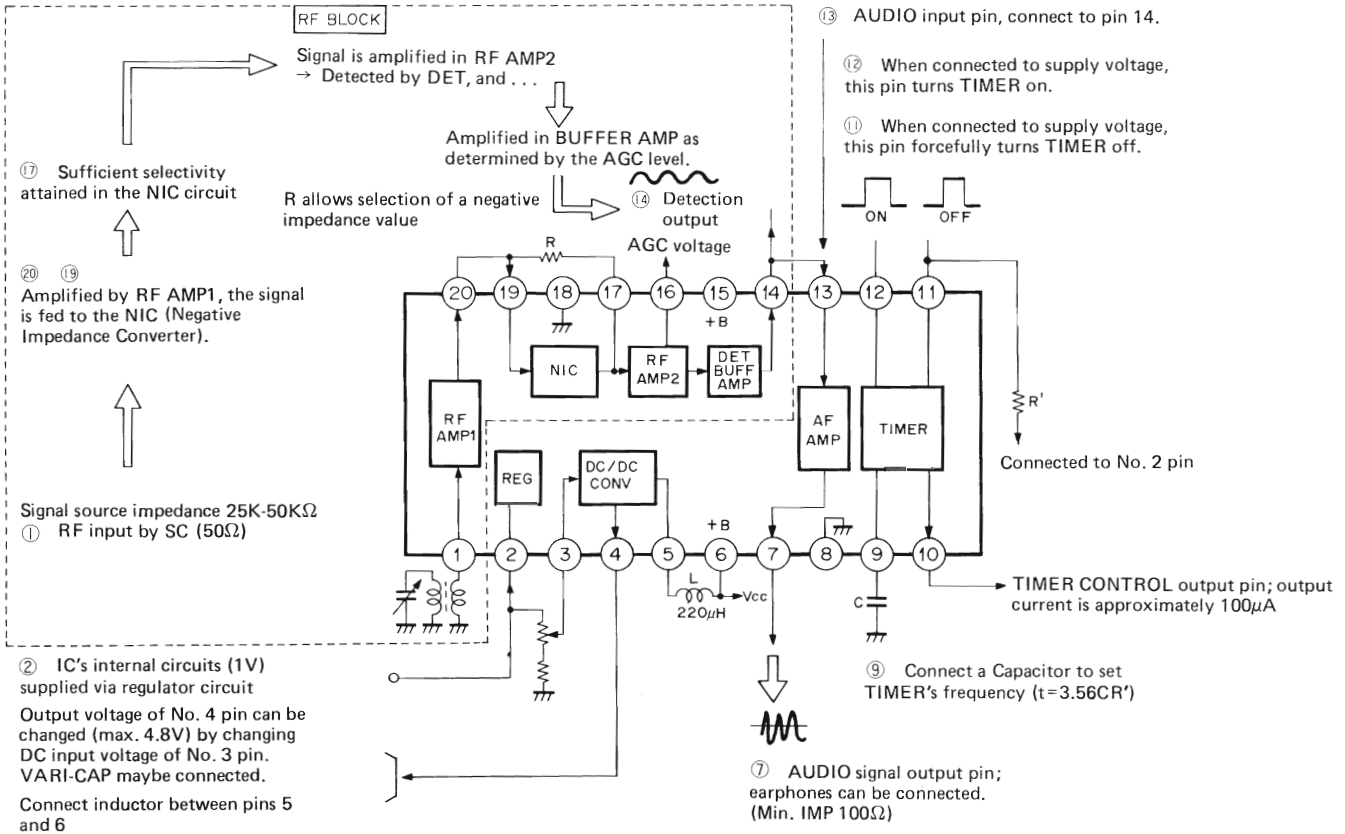
(0dBm = 775mVrms)

Electrical Characteristics Test Circuit

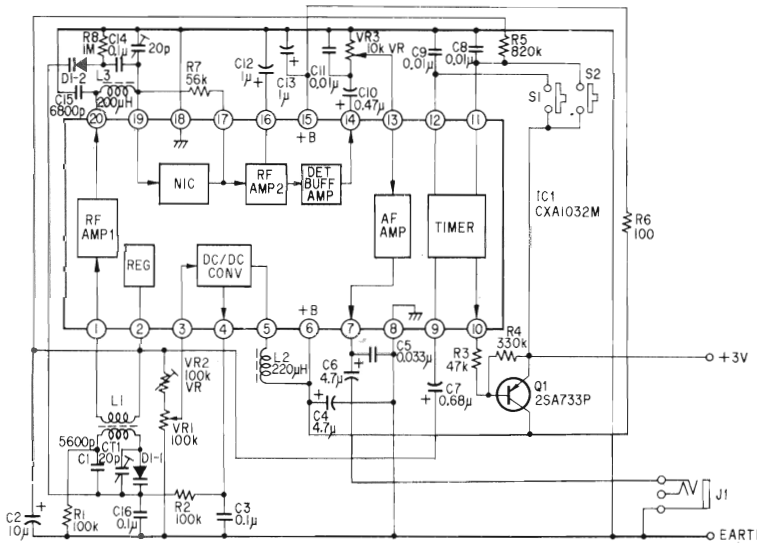


NIC : Negative Impedance Converter

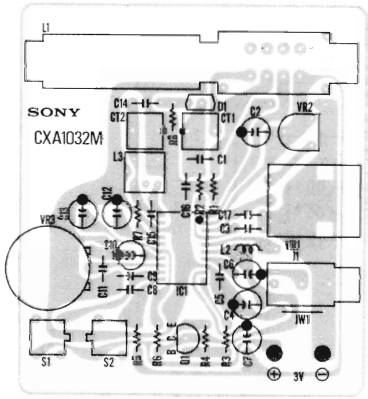
Description of Operation


RF BLOCK
Signal is amplified in RF AMP2
→ Detected by DET, and . . .
Amplified in BUFFER AMP as determined by the AGC level.
⑰ Sufficient selectivity attained in the NIC circuit
R allows selection of a negative impedance value
⑭ Detection output
AGC voltage
⑳ ⑲
Amplified by RF AMP1, the signal is fed to the NIC (Negative Impedance Converter).
⑬ AUDIO input pin, connect to pin 14.
⑫ When connected to supply voltage, this pin turns TIMER on.
⑪ When connected to supply voltage, this pin forcefully turns TIMER off.
ON
OFF
R
+B
NIC
RF AMP2
DET BUFF AMP
RF AMP1
REG
DC/DC CONV
AF AMP
TIMER
R'
Connected to No. 2 pin
Signal source impedance 25K-50KΩ
① RF input by SC (50Ω)
+B
L
220μH
Vcc
C
TIMER CONTROL output pin; output current is approximately 100μA
② IC's internal circuits (1V) supplied via regulator circuit
Output voltage of No. 4 pin can be changed (max. 4.8V) by changing DC input voltage of No. 3 pin.
VARI-CAP maybe connected.
Connect inductor between pins 5 and 6
Oscillation frequency of the DC/DC Converter can be measured at No. 5 pin.
The oscillation frequency (f) is determined by the coil (L) and the IC's internal capacity (C).
⑨ Connect a Capacitor to set TIMER's frequency (t=3.56CR')
⑦ AUDIO signal output pin; earphones can be connected. (Min. IMP 100Ω)

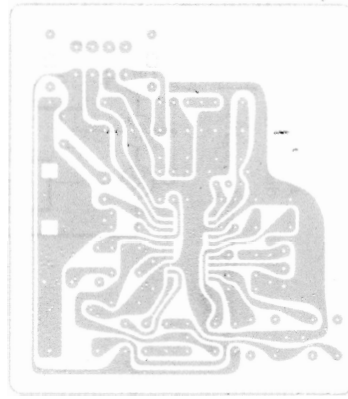
Application Circuit



Parts face

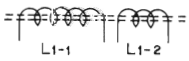


Pattern face



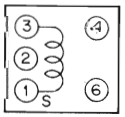
Reference data for parts used

Bar antenna coil



L_{1-1}	68T	4/0.07USTS
L_{1-2}	33T	3/0.07USTS
L_{1-1}	220μH	
Q	200 or above	
Core size	φ8.5mm×27	

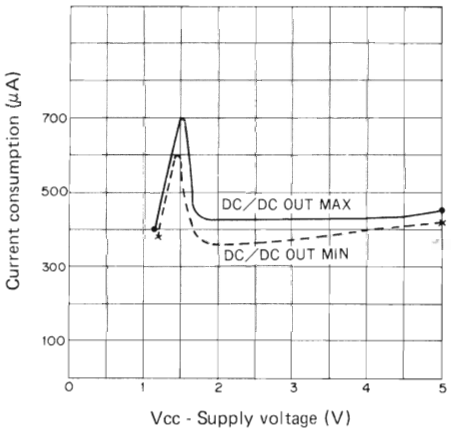
RF coil



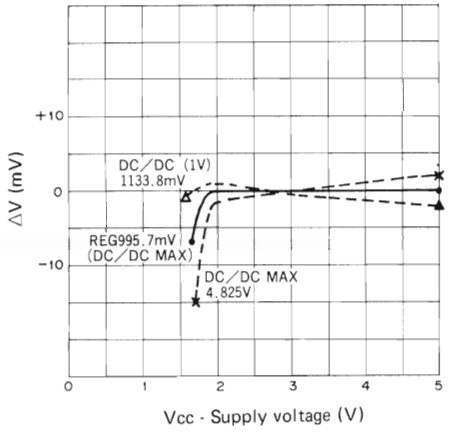
L = 200μH
Q = 100 or above
TOKO 7BRS-201000ZO or equivalent

Variable capacitor TOKO KV-1250M

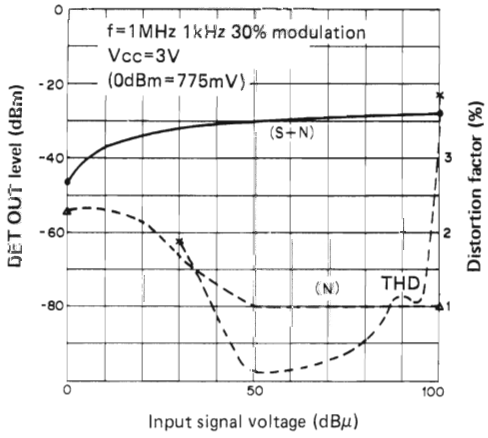
Current consumption vs. Supply voltage



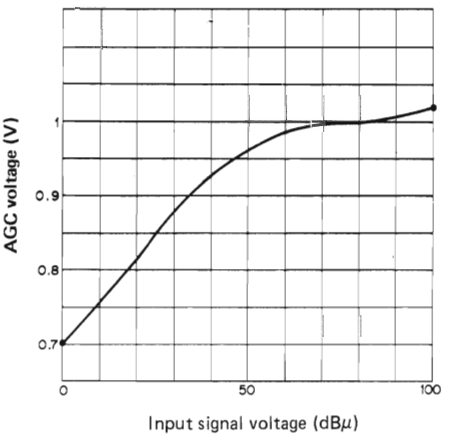
DC/DC output and REG voltage fluctuation vs. Supply voltage



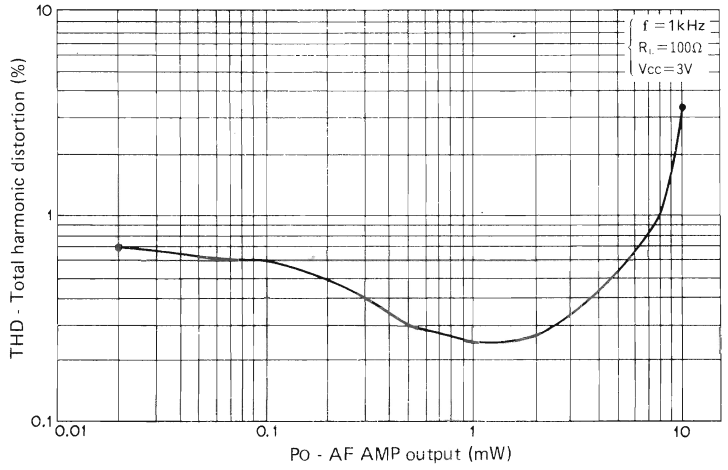
DET OUT level vs. Input signal voltage



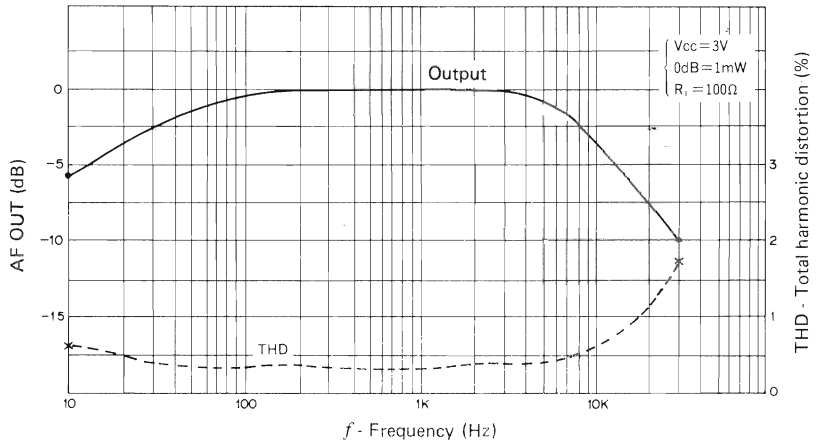
AGC voltage vs. Input signal voltage



Total harmonic distortion vs. AF AMP ouput



AF AMP fidelity characteristics



Notes on Application

1) Although the CXA1032M is provided with sufficient static electricity countermeasures, rough handling may cause damage to some of its pins.
2) AM radio band ranges up to approximately 2MHz.
   Beat interference due to harmonic can be prevented by selecting an oscillation frequency higher than 2MHz for the TIMER and DC/DC Converter.

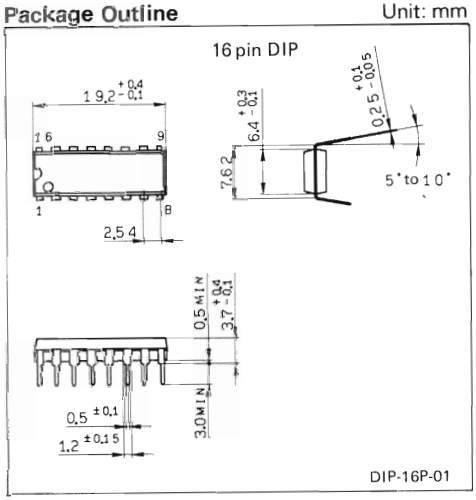
AM Radio

Description

The CXA1033P is one-chip bipolar IC which is specially designed for AM radio. It is fully equipped with all required functions such as AM front-end, AM IF amplifier (AM AGC, DET, LED driving circuit) and audio power amplifier (equipped with electronic volume control).

Package Outline

Unit: mm



Features

- All functions which cover from the front-end to the final audio stage are included.
- Standard minimum supply voltage at 1.8V
- Low current consumption ID = 2.7 mA (Typ.), Vcc = 3V
- Built-in LED operating circuit for tuning
- Built-in electronic volume control
- Little externally-attached equipment
- Large output EIAJ output = 540 mW (Typ.)
  Vcc = 6V (8 Ω load)

Structure

Bipolar silicon monolithic IC.

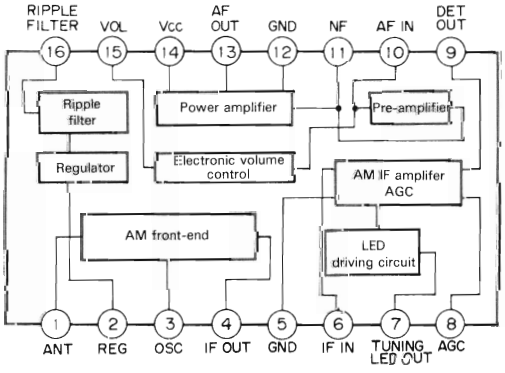
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	9	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−50 to +125	°C
• Allowable power dissipation	PD	650	mW

Recommended Operating Condition

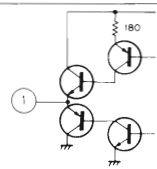
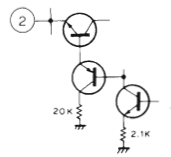
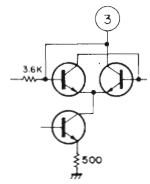
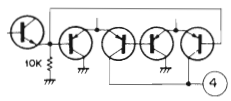
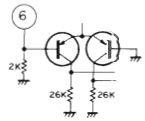
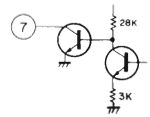
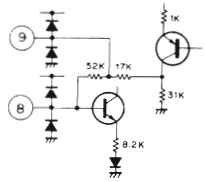
• Supply voltage	Vcc	2 to 7	V

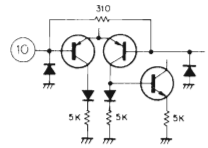
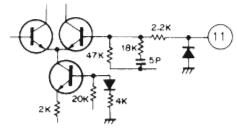
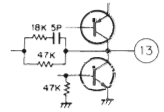
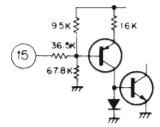
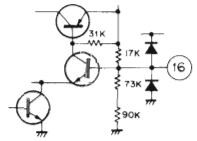
Block Diagram



Pin Description

Vcc = 3V

No.	Symbol	Value (Typ.)	Equivalent circuit	Description
1	ANT (RF IN)	1.25V		RF input pin to be connected with the antenna circuit
2	REG	1.25V		The output pin for the stabilized power source to provide a reference voltage to the internal circuit
3	OSC	1.25V		Oscillation output pin to be connected with an oscillation coil
4	IF OUT	0V		Mixer output pin to be connected with the IFT
5	GND	0V		Grounding pin for RF small signal system
6	IF IN	0V		The pin to be connected with an IF cerarnic filter
7	TUNING LED OUT	1.6V		The pin to operate LEDs. Open collector
8	AGC	1.35V		The pin to be connected with a capacitor
9	DET OUT	1.35V		Detection output pin to be connected to the AF IN pin

No.	Symbol	Value (Typ.)	Equivalent circuit	Description
10	AF IN	0.69V		Audio input pin
11	NF	1.5V		The pin to be connected with a capacitor
12	GND	0 V		Grounding pin for the audio output system
13	AF OUT	1.5V		Audio output pin to be connected with a capacitor and resistors
14	Vcc	3V		Power supply pin
15	VOL	1.25V		The pin to be connected to the midpoint of the volume control
16	RIPPLE FILTER	2.7V		The pin to be connected with a capacitor

Electrical Characteristics

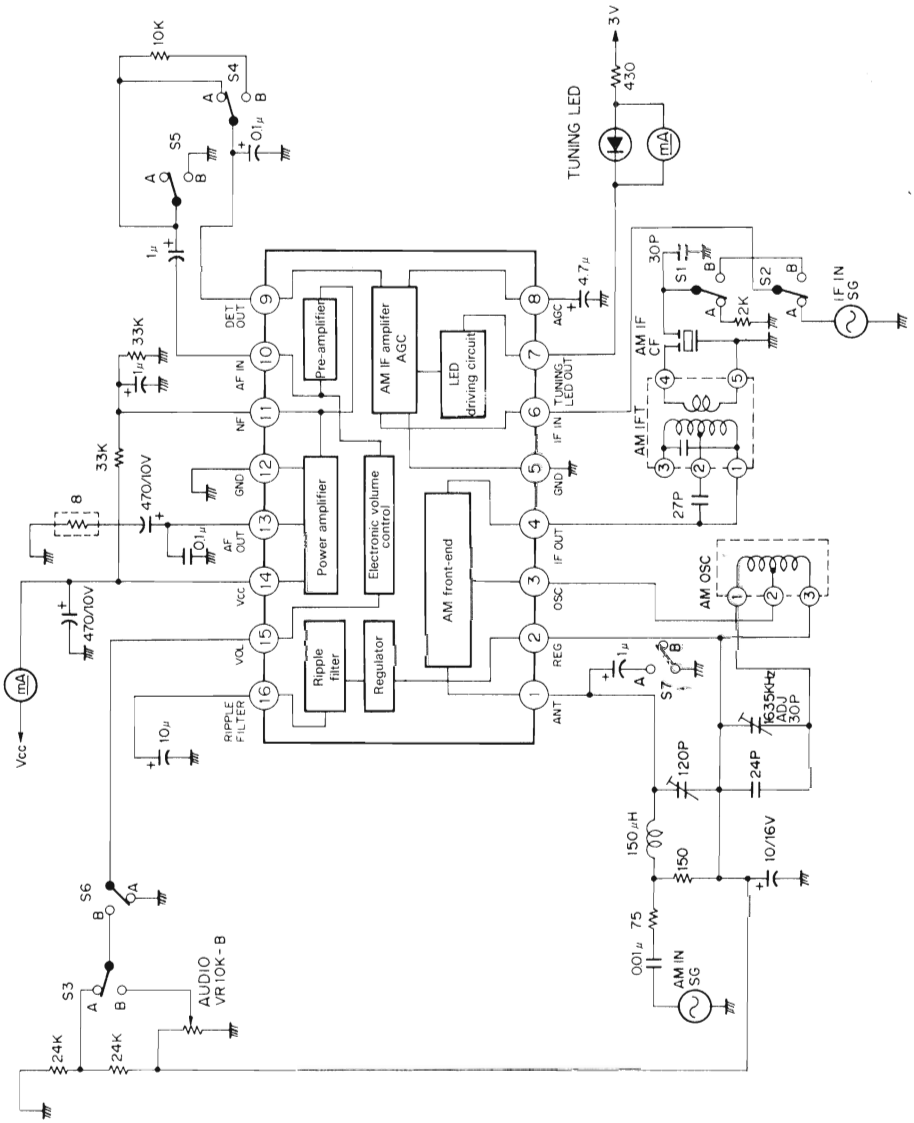
(Ta = 25°C, See the Electrical Characteristics Test Circuit)

	Item	Symbol	Switch mode							Test conditions	Min.	Typ.	Max.	Unit
			S1	S2	S3	S4	S5	S6	S7					
1	Non-signal circuit current	I_A	A	A	A	A	A	B	B	Measure current with an amperemeter by connecting it to the V_{CC} line when the level at AUDIO VR is set to Min.	2.0	3.3	4.5	mA
2	IF + AF output level (reduced voltage)	V_{B1}	A	A	B	A	A	B	B	IF IN = 455kHz +28dBμ, 1kHz30%MOD AUDIO VR = Max. V_{CC} = 2V Measure the clip output level at AF OUT.	−4	0	−	dBm
3	IF + AF voltage gain	G_{V1}	A	A	B	A	A	B	B	Measure the signal generator input level when the output level is set to −4 dBm.		23	29	dBμ
4	LED current	I_B	A	A	B	A	A	B	B	IF IN = 455kHz +85dBμ, 1kHz 30%MOD Measure current with an amperemeter.	1.4	2.5	4.0	mA
5	Front-end voltage gain	G_{V2}	B	B	B	A	A	B	B	AM IN = 1635kHz +60dBμ, No modulation. Measure voltage at IF OUT.	18	22	26	dB
6	EIAJ output (with 8-Ω load)	V_E	B	B	B	A	A	B	B	AM IN = 1635kHz +85dBμ, 1kHz 30%MOD Measure the output level where distortion factor becomes 10%.	1.85 (430)	2.1 (540)		V (mW)
7	Attenuation (1)	AT_1	B	B	A	B	A	A ↓ B	B	AM IN = 1635kHz +85dBμ, 1kHz 30%MOD Measure the difference between S6 A and B levels at AF OUT.	11	14	17	dB
8	Overall distortion factor	THD	B	B	B	A	A	B	B	AM IN = 1635kHz +95dBμ, 1kHz 30%MOD Measure the distortion factor when the output level at AF OUT is 0.63 Vrms.		0.6	2.5	%
9	Attenuation (2)	AT_2	B	B	B	A	A	B	B	AM IN = 1635kHz +85dBμ, 1kHz 30%MOD Measure the output level at AF OUT when the level at AUDIO VR is set to Min.		−76	−70	dBm
10	Overall noise level	AN	B	B	B	A	A	B	A	Short circuit at AM IN with a 1-μF capacitor. Measure the level at AF OUT when AUDIO VR is set to Max.		−28	−15	
11	Residual noise level	N	B	B	B	A	B	B	B	Measure the level at AF OUT with AM IN opened and AF IN short circuited.		−54	−48	

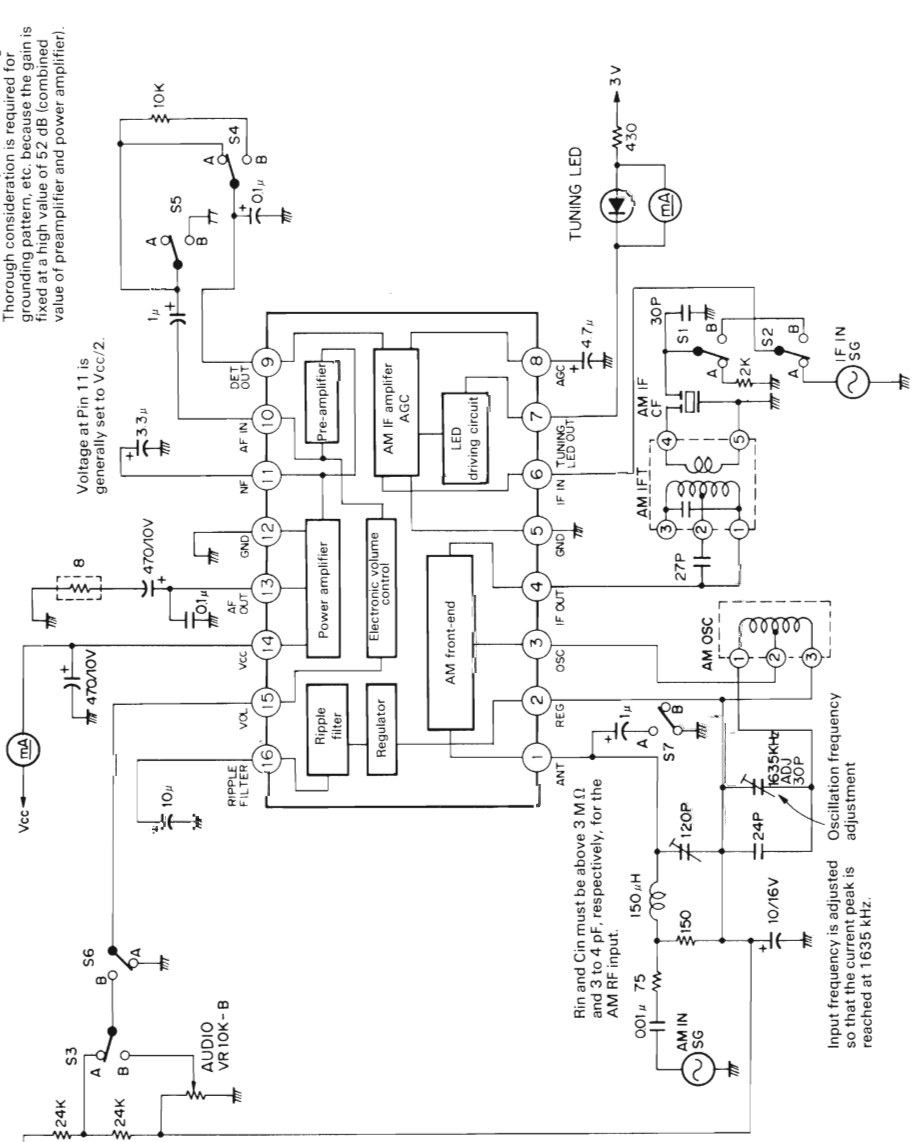
OdBm = 775mVrms

SONY

Electrical Characteristics Test Circuit



Description of Operation



Standard Circuit Design Data

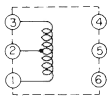
- **Pin Voltage**

No.	3V	6V	No.	3V	6V
1	1.25	1.25	9	1.35	1.35
2	1.25	1.25	10	0.69	0.69
3	1.25	1.25	11	1.5	3.0
4	0	0	12	GND	GND
5	GND	GND	13	1.5	3.0
6	0	0	14	V_{CC}	V_{CC}
7	1.6	4.5	15	1.25	1.25
8	1.35	1.35	16	2.7	5.4

Note) 1. All the above values represent standard values.
2. All the values were measured with the circuit shown below in non-signal and VOL MIN state.

Coil Data Wire diameter 0.08mmϕ UEW

AM OSC

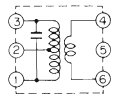


f (kHz)	L (μH)	Q_0	Number of turns (t)	
	1 - 3	1 - 3	1 - 2	2 - 3
796	270	110	30	60

7BRS-4718N of Toko Co., Ltd. or equivalent

Wire diameter 0.07mmϕ UEW

AM IFT

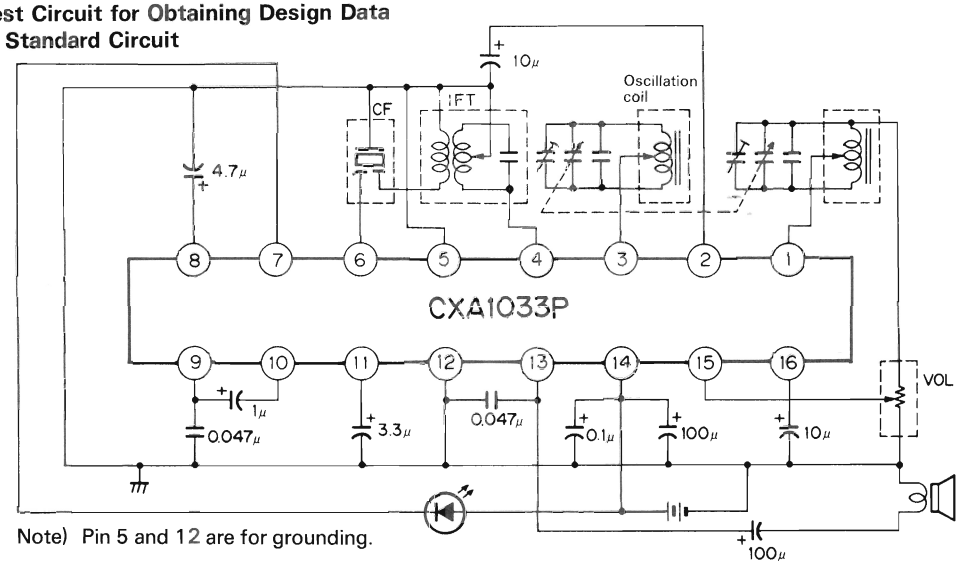


Co (pF)	f	Q_0	Number of turns (t)		
1 - 3	kHz	1 - 3	1 - 3	1 - 2	4 - 6
180	455	115	146	69	14

7MCS-4718N of Toko Co., Ltd. or equivalent

Ceramic Filter AHCF2-455AL of Toko Co., Ltd. or equivalent

Test Circuit for Obtaining Design Data of Standard Circuit

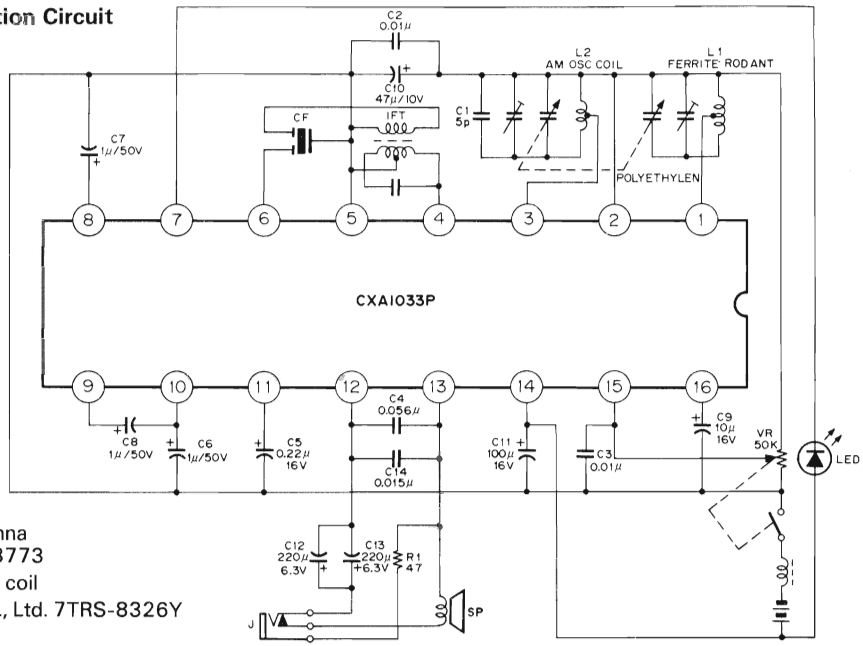


Note) Pin 5 and 12 are for grounding.

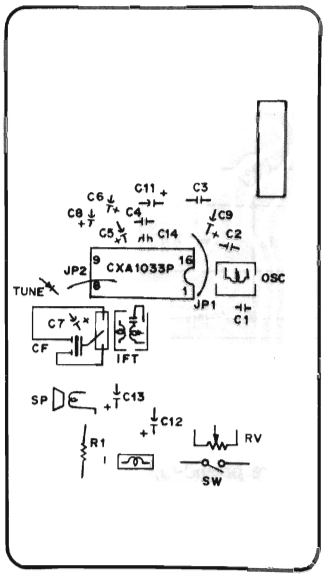
Notes on Application

1) Even though countermeasures against electrostatic damage are provided, take care when handling this IC to prevent pins from electrostatic damage.
2) Use SONY's specified parts for coil, ceramic filter, etc. as far as possible.

Application Circuit



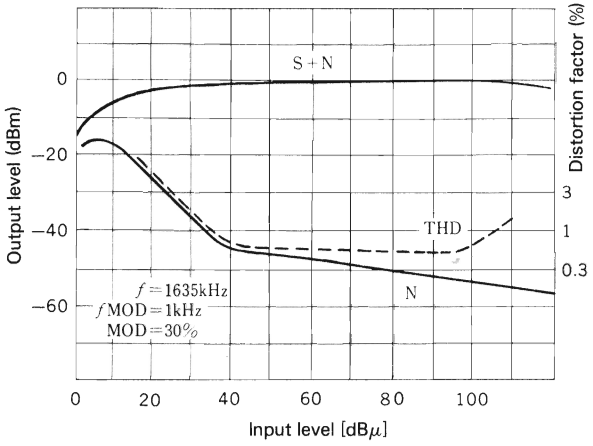
Bar antenna
CS-3773
AM OSC coil
Toko Co., Ltd. 7TRS-8326Y
AM IFT
Mitsumi Co., Ltd. R-12 4244
POLY variable capacitor
Mitsumi Co., Ltd. PVC-LYT
CF
Murata Co., Ltd. SFU-450B



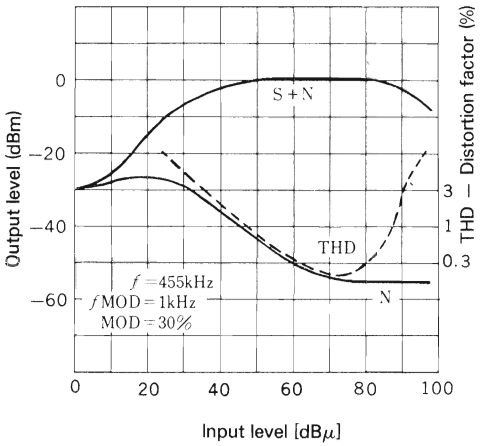
Parts arrangement

Pattern

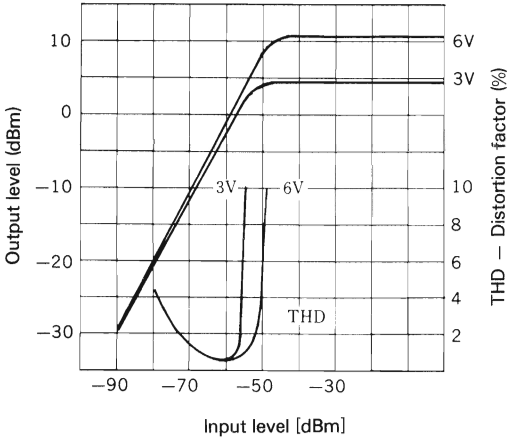
AM I/O characteristics



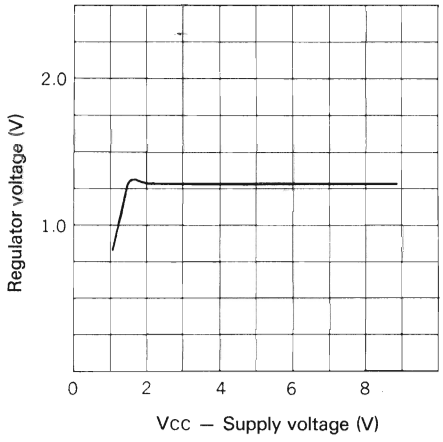
AM · IF I/O characteristics



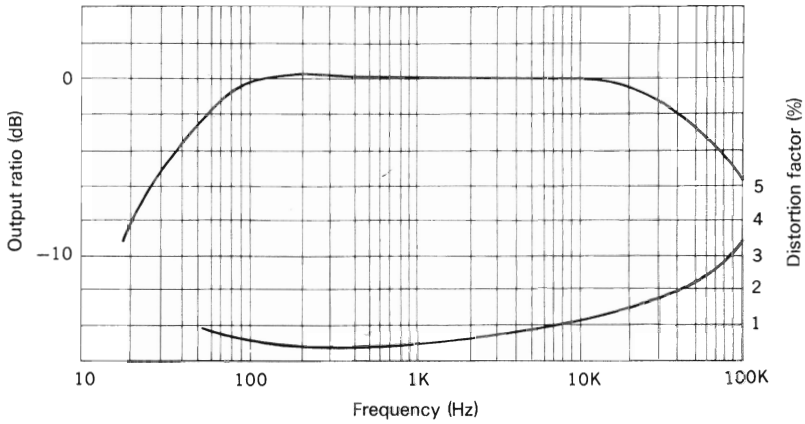
AF I/O characteristics



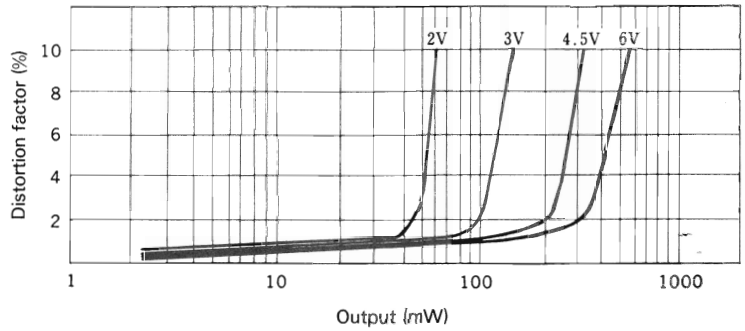
Regulator output — Supply voltage characteristics



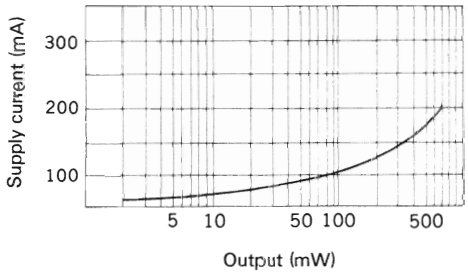
AF · frequency characteristics (AF only)



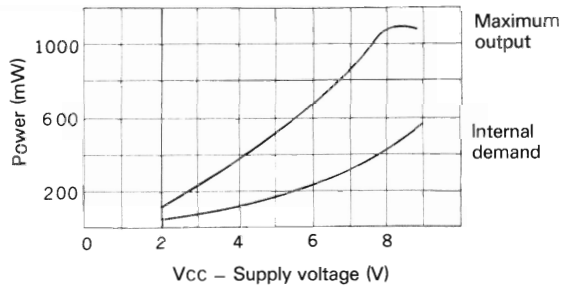
Distortion factor (AF only) — AF output



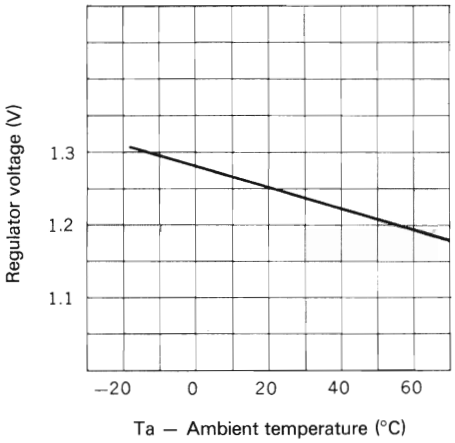
Supply current — Output characteristics



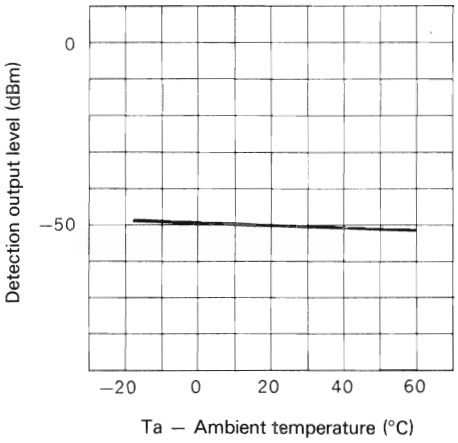
Maximum ouput and internal demand — Supply voltage



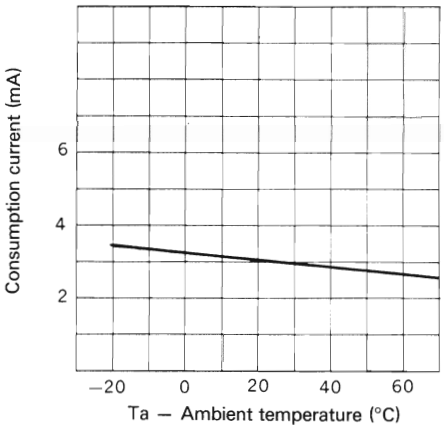
Temperature characteristics of regulator



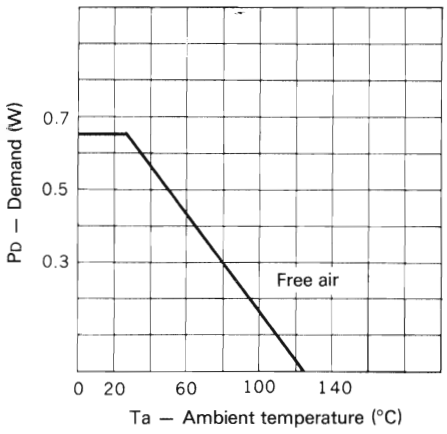
Temperature characteristics of detection output



Temperature characteristics of consumption current



Diminishing curve of maximumm demand



FM/AM Radio

Preliminary

Description

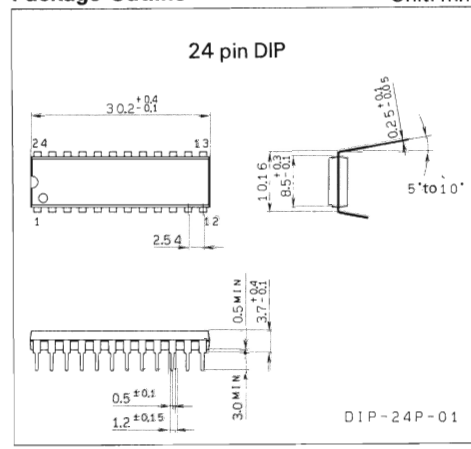
The CXA1111 is an IC designed for use in FM/AM radios, integrating all necessary functions from the front end to detector stage of a radio.

Features

- Wide application range as it contains functions from the front end to detector stage.
- Operable for a wide range of power supply voltages. (Vcc; 2 to 9V)
- Low current consumption. (For FM, I_D = 6.0 mA, for AM, I_D = 4.0 mA, at Vcc = 6V)
- Self contained LED drive circuit for tuning.
- Self contained FM band signal output circuit.
- Variable capacitance diode for FM AFC.
- Low distortion factor (0.1% typ.) for FM detection output.
- AM IF output pin which can be adapted for the AM stereo.
- Needs few peripheral parts. Due to its small size, a high density packaging design is possible.

Package Outline

Unit: mm



Structure

Bipolar silicon monolithic IC.

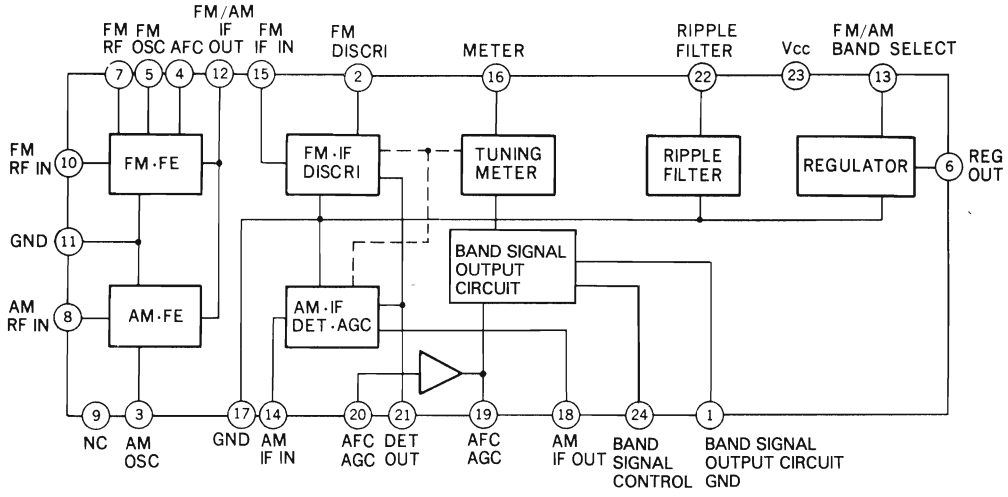
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	10	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

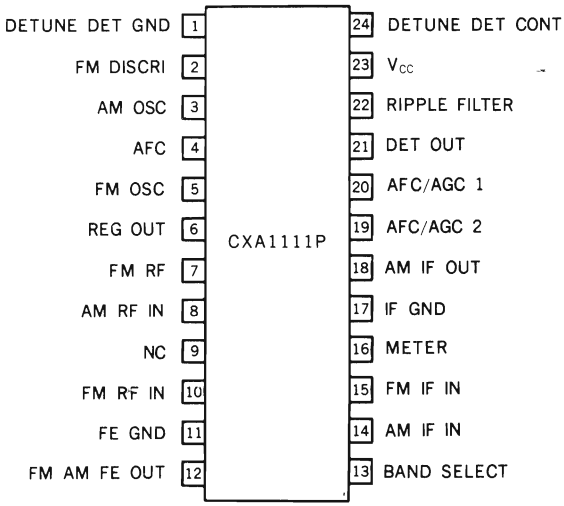
Recommended Operating Condition

• Supply voltage	2 to 9	V

Block Diagram



Pin Configuration



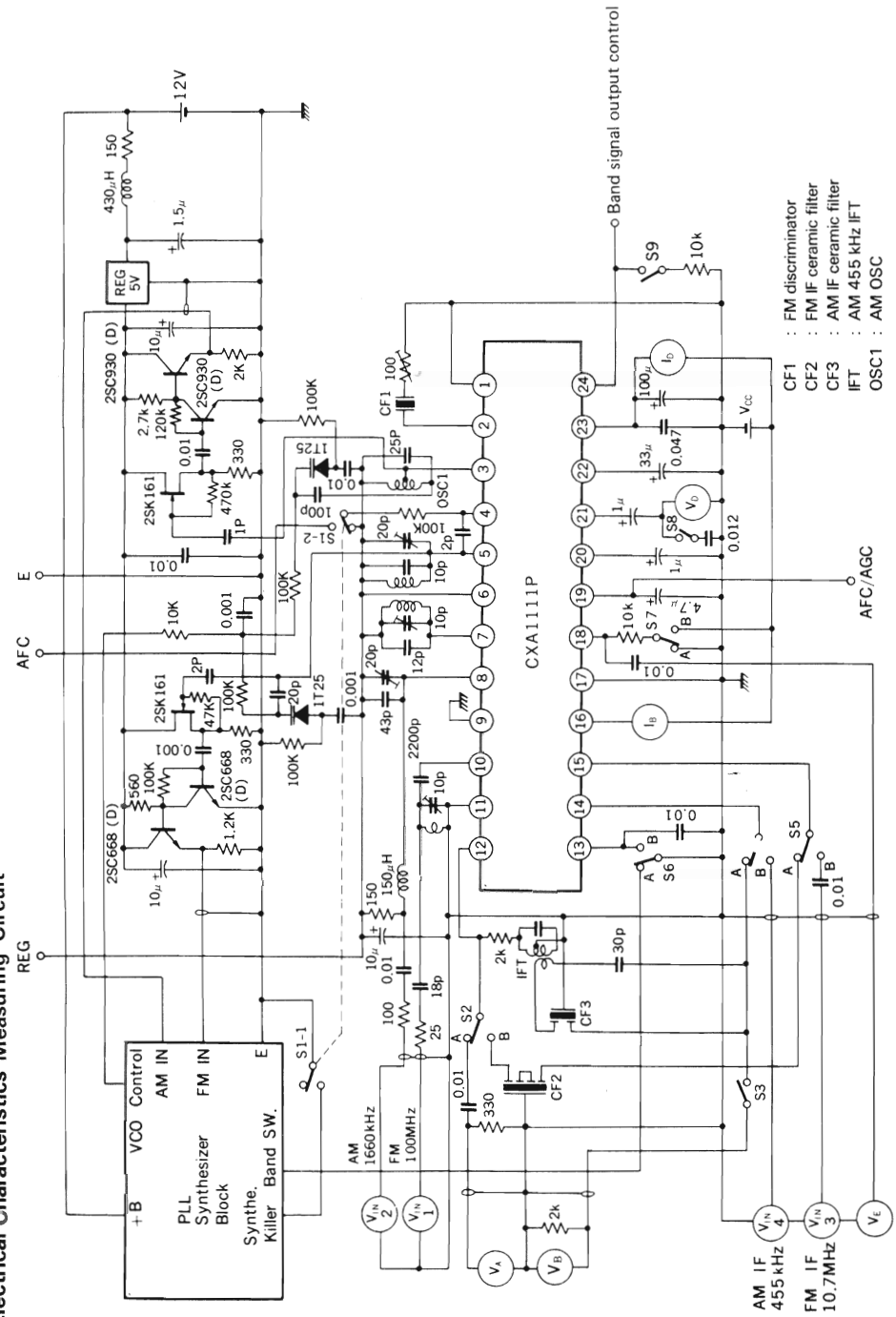
Pin Description

No.	Symbol	Function
1	GND	Ground for band signal output
2	FM DISCRI	Discriminator pin; to be connected to FM discriminator
3	AM OSC	AM local oscillator circuit
4	AFC	AFC input pin
5	FM OSC	FM local oscillator circuit
6	REG OUT	Regulator pin; 1.25V (typ.)
7	FM RF	FM RF input; connected to RF tank circuit
8	AM RF IN	AM RF input; connected to BAR ANT
9	NC	
10	FM RF IN	FM RF amplifier circuit; FM RF input
11	GND	Ground for front end
12	FM/AM FE OUT	IF output circuit for AM and FM; connected to AM and FM IF filters
13	BAND SELECT	Pin of FM and AM band switch; AM for "GND" and FM for "OPEN"
14	AM IF IN	Input stage of AM IF
15	FM IF IN	The first stage of FM IF amplifier circuit
16	METER	Meter drive circuit
17	IF GND	AM/FM IF stage; ground for detector stage
18	AM IF OUT	AM IF output; emitter output
19	AFC/AGC 2	AFC pin for W band; to adjust the time constant (using a condenser of external circuit) with AM
20	AFC/AGC 1	AFC pin for J band; to adjust the time constant (using a condenser of external circuit) with AM
21	DET OUT	Pin of detector output: impedence; approx. 5 kΩ
22	RIPPLE	The ripple filter: the hum suppression level of approximately 34.5 dB can be obtained by connecting a 10 μF condenser
23	Vcc	IC power supply
24	BAND SIGNAL OUTPUT CONTROL	Band signal output amplitude is adjusted by connecting an outside resistor

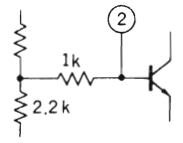
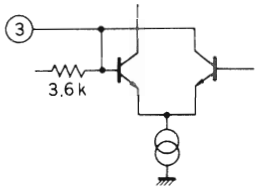
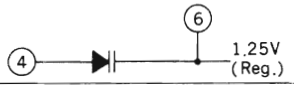
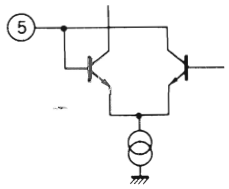
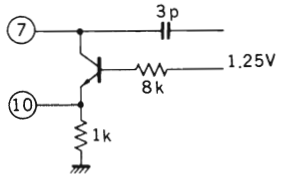
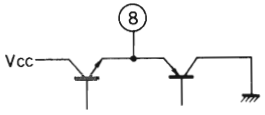
Electrical Characteristics (Ta = 25°C, See the Electrical Characteristics Measurement Circuit)

Test Number	Test Item	Symbol	Switch Position									Bias Condition				Test point	Output Waveform and Method of Measurement	Min.	Typ.	Max.	Units
			S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_{IN1}	V_{IN2}	V_{IN3}	V_{IN4}						
1	Circuit current (1)	ID_1	OFF	B	OFF	B	B	A	A	ON	OFF	OFF	OFF	OFF	OFF	I_D	Short circuit V_{IN1} through V_{IN4} when either AM signal of FM signal is not present	1.8	4.0	6.6	mA
2	Circuit current (2)	ID_2	↓	↓	↓	↓	↓	B	↓	↓	↓	↓	↓	↓	↓	I_D	↓	3.6	6.0	8.25	mA
3	FM front end voltage gain (a)	GV_1	ON	A	↓	↓	↓	↓	↓	↓	↓	ON	↓	↓	↓	V_A	V_{IN1} = 100 MHz 40 dBμV CW V_A = 10.7 MHz CW	33	39	45	dB
4	FM detector output level (1)	VD_1	OFF	B	↓	↓	↓	↓	↓	↓	↓	OFF	↓	ON	↓	V_D	V_{IN3} = 10.7 MHz 90 dBμV 1 kHz 22.5 kHz dev V_D = 1 kHz sin wave	−25.5	−22.5	−19.0	dBs
5	FM detector output level (2)	△VD	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	V_D	V_{D1} and V_{CC} = 9V: level difference with same value of V_{D1}	−4.0	−	+4.0	dB
6	FM IF knee level	VD_2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	V_{IN3}	V_{IN3} level is −3 dB with reference to V_{D1}	−	25	31	dBμ
7	FM detector output distortion factor (1)	THD_1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	V_D	V_{IN3} = 10.7 MHz 90 dBμV 1 kHz 75 kHz dev V_D = * kHz sin wave	−	0.1	1.1	%
8	Deviation of FM IF center frequency	F_1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	−	V_{IN3} = 10.7 MHz 90 dBμV CW	−55	C	55	kHz
9	FM meter current (1)	IB_1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	I_B	V_{IN3} = 10.7 MHz 60 dBμV CW	1.8	3.5	6.05	mA
10	FM band signal output band width	F_2	↓	↓	↓	↓	↓	↓	↓	↓	ON	↓	↓	↓	↓	I_B	V_{IN3} = 10.7 MHz ± 235 kHz Confirm I_B = 0 at 90 dBμV	±67.5	±110	±170.5	kHz
11	AM front end voltage gain (2)	GV_2	ON	↓	ON	↓	↓	A	↓	↓	OFF	↓	ON	OFF	↓	V_B	V_{IN2} = 1660 kHz 93 dBμV CW V_B = 455 kHz CW	19	24	28	dB
12	AM IF voltage gain (3)	GV_3	OFF	↓	OFF	↓	↓	↓	↓	↓	↓	↓	OFF	↓	ON	V_{IN4}	Level of V_{IN4} at V_D = −34 dBS	17	23	28	dBμ
13	AM IF voltage gain (4)	△GV	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	V_{IN4}	V_{CC} = 2V: level difference with same condition as GV_3	−4	0	3	dB
14	AM detector output level (3)	VD_3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	V_D	V_{IN4} = 455 kHz 85 dBμV 1kHz 30% MOD. V_D = 1 kHz sin wave	−25.5	−22.5	−19.0	dBs
15	AM meter current (2)	IB_2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	I_B	V_{IN4} = 455 kHz 85 dBμV CW	1.62	3.0	5.5	mA
16	AM IF output level	V_E	↓	↓	↓	↓	↓	↓	B	↓	↓	↓	↓	↓	↓	V_E	V_{IN4} = 455 kHz 85 dBμV CW V_E = 455 kHz CW	72	100	132	mV
17	AM detector output distortion factor (2)	THD_2	ON	↓	↓	A	↓	↓	A	↓	↓	↓	ON	↓	OFF	V_D	V_{IN2} = 95 dBμV 1660 kHz 1 kHz 30% MOD, V_D = 1 kHz sin wave V_{CC} = 7.8V	−	−0.6	1.1	%

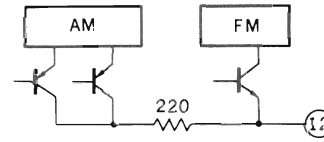
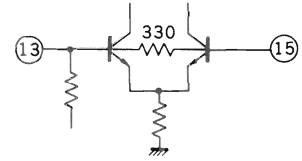
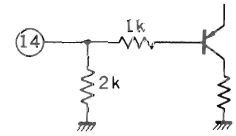
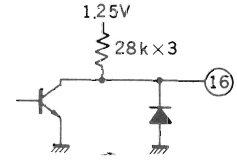
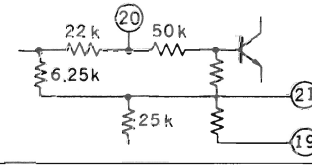
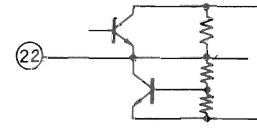
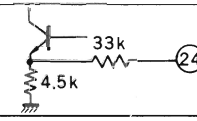
Electrical Characteristics Measuring Circuit



Standard Circuit Design Data

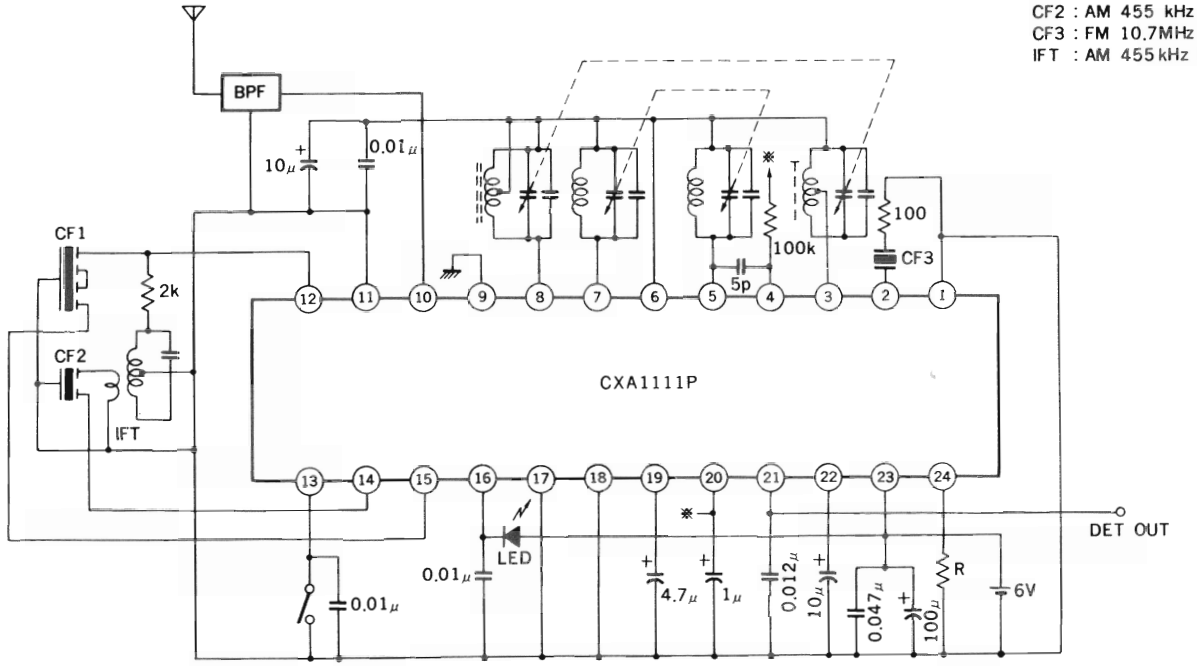
No.	Symbol	Pin Voltage (V)				Equivalent Circuit
		Vcc = 3V		Vcc = 6V		
		FM	AM	FM	AM	
1	GND	–	–	–	–	–
2	FM DISCRI	2.18	2.70	3.08	3.60	
3	AM OSC	1.25	1.25	1.25	1.25	
4	AFC	1.25	1.15	1.25	1.15	
6	REG OUT	1.25	1.25	1.25	1.25	
5	FM OSC	1.25	1.25	1.25	1.25	
7	FM RF	1.25	1.25	1.25	1.25	
10	FM RF IN	0.3	0	0.3	0	
8	AM RF IN	1.25	1.25	1.25	1.25	
9	NC	–	–	–	–	–
11	GND	–	–	–	–	–

*See the Voltage measurement circuit.
Values are typical values.

No.	Symbol	Pin Voltage (V)				Equivalent Circuit
		Vcc = 3V		Vcc = 6V		
		FM	AM	FM	AM	
12	FM/AM FE OUT	0.57	0.2	0.8	0.2	
13	BAND SELECT	1.25	0	1.25	0	
15	FM IF IN	1.25	0	1.25	0	
14	AM IF IN	0	0	0	0	
16	METER	1.6	1.6	4.5	4.5	
17	IF GND					
18	AM IF OUT					
19	AFC/AGC 2	1.15	1.47	1.15	1.47	
20	AFC/AGC 1	1.47	1.15	1.47	1.15	
21	DET OUT	1.0	1.0	1.0	1.0	
22	RIPPLE	2.7	2.7	4.0	4.0	
23	Vcc	3.0	3.0	6.0	6.0	
24	BAND SIGNAL OUTPUT CONTROL					

DC Voltage Measuring Circuit

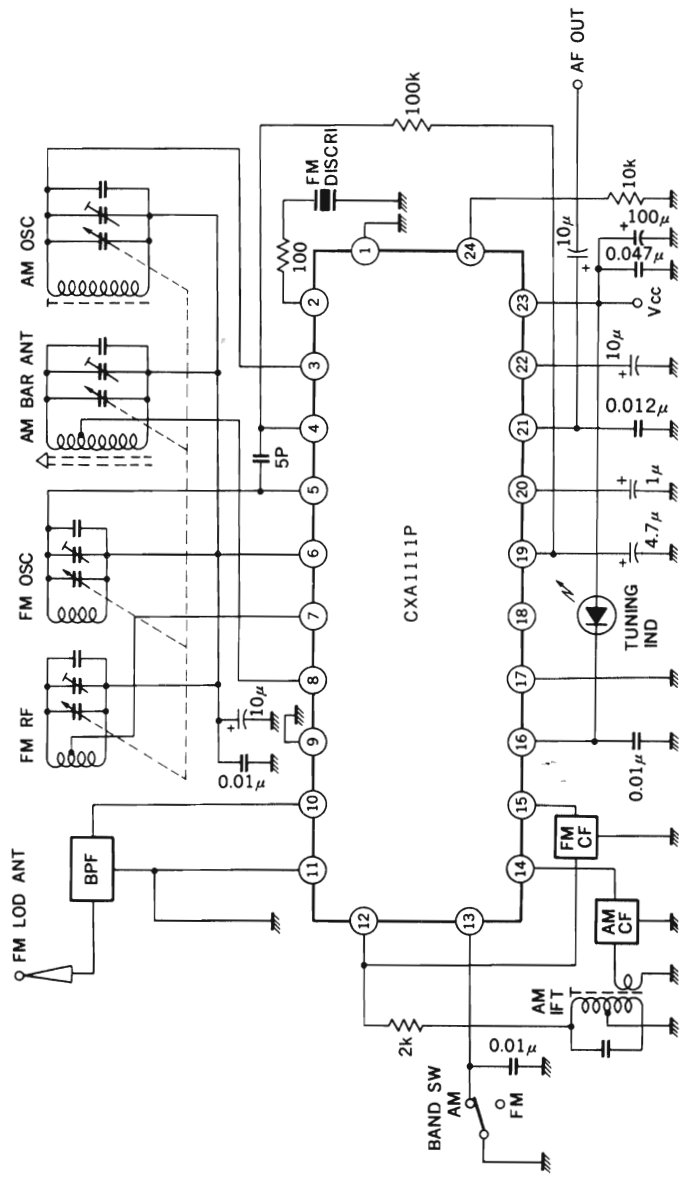
BPF : FM BAND PASS FILTER
CF1 : FM 10.7 MHz CF
CF2 : AM 455 kHz CF
CF3 : FM 10.7MHz DISCRI
IFT : AM 455 kHz IFT



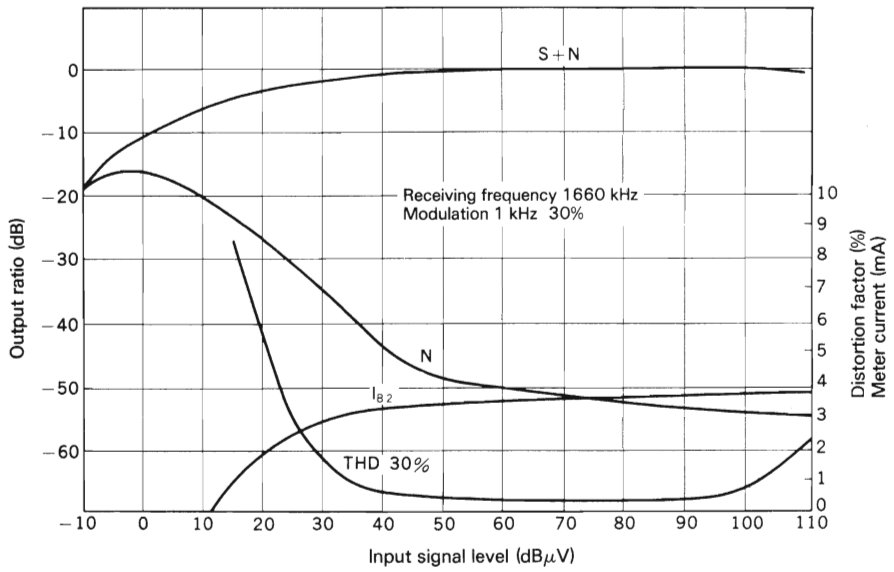
- The meter current is cut off under the following conditions: CDA 10.7MG1 (Murata Seisakusho Co.) is used as CF1, and the input frequency is either 10.7 MHz ± 100 kHz or more when R is 10 kΩ, or 10.7 MHz ± 150 kHz or more when R is 100 kΩ.
- The band signal output function cuts off the meter current when the signal is out of tuning by a specified frequency from the FM IF center frequency.
- The band signal output function is cut off when the voltage on pin 24 is the same as the regulator voltage or Vcc.

SONY

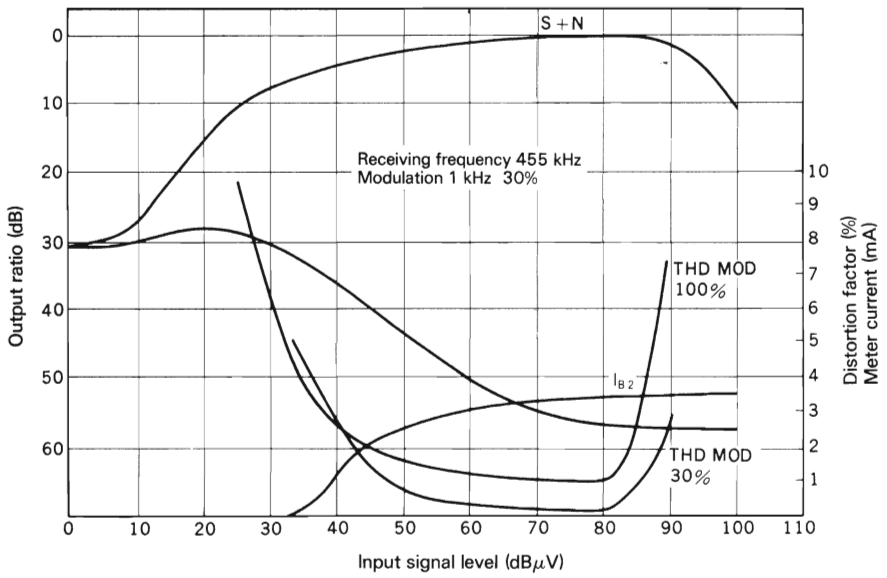
Application Circuit



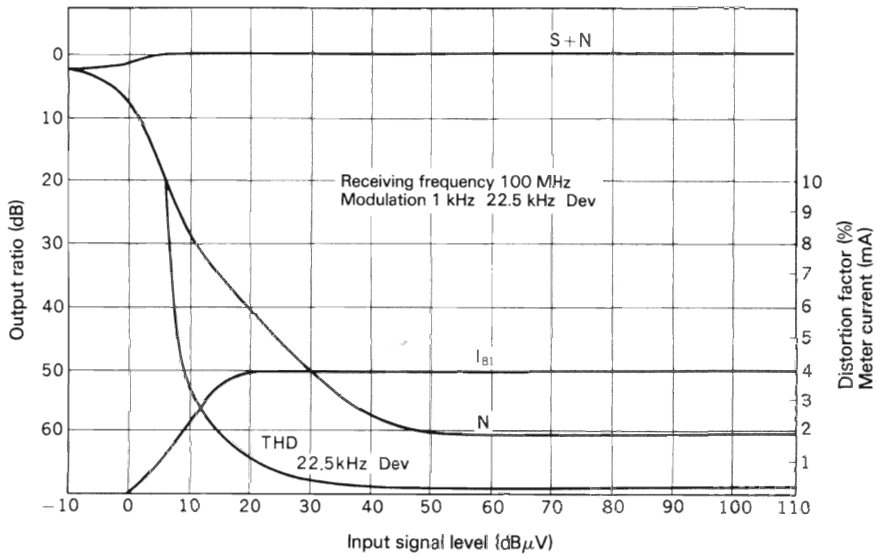
AM I/O Characteristics



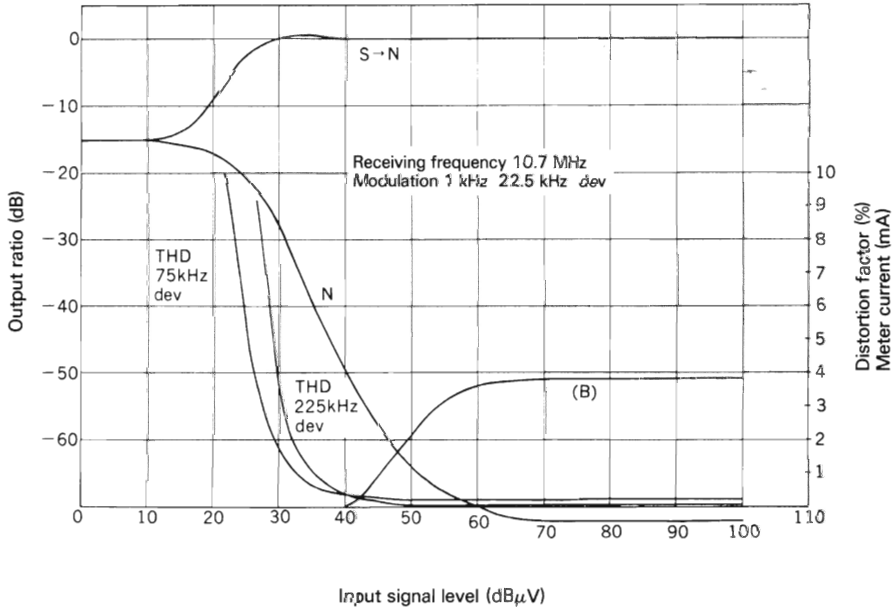
AM I/O Characteristics (IF single)



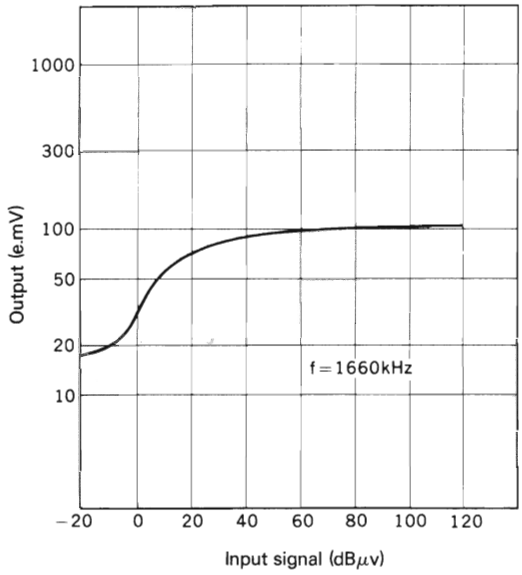
FM I/O Characteristics



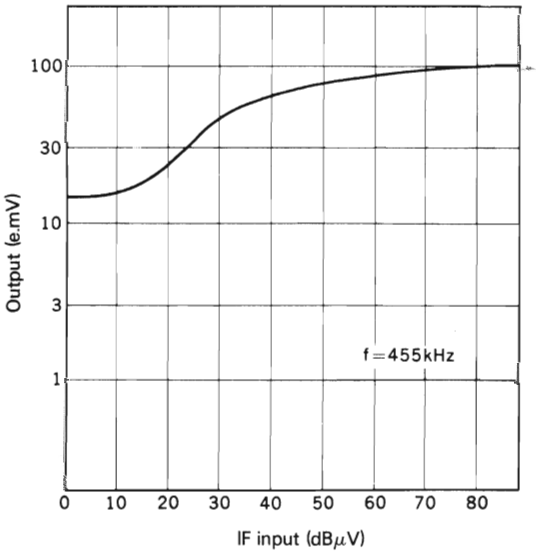
FM I/O Characteristics (IF single)



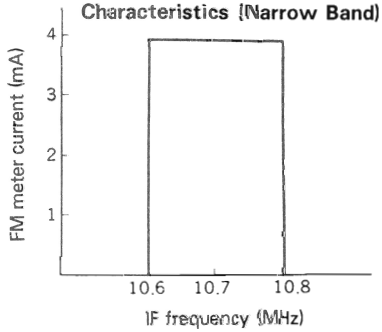
AM IF OUT Pin Output vs. Input (overall)



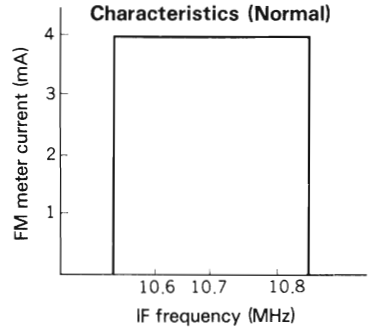
AM IF OUT Pin Output vs. Input



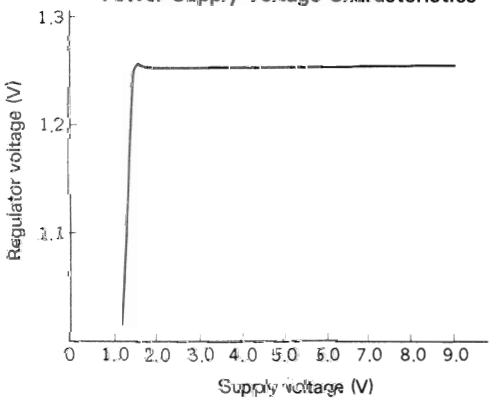
FM Band Signal Output Characteristics (Narrow Band)



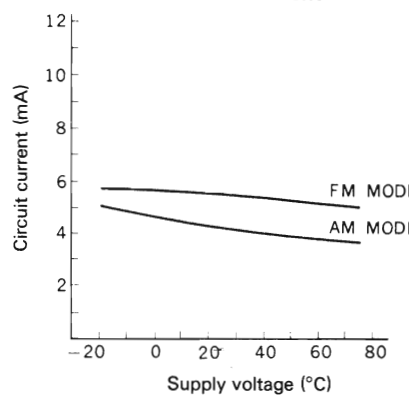
FM Band Signal Output Characteristics (Normal)



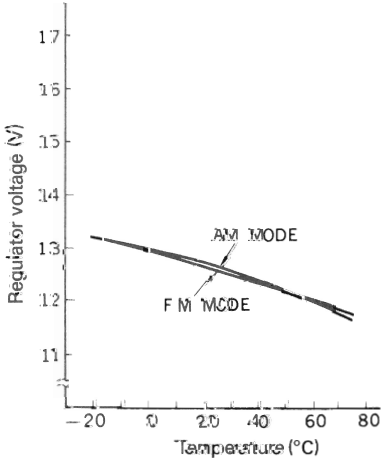
Regulator Output vs. Power Supply Voltage Characteristics



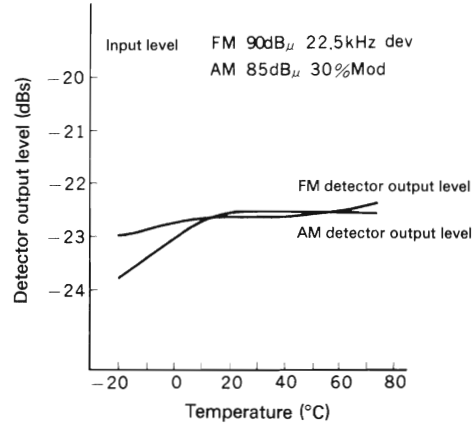
Temperature Characteristics of Circuit Current

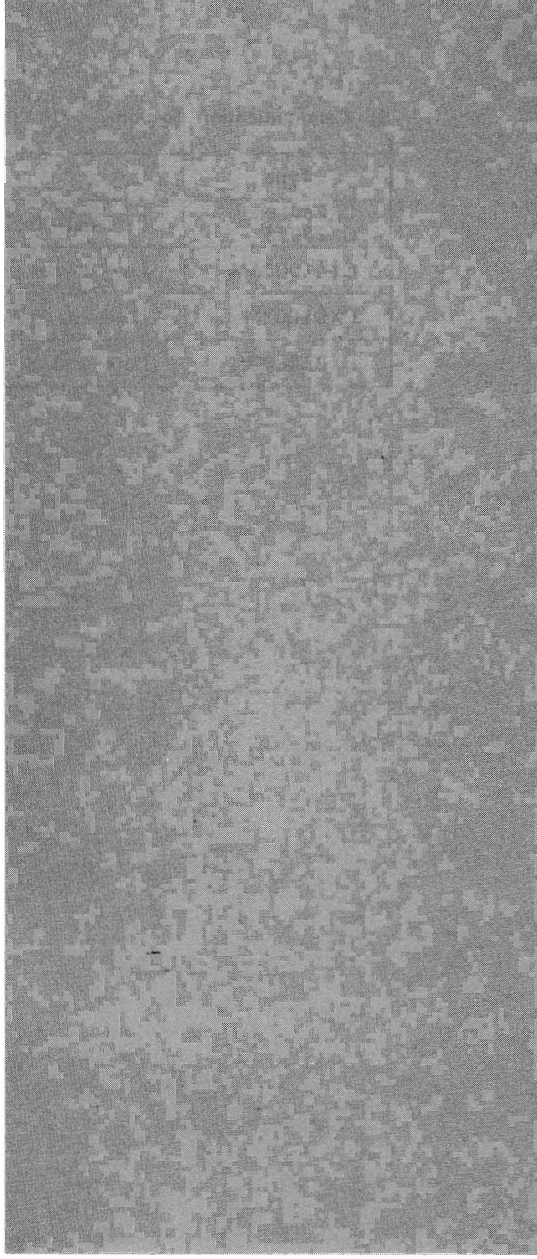


Regulator Temperature Characteristics

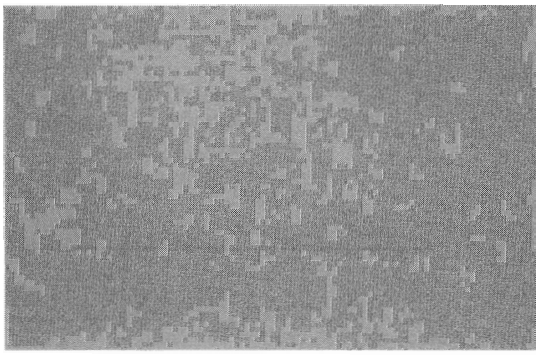


Temperature Characteristics of Detector Output Level





Communication System



5) Communication System

Type	Function	Page
CX23016 CX23086	Personal Radio MODEM	377
CXA1003AM	Low Power FM IF Amplifier	385
CXD1082M	Filter IC for Cellular Mobile Telephone	401
CXD1083Q	Data and SAT LSI for Cellular Radio Telephone	415

Personal Radio MODEM

Description

This LSI is a CMOS 1 chip MODEM for personal radio communication.

Structure

Silicon gate CMOS IC

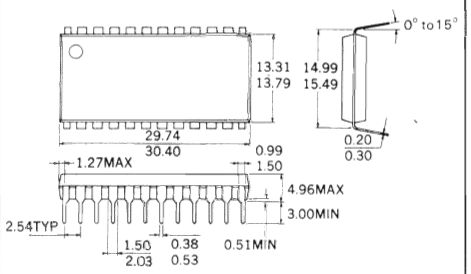
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	GND−0.3 to 7	V
• Input voltage	V_I	GND−0.3 to V_{DD}+0.3	V
• Output voltage	V_O	GND−0.3 to V_{DD}+0.3	V
• Output current	I_O	−10 to +10	mA
• Storage temperature	Tstg	−55 to +150	°C

Package Outline

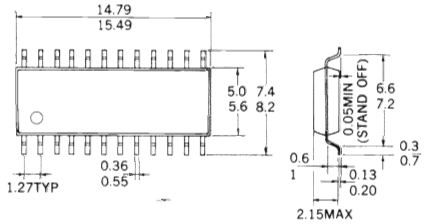
Unit: mm

CX23016 24 pin DIP



DIP-24P-021

CX23086 24 pin MFP

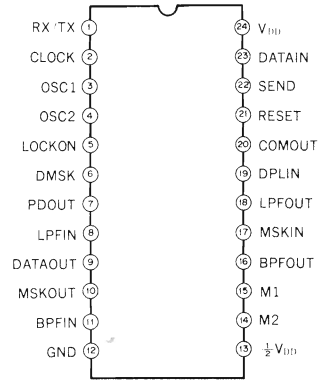


MFP-24P-L021

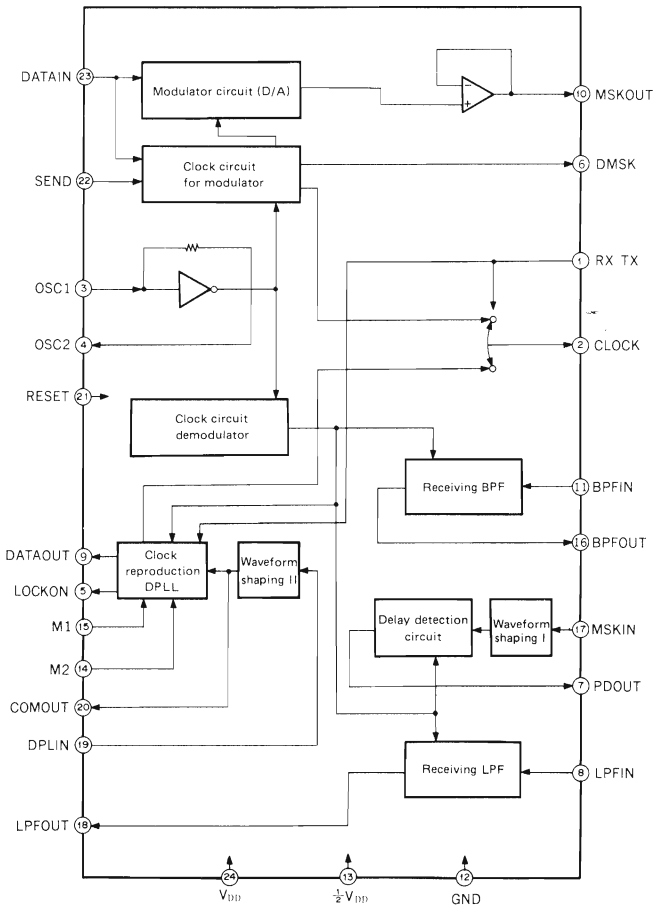
Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5 (5.0 Typ.)	V
• Input voltage	V_I	0 to V_{DD}	V
• Middle point loading capacity	C V_{DD}/2	3	μF
• Analog output loading resistance 1	RMO	−10	kΩ
• Analog output loading capacitance 1	CMO	30	PF
• Analog output loading resistance 2	RLO	−500	kΩ
• Analog output loading capacitance 2	CLO	15	PF
• OSC 1 pin loading capacitance	COSC1	25 to 100	PF
• OSC 2 pin loading capacitance	COSC2	25 to 100	PF
• Operating temperature	Topr	−10 to +60	°C

Pin Configuration (Top View)



Block Diagram



Pin Description

	No.	Name	Description
Power supply	24	V_{DD}	5V±10%
	12	GND	
	13	$\frac{1}{2}V_{DD}$	$\frac{V_{DD}}{2}$ current pin. Insert a capacitor between this pin and GND.
Input pin	3	OSC1	Crystal oscillator (3.6864MHz) connection pin 1.
	21	RESET	Reset signal input pin. All the circuits are reset at "L". During operation at "H" or "Open".
	22	SEND	Operates at "L" → "H" after reset pin at "H" or "Open".
	23	DATA IN	Transmission data input. During at "H", D MSK, MSK OUT and outputs 1.2kHz. During at "L", D HSK, MSK OUT and outputs 1.8kHz.
	11	BPF IN	Demodulation wave input pin. Input to the receiving BPF.
	17	MSK IN	Delay detection circuit input pin. It is directly connected or C-coupled to the BPF OUT.
	8	LPF IN	Input pin of the receiving LPF. It is directly connected to the PD OUT.
	19	DPL IN	Input pin of the clock reproduction circuit. It is directly connected to the LPF OUT.
	15	M1	D PLL control signal 1
	14	M2	D PLL control signal 2
	1	RX/TX	Transmission and receiving clock output control signal. During at "H", it outputs transmission clock (1.2kHz) from the CLOCK pin, and the DATA OUT becomes "L" and the LOCK ON becomes "H". During at "L", outputs receiving clock (1.2kHz) from the CLOCK pin.
Output pin	4	OSC2	Crystal oscillator (3.6864MHz) connection pin 2.
	6	D MSK	It outputs 1.2kHz when the DATA IN is at "H", 1.8kHz when the DATA IN is at "L", and "L" when the RESET is at "L".
	10	MSK OUT	Modulation wave output pin. It outputs $\frac{V_{DD}}{2}$ when the RESET is at "L".
	16	BPF OUT	Output pin of the receiving BPF.
	7	PD OUT	Output pin of the delay detection circuit.
	18	LPF OUT	Output pin of the receiving LPF.
	9	DATA OUT	Reproduce data output signal.
	5	LOCK ON	D PLL output pin.
	2	CLOCK	Transmission/receiving clock output pin. It outputs transmission clock (1.2kHz) when TX is at "H", and receiving clock (1.2kHz) when at "L".
	20	COM OUT	Output pin of the waveform shaping II.

Electrical Characteristics

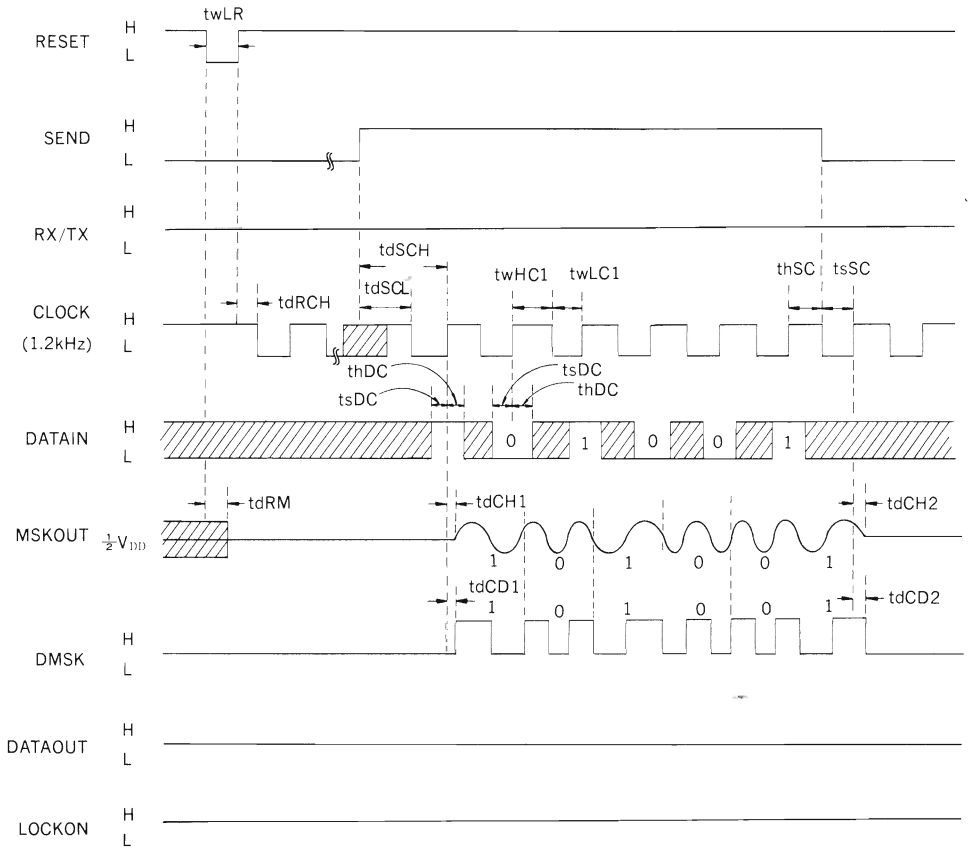
Item	Symbol	Name	Test condition	Min.	Typ.	Max.	Unit
Power supply current	I_{DD}	V_{DD}				10	mA
Digital input "L" voltage	V_{IL}	RESET, SEND, DATA, IN, M1, M2, RX/TX		0		0.8	V
Digital input "H" voltage	V_{IH}	RESET, SEND, DATA IN, M1, M2, RX/TX		2.2		V_{DD}	V
Digital input "L" current	I_{IL}	SEND, DATA IN, M1, M2, RX/TX	V_I=GND	−10		0	μA
Digital input "H" current	I_{IH}	RESET, SEND, DATA IN, M1, M2, RX/TX	V_I=V_{DD}	0		10	μA
Pull-up current	IPLU	RESET	V_I=GND	−200	−100	−50	μA
Digital output "L" voltage	V_{OL}	D MSK, DATA OUT, LOCK ON, CLOCK	I_{OL}=2.0mA	0		0.4	V
Digital output "H" voltage	V_{OH}	D MSK, DATA OUT, LOCK ON, CLOCK	I_{OH}=1.0mA	2.4		V_{DD}	V
Oscillation frequency	OSC IN	OSC1, OSC2			3.6864		MHz
Analog input resistance 1	RAIN1	PBF IN	Between $-\frac{1}{2}$ input pin V_{DD}	50	100	200	kΩ
Analog input resistance 2	RAIN2	LPF IN	Between $-\frac{1}{2}$ input pin V_{DD}	100			kΩ
Analog input resistance 3	RAIN3	MSK IN		200			kΩ
Analog input voltage 1	AIN1	BPF IN	When direction coupling of the BPF OUT and MSK IN	1.0		2.5	Vp-p
			When C-coupling of the BPF OUT and MSK IN	0.3		2.5	Vp-p
Analog input voltage 2	AIN2	MSK IN	When C-coupling	0.27		2.8	Vp-p

Item	Symbol	Name	Test condition	Min.	Typ.	Max.	Unit
Analog output voltage 1	AOUT1	MSK OUT	During operation	0.8	1.0	1.2	Vp-p
			Offset voltage during operation	$\frac{V_{DD}}{2}$−0.3	$\frac{V_{DD}}{2}$	$\frac{V_{DD}}{2}$+0.3	V
			RESET "L"	$\frac{V_{DD}}{2}$−0.3	$\frac{V_{DD}}{2}$	$\frac{V_{DD}}{2}$+0.3	V
Receiving BPF absolute gain	ABS1		Input frequency 1500Hz	−1.5	0	+1.0	dB
Input BPF frequency characteristics	F1		0−200Hz 900−1200Hz 1200−1800Hz 1800−2100Hz 3000−5000Hz Reference frequency 1500Hz	 −3.5 −1.2 −4.0 		−20.0 −33.0	dB dB dB dB dB
Receiving LPF cutoff frequency	Fo		3dB down		800		Hz
Receiving LPF absolute gain	ABS2		0Hz<input frequency≦300Hz		−6.0		dB
Transmission clock delay time 1	tdRCH	CLOCK	RX/TX="H"	0	150	417	μs
Transmission clock delay time 2	tdSCH	CLOCK	RX/TX="H"	417	570	834	μs
Transmission clock delay time 3	tdSCL	CLOCK	RX/TX="H"	0	150	417	μs
Transmission clock "H" width	twHC1	CLOCK	RX/TX="H"	390	417	444	μs
Transmission clock "L" width	twLC1	CLOCK	RX/TX="H"	390	417	444	μs
SEND setup time	tsSC	SEND	RX/TX="H"	1			μs
SEND holding time	thSC	SEND	RX/TX="H"	1			μs
DATA IN setup time	tsDC	DATA IN	RX/TX="H"	1			μs
DATA IN holding time	thDC	DATA IN	RX/TX="H"	1			μs
MSK OUT output delay time 1	tdCM1	MS OUT	RX/TX="H"	−10		10	μs
MSK OUT output delay time 2	tdCM2	MSK OUT	RX/TX="H"	−10		10	μs

Item	Symbol	Name	Test condition	Min.	Typ.	Max.	Unit
DMSK output delay time 1	tdCD1	D MSK	RX/TX="H"	−1		1	μs
DMSK output delay time 2	tdCD2	D MSK	RX/TX="H"	−1		1	μs
BPF IN invalid time	tdRB	BPF IN		0		10	ms
Lead-in bit number	N		RX/TX="L", M1=M2="L" During BPF IN non-noise			15	bit
Demodulator delay time	tdBD	DATA OUT	RX/TX="L", M1=M2="L" N≧15, During BPF IN non-noise	1483	1900	2317	μs
DATA OUT timing	tdCD	DATA OUT	RX/TX="L"	−1		1	μs
Receiving clock "H" width	twHC2	CLOCK	RX/TX="L", M1=M2="L" N≧ During BPF IN non-noise	338	417	496	μs
Receiving clock "L" width	twLC2	CLOCK	RX/TX="L", M1=M2="L" N≧15, During BPF IN non-noise	338	417	496	μs
RESET "L" width	twLR	RESET		20			μs
MSK OUT output delay time 3	tdRM	MSK OUT		0		10	μs
Transmission clock delay time 4	tdTC4	CLOCK		0		2	μs
Transmission clock delay time 1	tdRC1	CLOCK		0		2	μs

Timing Chart

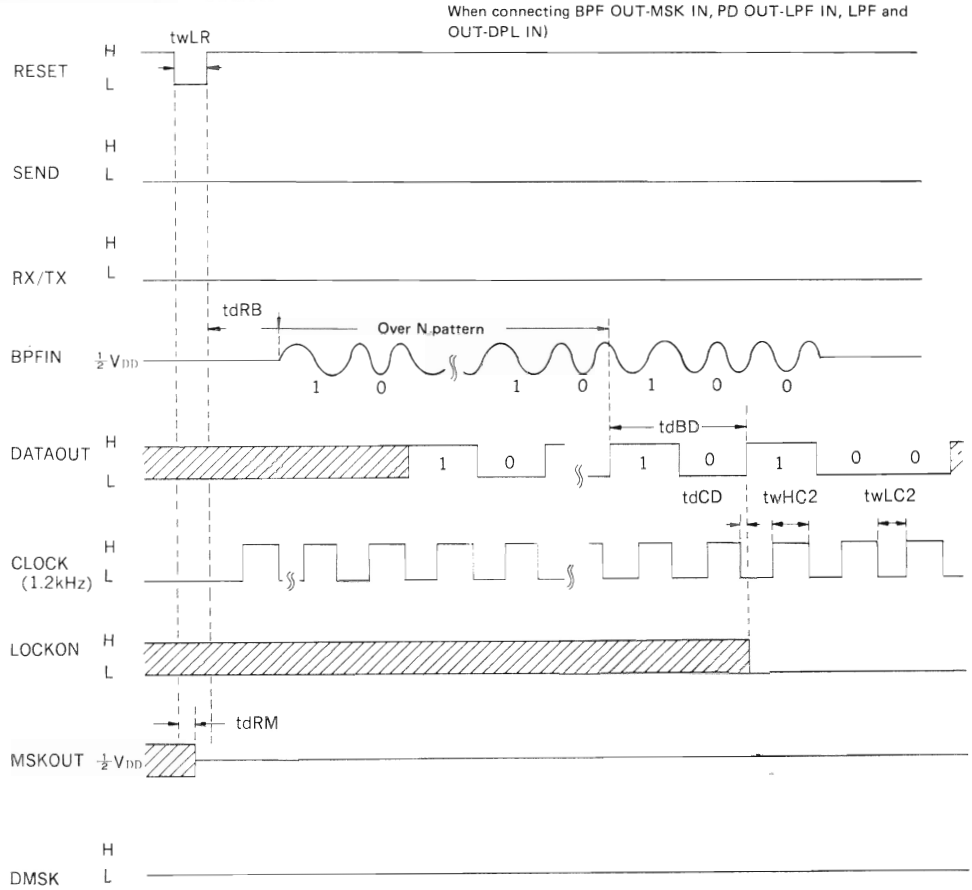
1. Modulation section



Note)

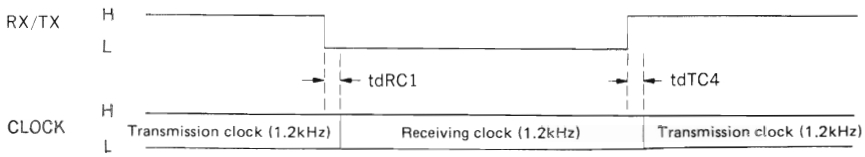
- The SEND pin turns the RESET pin to "H" from "L" after having turned it "H" or open from "L".
- The DATA IN signal reads in the data at the rising of the CLOCK.
- When the SEND pin is turned to "H" from "L", the CLOCK pin is once set at "H", then it outputs 1.2kHz of clock.
- When the RX/TX pin is at "H", the DATA OUT pin outputs "L" and the LOCK ON pin outputs "H".
- After turning the power ON, set the RESET pin once into "L" to reset all the circuits for use.

2. Demodulation section



Note)
- DATA OUT outputs synchronous with falling of CLOCK.
- Fix the SEND pin at "H" or "L" during using the demodulation section. When the SEND pin is fixed at "L", the MSK OUT pin outputs "$\frac{1}{2}$ V_{DD}" and the D MSK pin outputs "L".
- The LOCK ON pin is fixed at "L" after the O PIL circuit has been locked.
- After turning the power ON, set the RESET pin once into "L" to reset all the circuits and then use.

3. Clock output



Low Power FM IF Amplifier

Description

CXA1003AM is a single-chip IC for FM Radio such as cellular mobile, etc.. Its outline is 24 pin MFP.

Features

- It includes all the functions needed to the cellular mobile such as second mixer, FM detecting circuit, muting circuit, RSSI, etc..
- It has wide operating voltage (4.5 to 9.5V) and low current consumption. (During V_{CC}=5V, I_{CC}=6.6 mA Typ.)
- It includes the audio output buffer, so it needs small number of peripheral parts.
- It has wide RSSI range and excellent temperature characteristics.

Functions

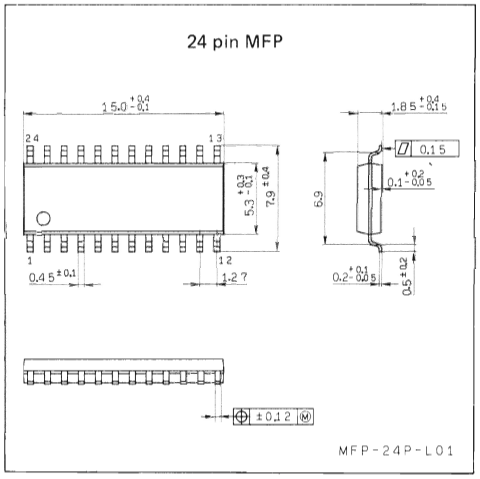
- Second mixer and oscillation circuit
- IF amplifier and limiter
- RSSI (Received Signal Strength Indicator)
- FM detecting circuit
- Muting circuit

Structure

Bipolar silicon monolithic IC

Package Outline

Unit: mm



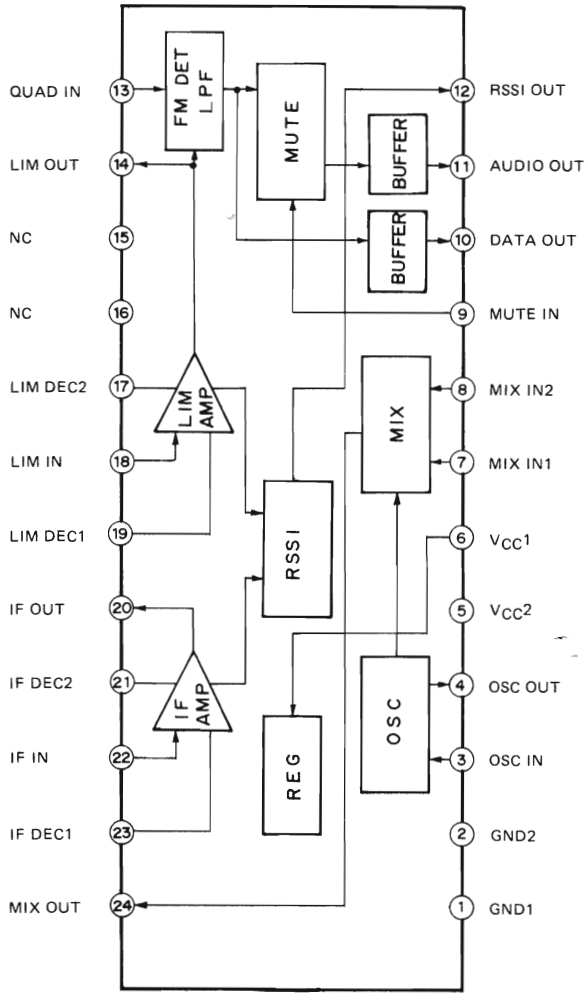
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	17	V
• Operating temperature	Topr	−35 to +85	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	780	mW

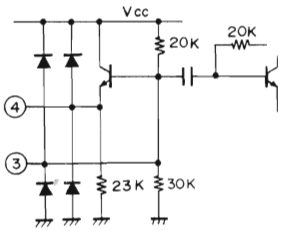
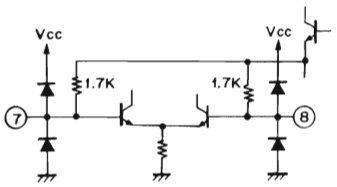
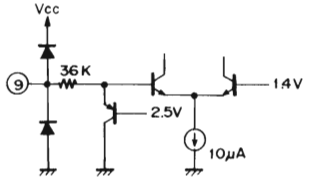
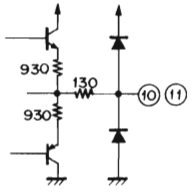
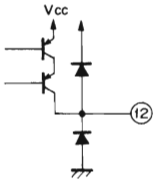
Recommended Operating Condition

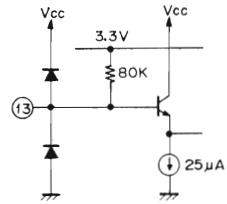
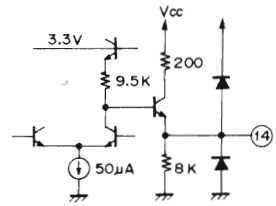
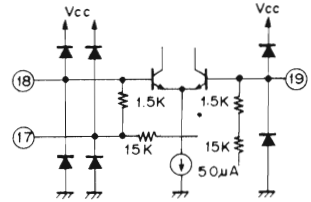
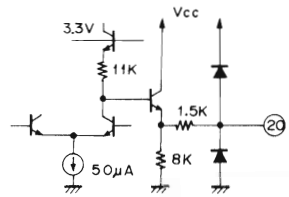
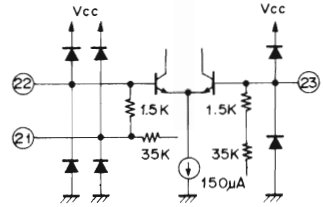
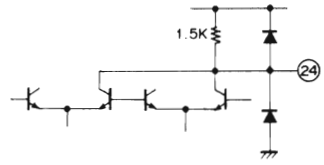
• Supply voltage	V_{CC}	4.5 to 9.5	V

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Name	Voltage (Typ.)	Equivalent circuit	Description
1 2	GND1 GND2	0V		Grounding pin
3 4	OSC IN OSC OUT	3.0V 2.3V		Connect a crystal oscillator to compose a Colpitts type oscillation circuit. In case of using an external oscillator, input a signal to pin ③ and connect pin ④ to Vcc.
5 6	Vcc2 Vcc1	5.0V		Power supply pin
7 8	MIX IN1 MIX IN2	1.2V 1.2V		Input pin of mixer. In case of using a single input, connect pin ⑧ to GND with capacitor.
9	MUTE IN			Control pin of pin ⑪ ; audio output. A signal is output at L (<0.8V), and is muted at H (>2.0V).
10 11	DATA OUT AUDIO OUT	2.5V 2.5V		FM detected signal is output. The output of pin ⑪ can be muted by the input of pin ⑨ .
12	RSSI OUT			Output current is corresponding to a input signal level.

No.	Name	Voltage (Typ.)	Equivalent circuit	Description
13	QUAD IN	3.3V		Input pin of quadrature detecting circuit. Connect a resonance circuit between pin ⑬ and ⑭
14	LIM OUT	1.7V		Output pin of limiter.
17 18 19	LIM DEC2 LIM IN LIM DEC1	1.7V 1.7V 1.7V		Input and decoupling pin of limiter. Connect pin ⑰ and ⑲ to GND with capacitor (0.01 to 0.047μF).
20	IF OUT	1.6V		Output pin of IF amp.
21 22 23	IF DEC2 IF IN IF DEC1	1.6V 1.6V 1.6V		Input pin and decoupling pin of IF amp. Connect pin ㉑ and ㉓ to GND with capacitor (0.01 to 0.047μF).
24	MIX OUT	3.8V		Output pin of mixer.

Electrical characteristics

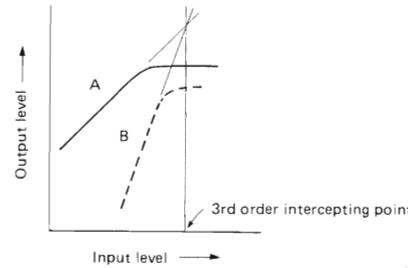
(T_a=25°C, V_{CC}=5V See the Electrical Characteristics Test Circuit)

0 dBm=223.6 mVrms

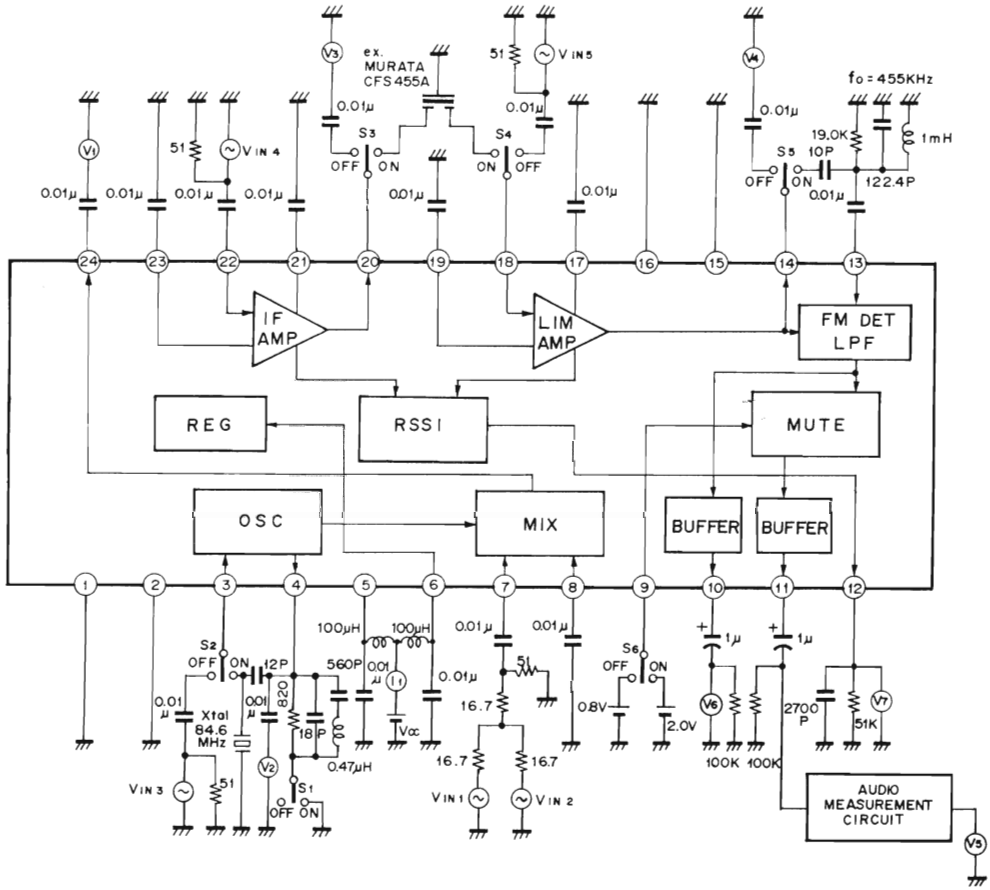
No.	Item	Symbol	SW which turns ON	Input signal, No.	Remark	Test point	Min.	Typ.	Max.	Unit
1	Consumption current	I_{CC}				I_1	5.7	6.6	8.0	mA
2	Mixer conversion gain	VG1		V_{IN1}: 80MHz −40dBm V_{IN3}: 80.455MHz 0dBm	f_{OUT}=455kHz Output level of 455kHz component Input level of pin ⑦.	V_1	18	20	22	dB
3	3rd order intercepting point	IM1		V_{IN1}: 80.06MHz V_{IN2}: 80.12MHz V_{IN3}: 80.455MHz 0dBm	f_{OUT}=455kHz See Note 1	V_1	−6.0	−4.5		dBm
4	Oscillator output voltage	VO1	S1, S2		0dB=223.6mVrms	V_2	−5	0	+5	dB
5	IF amp voltage gain	VG2		V_{IN4}: 455kHz −50dBm		V_3	34	36	38	dB
6	Limiter voltage gain	VG3		V_{IN5}: 455kHz −90dBm		V_4	70	72	74	dB
7	Limiter output voltage	VO3		V_{IN5}: 455kHz −20dBm		V_4	500	570	640	mVp-p
8	Audio output voltage	VO4	S5	V_{IN5}: 455kHz −20dBm	f_{AUDIO}=1kHz DEV=±8kHz FM	V_5	155	195	245	mVrms
9	Audio output distortion	VD4		V_{IN5}: 455kHz −20dBm	f_{AUDIO}=1kHz DEV=±8kHz FM	V_5			1	%
10	Audio output S/N	SN4		V_{IN5}: 455kHz −20dBm		V_5	40			dB
11	Audio output AMRR	AR4		V_{IN5}: 455kHz −20dBm	f_{AUDIO}=1kHz MOD=±80% AM	V_5	30			dB
12	Crosstalk in muting	MX4	S6	V_{IN5}: 455kHz −20dBm	f_{AUDIO}=1kHz DEV=±8kHz FM	V_5			−65	dB
13	Data output voltage	VO5	S5	V_{IN5}: 455kHz −20dBm	f_{AUDIO}=1kHz DEV=±8kHz FM	V_6	155	195	245	mVrms
14	RSSI output voltage L	VO6	S3, S4	V_{IN4}: 455kHz −100dBm		V_7	0.25	0.40	0.55	V
15	RSSI output voltage H	VO7	S3, S4	V_{IN4}: 455kHz −20dBm		V_7	1.50	1.85	2.20	V

Note) See next page

Note) Definition of the 3rd order intercepting point. The 3rd order intercepting point is determined by the input level of pin ⑦ at the tangent intersection of A and B. A and B is 455 kHz component in case of 1 and 2. In case 1, V_{IN1} is 80 MHz, V_{IN2} is terminated by 50Ω and V_{IN3} is 0 dBm 80.455 MHz. In case 2, V_{IN1} is 80.06 MHz, V_{IN2} is 80.12 MHz (level of V_{IN1} and V_{IN2} is eaqual) and V_{IN3} is 0 dBm 80.455 MHz.

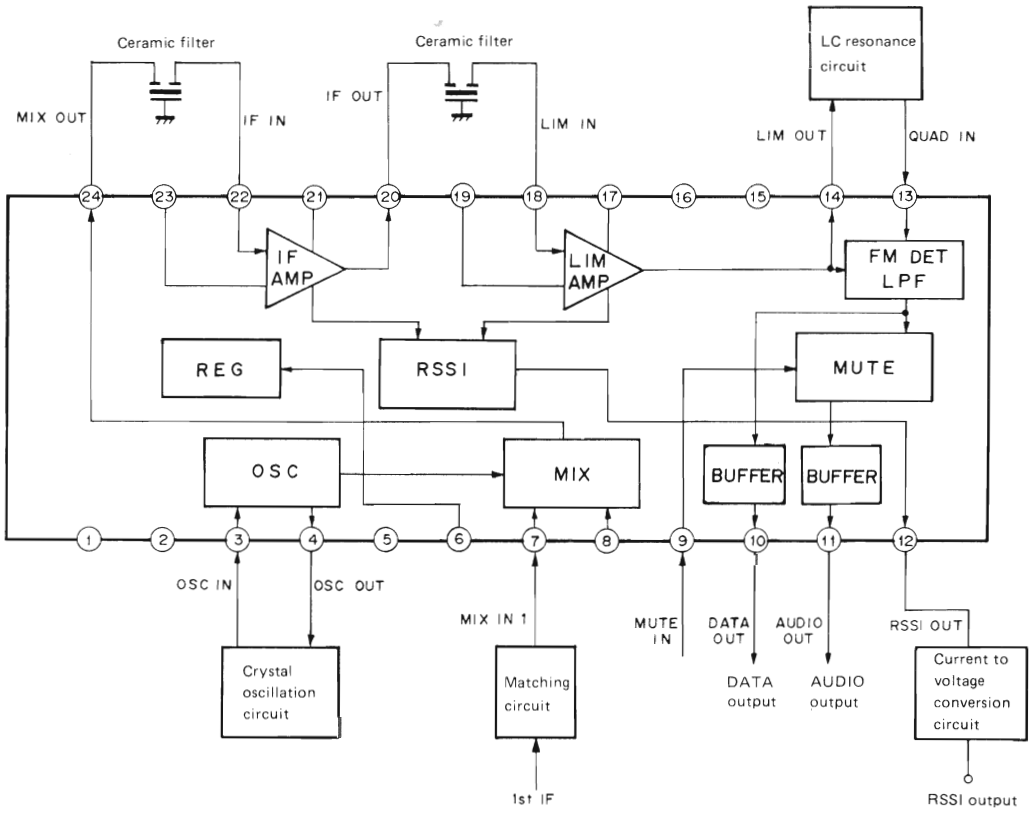


Electrical Characteristics Test Circuit



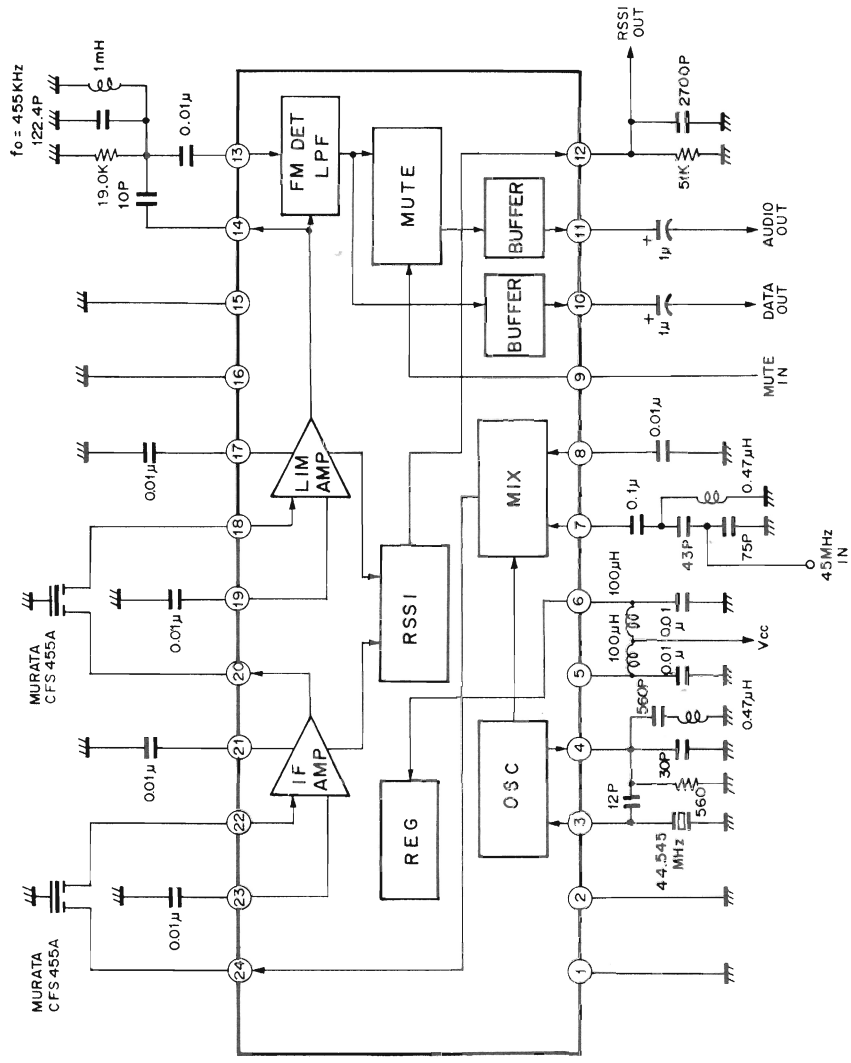
Description of Operation

The signals which have been input from pins ⑦ and ⑧ are mixed with the local oscillation signals from the oscillator in the mixer, and the frequency converted signal is output from pin ㉔ . The oscillator is self-oscillated by composing Colpitts type crystal oscillation circuit between pin ③ and ④ . In addition, it is possible to apply a local oscillation signal to pin ③ from the external circuit. After the bandwidth is limited by BPF, the mixer output is amplified by IF amplifier and output from pin ⑳ . The IF amplifier output is limited its bandwidth again, and amplitude limited by the limiter and output from pin ⑭ . The limiter amplifier output is phase-shifted by LC resonance circuit, etc., and audio signal is output from pin ⑩ and ⑪ after being quadrature detected. The output from pin ⑪ can be muted by control signal from pin ⑨ . The control signal is muting at "H" in TTL level and through at "L".



The RSSI output is the currents corresponding to the input levels at the IF amplifier and the limiter. It is possible to convert a current into a voltage by connecting a proper I. V conversion circuit.

Application Circuit



Notes on Use

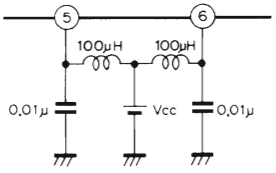
The CXA1003AM has very high at voltage gain, so take care of the following.

1. Decouple pin ⑤ (V_{CC2}) and ⑥ (V_{CC1}) with L and C as near to the pins as possible.
2. Connect pin ⑮ and ⑯ (NC) to GND.
3. Separate input line from the output line as far as possible, and make the wiring short.
4. Connect pin ⑧, ㉑, ㉓, ⑰ and ⑲ to GND with capacitor as near to pins as possible.
5. The GND impedance should be as low as possible.
6. It is better to separate statically the input from the output of the limiter with shielding plate.

Notes on Application

1) Power supply

The CXA1003AM has a voltage regulater within the IC, so it has wide operating power supply range (+4.5 to +9.5V; Typ: 5.0V). There is little change in characteristics in the operating range. Decouple pin ⑤ (V_{CC2}) and ⑥ (V_{CC1}) with L and C. (See Fig. right)



Power supply decoupling

2) Oscillator

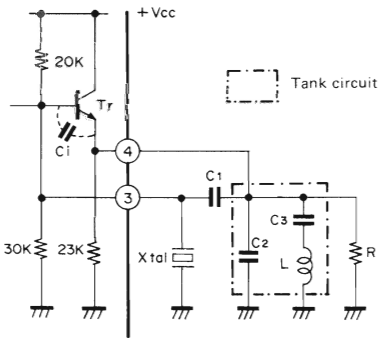
The method to use oscillator of CXA1003AM is the following:

(a) Method to input from pin ③ with the self-excitating oscillation signal by composing a crystal oscillation circuit of the Colpitts type to pin ③ and ④.

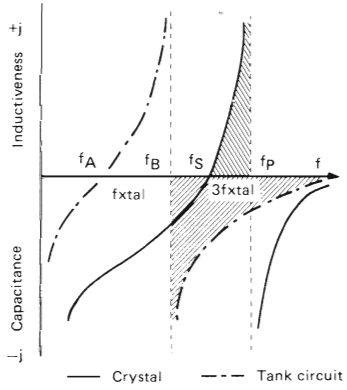
(b) Method to input directly the external local oscillation signal to pin ③.

<Crystal oscillation circuit>

The 3rd overtone crystal oscillation circuit of the Colpitts type is Fig. bellow.



Colpitts type crystal oscillation circuit



Reactance characteristics

The conditions of the 3rd overtone oscillation of this oscillation circuit are the following.

- The parallel resonance frequency (f_B) of the tank circuit should be smaller than the 3rd oscillation frequency ($3f_{xtal}$) and the serial resonance frequency (f_A) should be smaller than the basic oscillation frequency (f_{xtal}) ($3f_{xtal} > f_B$, $f_{xtal} > f_A$).
- The load capacitance (:C_L) of the crystal should be adequate.
- The f_t of the amplifier (Tr) should be sufficiently larger than $3f_{xtal}$.

The constant is determined so as to satisfy these conditions.
The oscillation level is set at 125 to 400 mVrms (Typ: 224 mVrms) and adjust the level by changing the resistance value (R). The slight adjustments of the oscillation frequency and oscillation level are performed with C_2 and L.

<In case of direct input>
In case of direct input, connect pin ④ to V_{CC} and input external local oscillation signal to pin ③. Input level at this point is also 125 to 400 mVrms (Typ: 224 mVrms).

3) Mixer

Mixer of the CXA1003AM is a double balance type. Input ports are pin ⑦ and ⑧, and in case of single input, input signal to pin ⑦, and connect pin ⑧ to GND with capacitor. It is possible to use differential input. The standard input level is −110 to −30 dBm (0.7μ to 7.0 mVrms), and input through a suitable matching circuit.

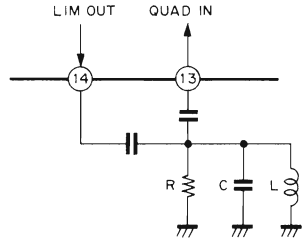
4) Filter

The band-pass filters which are connected between pin ㉔ and ㉒ and between pin ⑳ and ⑱ of the CXA1003AM are desired to have the specifications as follows.

- Input/output impedance: 1.5 k$\Omega\pm$10%
- Insertion loss (center frequency): <6 dB

5) Phase shifter

Input to pin ⑬ to shift the phase of the limiter output (pin ⑭) 90° by the RLC parallel resonance circuit or the discriminator, etc. in order to quadrature FM detection. The Fig. below shows the RLC phase shifter. In this case, determine the L and C values so that the 2nd IF signal frequency and the parallel resonance frequency are the same, and the audio output level is determined by R value. RLC Phase shifter or Oscillator is connected between pin ⑬ and ⑭, the phase shifted signal is input to pin ⑬ and demodulated in quadrature detector.



RLC phase shifter

6) Audio output, data output and muting

The FM modulated audio or data signal is demodulated in the prior stage and is output from pin ⑪ (AUDIO OUT) and ⑩ (DATA OUT). Output from pin ⑪ can be muted by control signal of TTL level from pin ⑨ (MUTE IN). (See table below.)

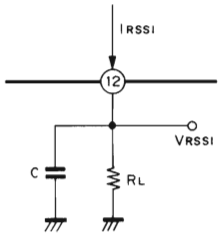
Control signal	Audio signal
H (>2.0V)	Mute
L (<0.8V)	Slew

Table of muting control

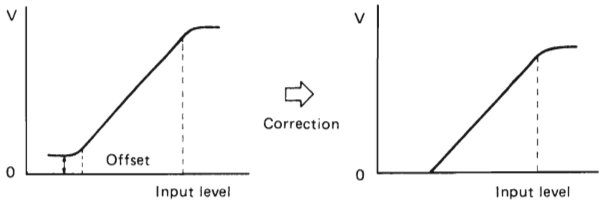
7) RSSI

The function of RSSI is to detect the input level, and output current increases monotonously within the range of IF input level −100 to 0 dBm (2.24μ to 224 mVrms). The power supply and temperature effect little on output current. However, the output current is distributed within the range of ±20% due to the resistance within the IC. In case voltage output is required, it needs current to voltage conversion circuit composing with resistance, etc. The resistance value is determined by the RSSI maximum output current and the allowable maximum voltage of pin ⑫ . The RSSI maximum output current is approximately 60 μA (Typ: 45 μA) and the allowable maximum voltage (recommended maximum voltage) is V_{CC}−1.8V, select the resistance according to the power supply and the required output voltage. In case the output voltage is required above V_{CC}−1.8V, amplify a voltage using an operational amplifier, etc.

The AMPS defines that the RSSI output voltage increases monotonously from 0 to 0.5V. The CXA1003AM has an offset of approximately 0.3 to 0.5V (V_{CC}=5V R_L=51 kΩ), if it needs, utilize the offset correction circuit.

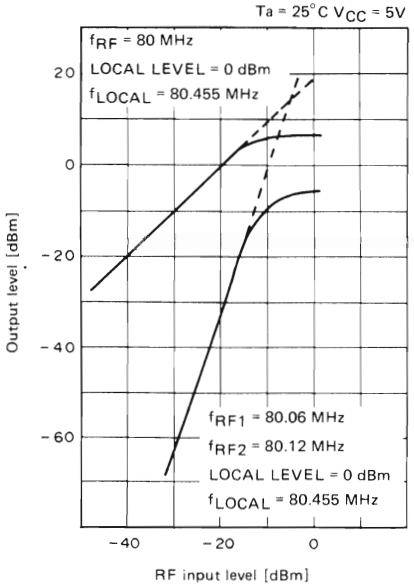


Current to voltage conversion with resistance of RSSI output

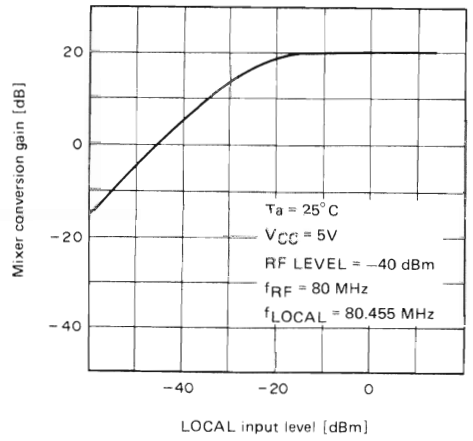


Offset correction of RSSI output voltage

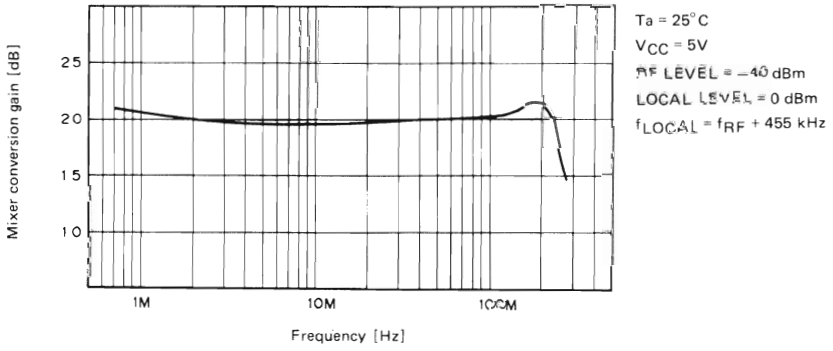
Mixer I/O characteristics and the 3rd order intercepting point



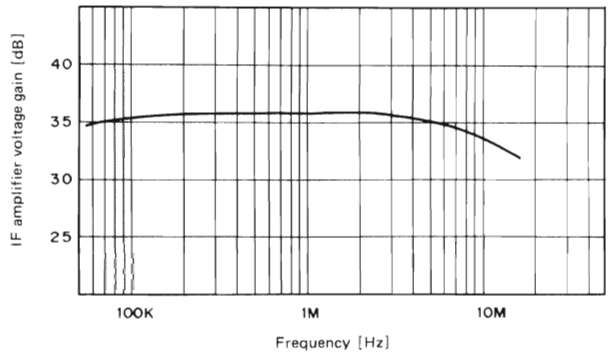
Mixer conversion gain vs. Local input level



Mixer conversion gain frequency characteristics

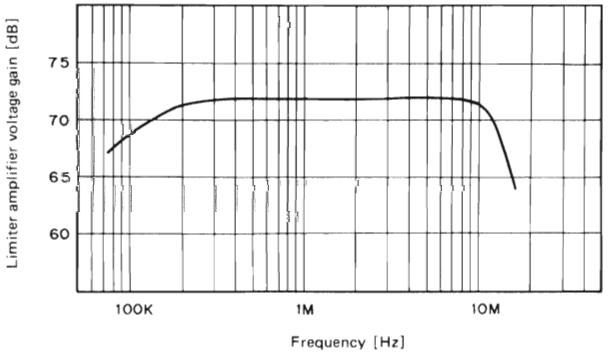


IF amplifier voltage gain frequency characteristics



Ta = 25°C
V_{CC} = 5V
RF LEVEL = −50 dBm

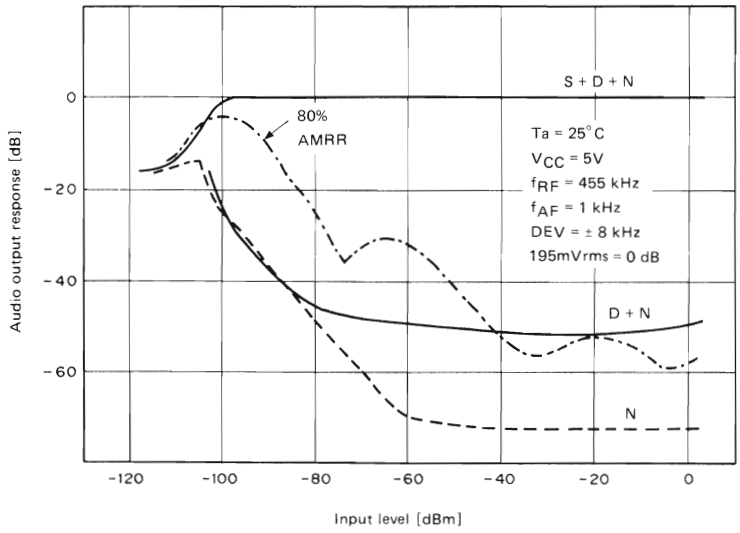
Limiter voltage gain frequency characteristics



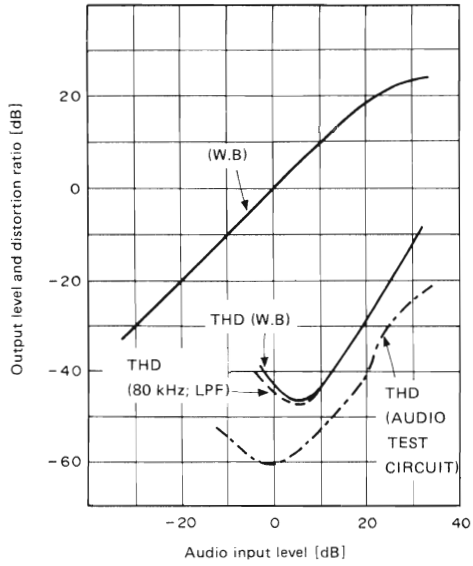
Ta = 25°C
V_{CC} = 5%
RF LEVEL = −90 dBm

Audio demodulation characteristics (IF IN/AUDIO OUT)

* Uses AUDIO Test Circuit

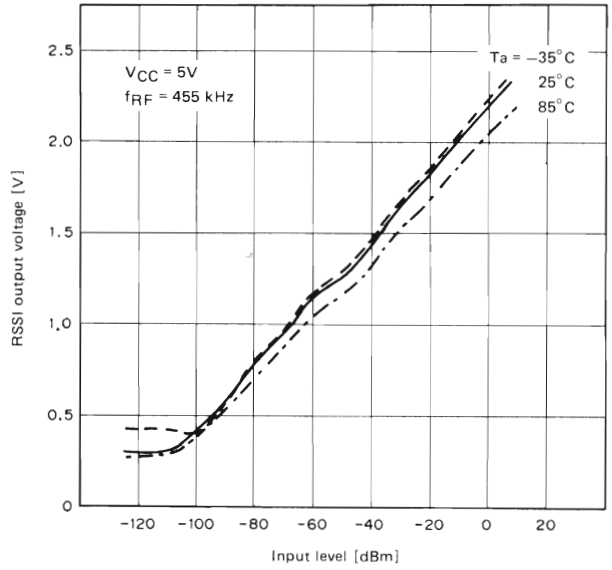


Audio I/O characteristics

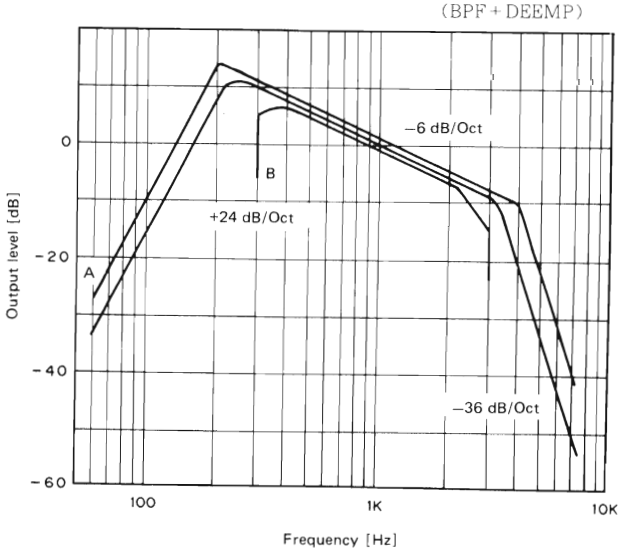


Ta = 25°C
V_{CC} = 5V
RF LEVEL = −20 dBm
f_{RF} = 455 kHz
f_{AF} = 1 kHz
AUDIO INPUT LEVEL
DEV; ± 2.9 kHz = 0 dB

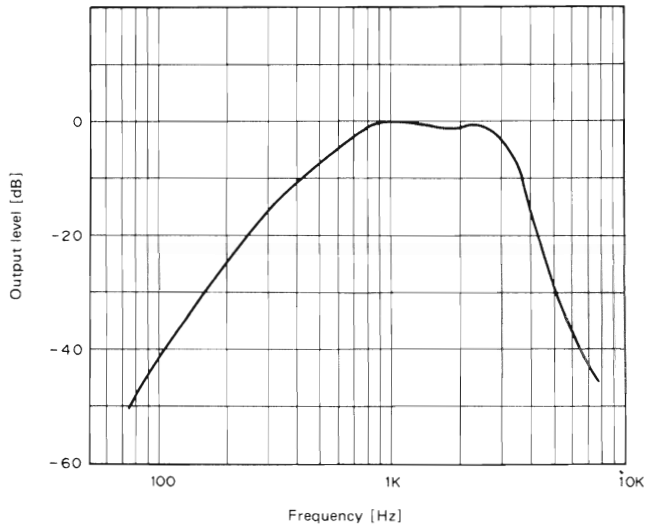
RSSI characteristics (IF IN/RSSI OUT)



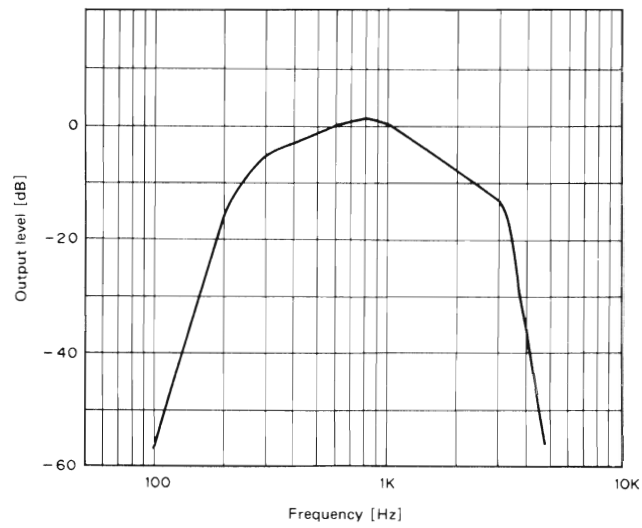
RX-audio filter frequency characteristics (A-B; AMPS Typ.)



C-message filter frequency characteristics



Audio measurement circuit frequency characteristics



SONY CXD1082M

Filter IC for Cellular Mobile Telephone

Description

The CXD1082M is a filter IC developed for cellular mobile telephone. By using this IC in conjunction with the DATA·SAT LSI CXD1083Q, a modem can be set up.

Features

- Miniaturized filter by use of switched capacitor technology
- 5V single power supply operation
- Low power consumption (28 mW, typ. in 5V operation)

Functions

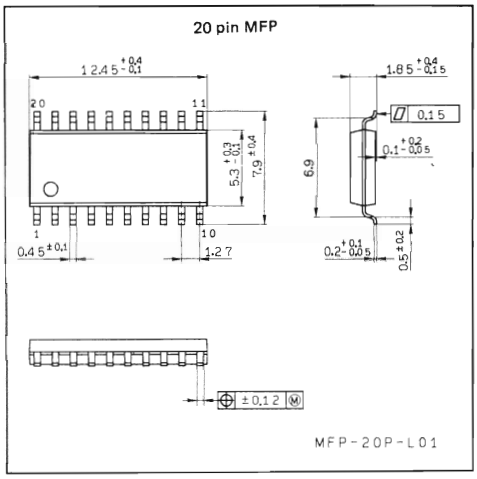
- Filtering of received wide band data
- Filtering of received SAT
- Detection of PLL lock of received SAT
- Summing of wide band data, ST, and SAT to be transmitted
- Filtering of wide band data, ST, and SAT to be transmitted

Structure

Silicon gate CMOS IC

Package Outline

Unit: mm



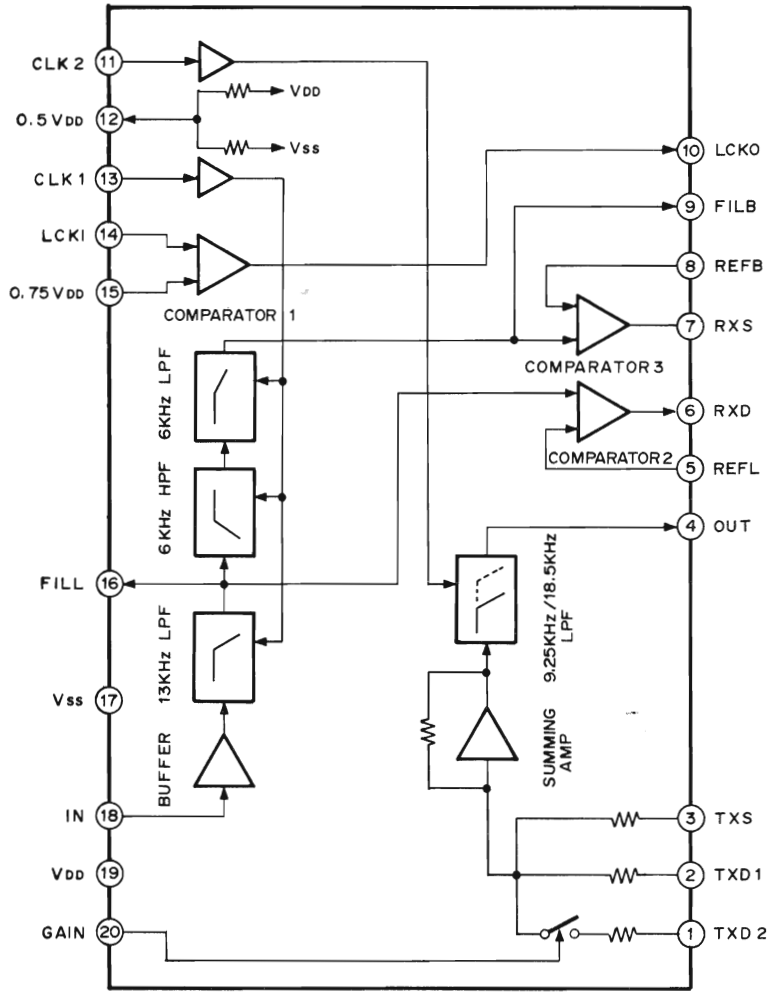
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	−0.3 to 7.0	V
• Input voltage	V_{IN}	−0.3 to V_{DD} +0.3	V
• Output voltage	V_{OUT}	−0.3 to V_{DD} +0.3	V
• Operating temperature	Topr	−34 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

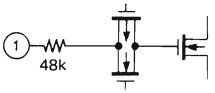
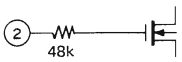
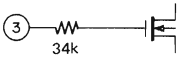
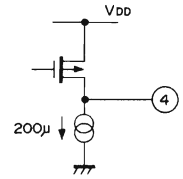
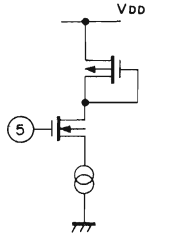
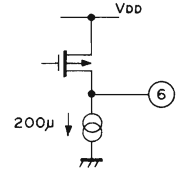
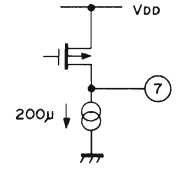
Recommended Operating Conditions

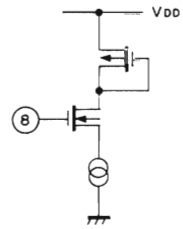
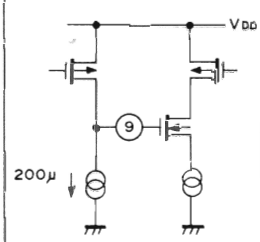
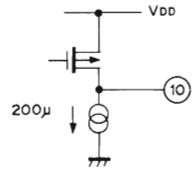
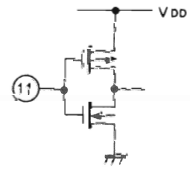
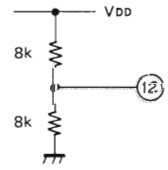
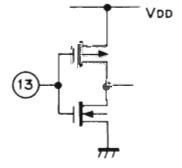
• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	Topr	−34 to +75	°C

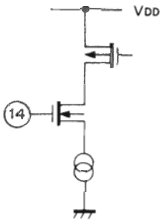
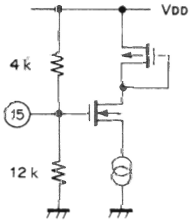
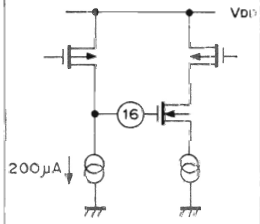
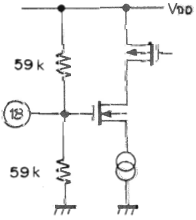
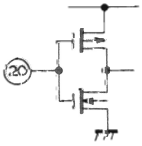
Block Diagram



Pin Description

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
1	TXD2		I		Input pin 1 for transmission of wide band data and ST from a mobile station to a land station.
2	TXD1		I		Input pin 2 for transmission of wide band data and ST from a mobile station to a land station.
3	TXS		I		Input pin for transmission of SAT from a mobile station to a land station.
4	OUT		O		Output pin for 9.25kHz/18.5kHz low-pass filter with variable cutoff frequency.
5	REFL		I		Reference voltage input pin of a comparator for wide band data received by a mobile station from a land station. By an external 1μF capacitance, output offset of 13kHz low-pass filter for received wide band data is eliminated.
6	RXD		O		Output pin of a comparator for wide band data received by a mobile station from a land station. When 13kHz low-pass filter output voltage exceeds reference voltage (pin 5), output level of this pin goes from "low" to "high."
7	RXS		O		Output pin of a comparator for SAT received by a mobile station from a land station. When 6kHz low-pass filter output voltage exceeds reference voltage (pin 8), output level of this pin goes from "low" to "high."

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
8	REFB		I		Reference voltage input pin of a comparator for SAT received by a mobile station from a land station. By an external 1μF capacitance, output offset of 6kHz low-pass filter for received SAT is eliminated.
9	FILB		O		6kHz low-pass filter output pin for SAT received by a mobile station from a land station. This pin is connected to the comparator used for receiving SAT.
10	LCKO		O		Output pin for the comparator used to detect PLL lock for the received SAT. When input voltage (pin 14) exceeds reference voltage (pin 15), output level of this pin goes from "low" to "high".
11	CLK2		I		Clock input pin for 9.25kHz/18.5kHz low-pass filter with variable cutoff frequency. 400kHz clock input provides 18.5kHz cutoff frequency, and 200kHz input provides 9.25kHz cutoff frequency.
12	0.5VDD		O		Internal operational amplifiers virtual ground level output pin. Output voltage of this pin will be half of the supplied voltage. An external capacitance of 3.3μF is required as a ripple filter.
13	CLK1	2.5V	I		Clock input pin for receiving 13kHz low-pass filter, 6kHz high-pass filter, and 6kHz low-pass filter. Input clock frequency is 400kHz.

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
14	LCKI		I		Input pin for the comparator used to detect PPL lock of the received SAT.
15	0.75VDD	3.75V	I		Reference voltage input pin for the comparator used to detect PLL lock of the received SAT. This pin is biased at 3/4 of the supplied voltage. An external capacitance of 3.3μF is required as a ripple filter.
16	FILL		O		Output pin for the 13kHz low-pass filter for wide band data received by a mobile station from a land station. This pin is connected to the comparator used for receiving wide band data.
17	VSS				Ground pin
18	IN	2.5V	I		Input pin for wide band data and SAT received by a mobile station from a land station. This pin is connected to the voltage follower whose input is biased at a half of the supplied voltage.
19	VDD				Supply voltage pin
20	GAIN		I		Gain switching input pin for wide band data and ST to be transmitted. Input level must be "low" for ST transmission, and "high" for data transmission.

Note 1) The pin voltages specified in this table are those for $V_{DD} = 5V$.

2) The resistances and currents are typical values.

Electrical Characteristics

(Ta = 25°C, V_{DD} = 5V. See Fig. 1 to 4.)

	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
	Current consumption	I_{DD}			5.6	6.5	mA
	Clock 1 frequency	F_{CK1}			400		kHz
	Clock 1 input voltage	V_{CK1}		3.5			Vp-p
	Clock 1 input threshold level			2.0	2.5	3.0	V
	Clock 2 frequency	F_{CK2}		200		400	kHz
	Clock 2 input voltage	V_{CK2}		3.5			Vp-p
	Clock 2 input threshold level			2.0	2.5	3.0	V
	Gain control input voltage	V_G		0		5.0	V
	Gain control input threshold level			2.0	2.5	3.0	V
Input voltage	Received signal input	IN		0.2		1.0	Vp-p
	Transmission signal input 1	T_{XD1}		0.2		0.7	Vp-p
	Transmission signal input 2	T_{XD2}		0.2		0.7	Vp-p
	Transmission signal input 3	T_{XS}		0.2		1.0	Vp-p
Input impedance	Received signal input	Z_{IN}		24	29		kΩ
	Transmission signal input 1	Z_{TXD1}		40	48		kΩ
	Transmission signal input 2	Z_{TXD2}		40	48		kΩ
	Transmission signal input 3	Z_{TXS}		30	34		kΩ
Output voltage	13kHz low-pass filter	F_{ILL}		0.2		1.0	Vp-p
	7kHz band-pass filter	F_{ILB}		0.2		1.0	Vp-p
	9kHz/18kHz low-pass filter	OUT	TXS = 0V, VG = 0V, TXD1 = TXD2	0.56		2.0	Vp-p
	Comparator reference voltage	REF		3.55	3.75	3.90	V
	Analog reference voltage	AREF		2.35	2.50	2.65	V
Duty	Comparator 1	LCKO		42	50	58	%
	Comparator 2	RXD	Received signal input: 1kHz, 1Vp-p	47.5	50	52.5	%
	Comparator 3	RX6	Received signal input: 7kHz, 1Vp-p	47.5	50	52.5	%
Gain	Transmission signal input 1 gain	G_{TXD1}		−3.4	−2.9	−2.4	dB
	Transmission signal input 2 gain	G_{TXD2}	V_G = 0V	−3.4	−2.9	−2.4	dB
	Transmission signal input 3 gain	G_{TXS}		−0.5	0	+0.5	dB
Stop band attenuation	13kHz low-pass filter		Received signal input: 13kHz, 1Vp-p	−3.64	−2.61	−1.58	dB
	6kHz band-pass filter		Received signal input: 3kHz, 1Vp-p	−23.71	−21.49	−19.27	dB
			Received signal input: 7kHz, 1Vp-p	−0.07	−0.02	+0.03	dB
			Received signal input: 12kHz, 1Vp-p	−10.46	−8.84	−7.22	dB
	18.5kHz low-pass filter		Received signal input 3: 18.5kHz, 0.5Vp-p	−2.90	−2.44	−1.98	dB
			Received signal input 3: 60kHz, 0.5Vp-p	−40.16	−39.66	−39.16	dB
	9.25kHz low-pass filter		Received signal input 3: 9.25kHz, 0.5Vp-p	−2.99	−2.55	−2.11	dB

Electrical Characteristics Test Circuit 1 (Frequency Characteristics, Output Voltage)

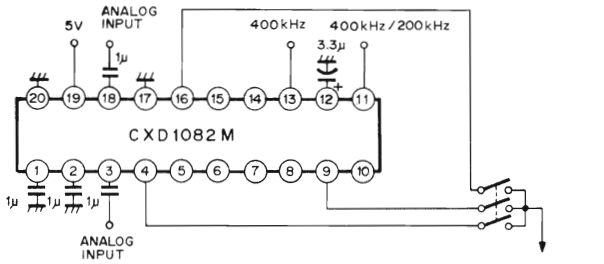


Fig. 1

Electrical Characteristics Test Circuit 2 (Comparator Output Duty)

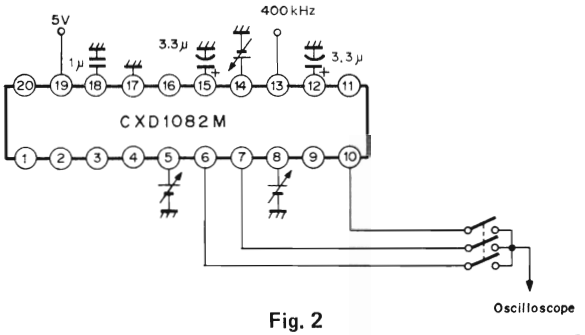


Fig. 2

Electrical Characteristics Test Circuit 3 (Summing Amplifier Gain)

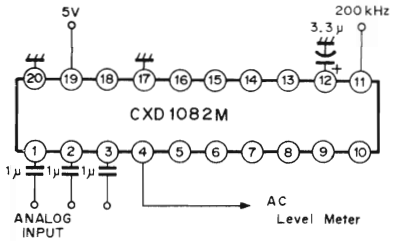


Fig. 3

Electrical Characteristics Test Circuit 4 (Current Consumption)

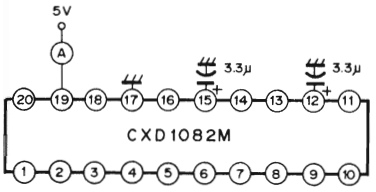


Fig. 4

Description of Operations

The CXD1082M is a filter IC developed for cellular mobile telephone. By using this IC in conjunction with the DATA·SAT LSI CXD1083Q, a modem having the following functions can be set up:

(1) Filtering of received wide band data
(2) Filtering of received SAT
(3) Detection of PLL lock of received SAT
(4) Summing of wide band data, ST, and SAT to be transmitted
(5) Filtering of wide band data, ST, and SAT to be transmitted

This section provides brief descriptions of these functions.

1. Filtering of received wide band data

In the cellular mobile telephone system, data is transmitted between the land and mobile stations for purposes of channel setting, etc., during speech or hand-off (Transition between cells). This data is called wide band data, which is Manchester coded, and is transmitted at a rate of 20K baud. The received wide band data is fed through a buffer amplifier via a voltage follower to the 13kHz quartic Butterworth low-pass filter which operates as a data demodulating roll-off filter. This filter is of switched capacitor type, providing a cutoff frequency of 13kHz (typ.) when the sampling clock frequency is 400kHz. The filter output is shaped to the CMOS logic level with a comparator, and is then sent out to the CXD1083Q.

2. Filtering of received SAT

In the cellular mobile telephone system, even during speech, a sine wave signal called SAT (Supervisory Audio Tone) is transmitted between the land station and the mobile station in order that they recognize each other. SATs of three frequencies, 5.97kHz, 6.00kHz, and 6.03kHz, are available. The SAT frequency to be used is determined at the hand-off time by 2-bit data called SCC (SAT Color Code) which is transmitted from the land station to the mobil station. During speech, the mobile station recognizes the land station by receiving the SAT from the land station, and the land station recognizes the mobile station by receiving the SAT from the mobile station.

Similarly to the wide band data, the SAT received from the land station is fed through the buffer amplifier to the 13kHz quartic Butterworth low-pass filter. Then the SAT is fed to the 6kHz quartic Butterworth high-pass filter to prevent interference from the voice component (300Hz to 3kHz), and then to the 6kHz quadratic Tchebycheff low-pass filter (pass range ripple 1dB) to reduce the high-band noise (6kHz to 13kHz) in the event of a weak electric field strength. These 6kHz high-pass and low-pass filters are of switched capacitor type, providing a cutoff frequency of 6kHz (typ.) when the sampling clock frequency is 400kHz. The above three filters constitute a band-pass filter with a center frequency of approx. 7kHz so that the SAT can be efficiently detected. The output of the 6kHz low-pass filter is shaped to the CMOS logic level with a comparator, and is then sent out to the CXD1083Q.

3. Detection of PLL lock of received SAT

In the CXD1083Q, DPLL locks when the SAT having the frequency specified with SCC is received. The CXD1082M has a comparator to detect this lock/unlock state. The comparator output changes from the "low" level to the "high" level when the level of the SAT lock detect signal (SDET) from the CXD1083Q exceeds the reference voltage ($0.75V_{DD}$).

4. Summing of wide band data, ST, and SAT to be transmitted

In the cellular mobile telephone system, wide band data or ST, and SAT are transmitted from the mobile station to the land station. The ST is a 10kHz signal that is transmitted at the end of the call or for ringing. From the CXD1083Q to the CXD1082M, the wide band data and ST are fed through a –6dB attenuation pad, and the SAT is fed through a –18dB attenuation pad.

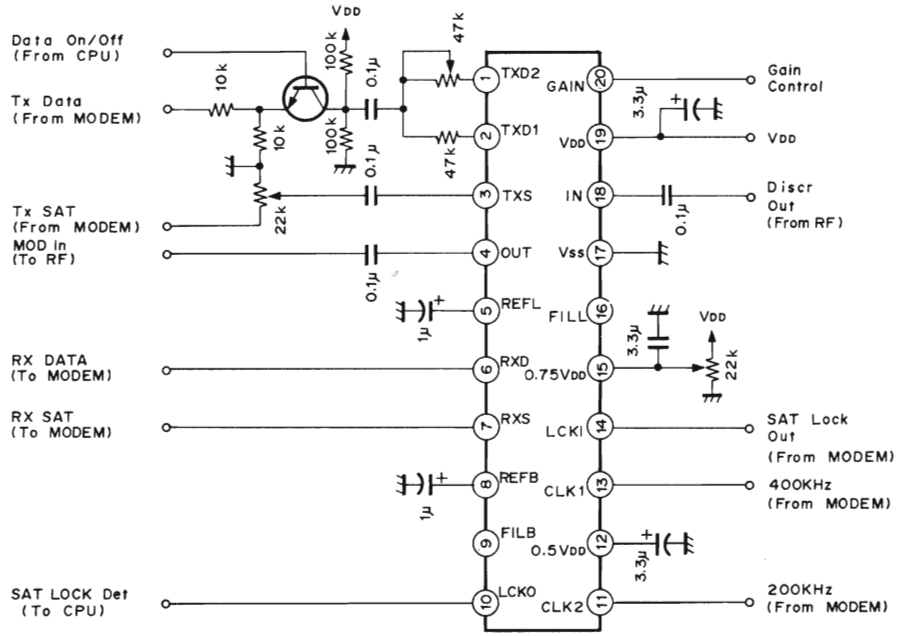
The CXD1082M has an inverting amplifier which operates as a summing amplifier to sum these signals before transmission. As the transmitting amplifier in the next stage of the summing amplifier, the 18.5kHz quartic Butterworth low-pass filter is selected for wide band data transmission, and the 9.25kHz quartic Butterworth low-pass filter for ST transmission.

In order to compensate for the amplitude characteristics difference (–2.98dB to –4.62dB) between the 18.5kHz and 9.25kHz low-pass filters at the ST frequency (10kHz), +3dB or –2.9dB can be selected as the summing amplifier gain. When the ST is transmitted, the +3dB gain can be obtained by setting the gain control input (GAIN) to the "low" level, and the –2.9dB gain can be obtained by setting GAIN to the "high" level. The CXD1082M is provided with two input pins (TXD1 and TXD2) for the wide band data and ST so that the gain can be further adjusted by inserting appropriate resistors into the respective input lines. This allows the output level difference between ST transmission and data transmission to be completely compensated.

5. Filtering of wide band data, ST, and SAT to be transmitted

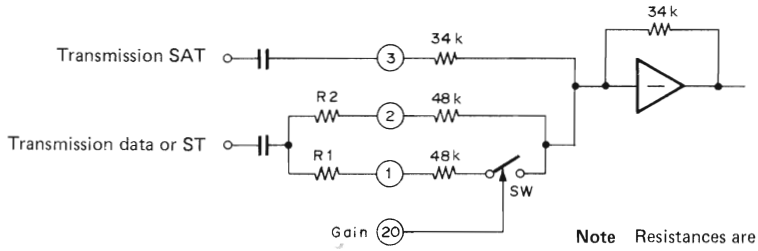
In the next stage of the summing amplifier, a low-pass filter is provided for removing the high-order harmonics from the summing amplifier output. The AMPS (Advanced Mobile Phone Service) Standards of AT&T (American Telephone and Telegraph) require a "20kHz ±10% quartic Butterworth low-pass filter" as the transmission wide band data roll-off filter. In the CXD1082M, the filter used in the next stage of the summing amplifier is an 18.5kHz quartic Butterworth low-pass filter, and this filter also satisfies the condition of 38dB or more attenuation at 60kHz specified by the AMPS. When ST and SAT are transmitted, the cutoff frequency of this transmitting filter must be lowered because frequencies of ST and SAT are 10kHz and 6kHz, respectively. The transmitting filter of the CXD1082M is a switched capacitor filter providing a cutoff frequency of 18.5kHz (typ.) when the sampling frequency is 400kHz, and 9.25kHz (typ.) when the sampling frequency is 200kHz.

Application Circuit



Notes on Application

1. Summing amplifier gain adjustment



Note Resistances are typical values.

The summing amplifier is an inverting amplifier having a configuration shown in the above figure.

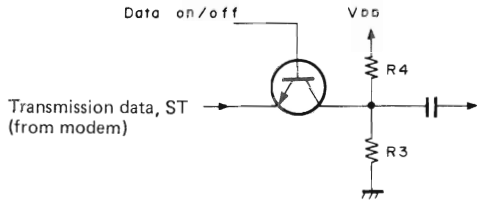
Therefore, for the transmission SAT, a gain of 0dB (typ.) is obtained, and for the transmission data and ST, +3.0dB (typ.) or −2.9dB (typ.) is obtained when the SW is on or off, respectively, provided R1=R2=0Ω, that is, if pins ① and ② are short-circuited. The reason for provision of gain switching for the transmission data and ST is that the difference between the filter cutoff frequency for data transmission (18.5kHz) and that for ST transmission (9.25kHz) causes transmission output level difference of −3.0 to −4.6dB between the data and ST. In order to compensate this transmission level difference, the gain control input is set to "L" for ST transmission, which turns on the SW and consequently sets the summing amplifier gain to +3.0dB, and the gain control input is set to "H" for data transmission, which turns off the SW and consequently sets the summing amplifier gain to −2.9dB. However, this level compensation is not complete. The summing amplifier gain can be further adjusted by inserting R1 and R2. For this adjustment, proceed as follows:

① Set the CLK2 frequency to 400kHz, and the gain control input level to "H". Apply a 10kHz, 0.7Vp-p sine wave to pins ① and ② via R1 and R2, and measure the transmitting filter output level at pin ④ . The measurement result corresponds to the output level for data transmission.

② Set the CLK2 frequency to 200kHz, and the gain control input level to "L". Apply a 10kHz, 0.7Vp-p sine wave to pins ① and ② via R1 and R2, and measure the transmitting filter output level at pin ④ . The measurement result corresponds to the output level for ST transmission.

③ Adjust R1 or R2 so that the same result can be obtained in the above measurements.

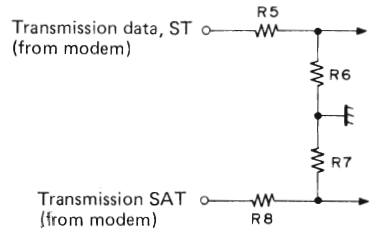
2. Three-state processing for transmission data and ST input pin



The transmission data and ST output level of the modem (ex. CXD1083Q) is "L" when neither data nor ST is being transmitted. Therefore the modem cannot be connected to the CXD1082M by capacitor coupling unless any countermeasure is taken.

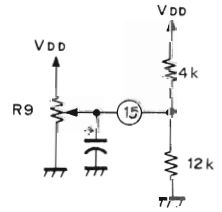
In order to connect the modem to the CXD1082M by capacitor coupling, attach an external transistor which is kept on during transmission, and is kept off when neither data nor ST is being transmitted. R3 and R4 provide a voltage level of $V_{DD}/2$.

3. Attenuation pads for transmission data and ST, and transmission SAT



The transmission data and ST output and the transmission SAT output from the modem (ex. CXD-1083Q) must be fed to the CXD1082M after being attenuated by R5 and R6, and R7 and R8, respectively. Set the attenuation ratio by R5 and R6 to –6dB, and that by R7 and R8 to –18dB.

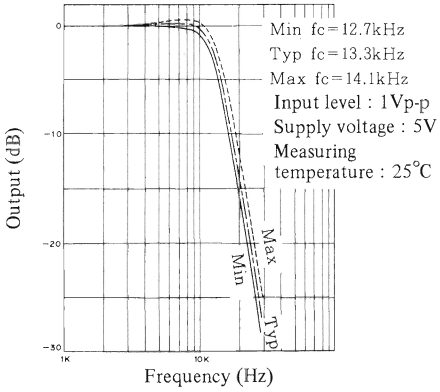
4. Adjustment of $0.75V_{DD}$



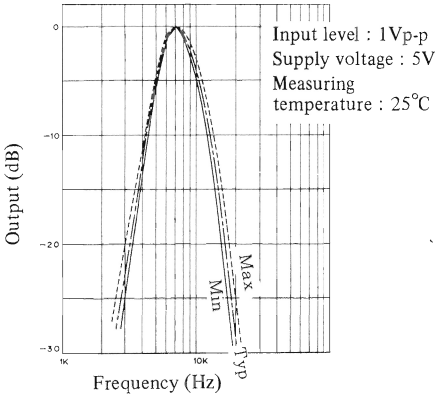
Note) Resistances are typical values.

The voltage obtained inside the CXD1082M by dividing the supply voltage to $0.75V_{DD}$ is output. This voltage can be externally adjusted as shown in the above figure.

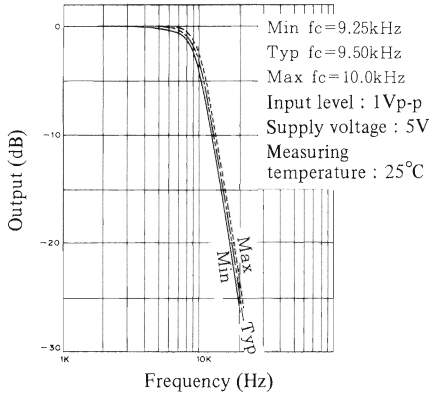
13kHz LPF Amplitude characteristics



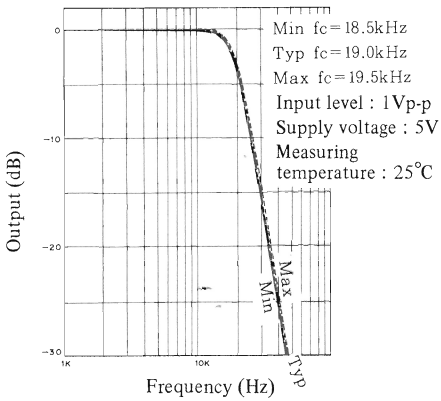
BPF Amplitude characteristics



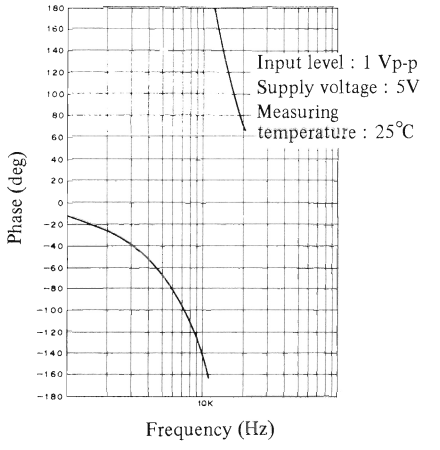
9.25kHz LPF Amplitude characteristics



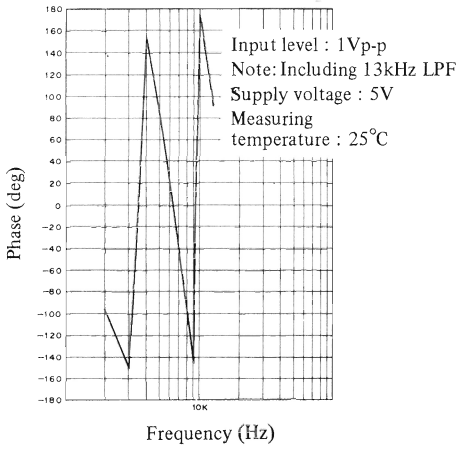
18.5kHz LPF Amplitude characteristics



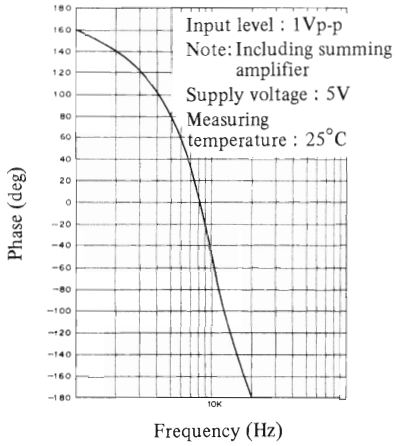
13kHz LPF Phase characteristics



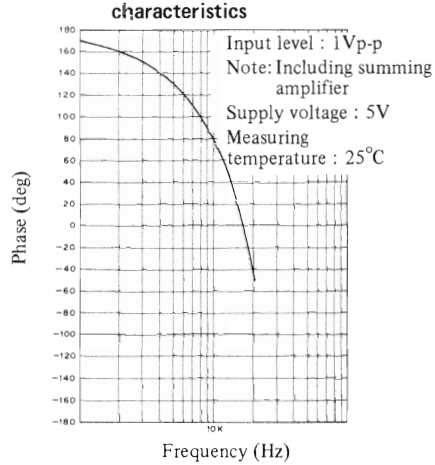
BPF Phase characteristics



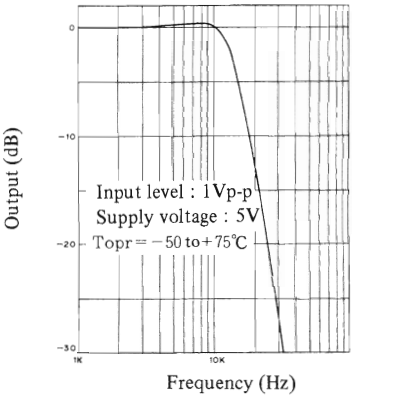
9.25kHz LPF Phase characteristics



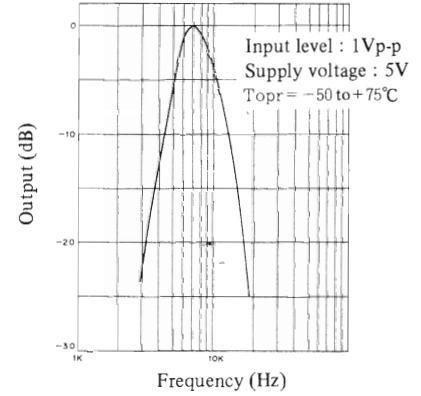
18.5kHz LPF Phase characteristics



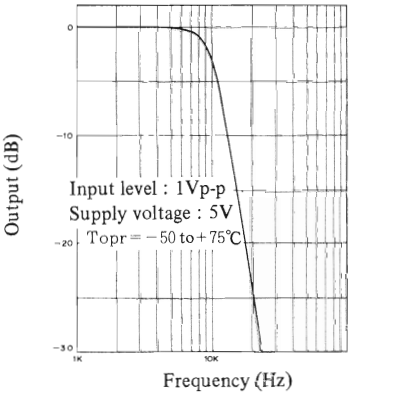
13kHz LPF Amplitude-temperature characteristics



BPF Amplitude-temperature characteristics



9.25kHz LPF Amplitude-temperature characteristics



SONY® CXD1083Q

Data and SAT LSI for Cellular Radio Telephone

Description

The CXD1083Q is a DATA and SAT LSI for the US cellular radio telephone system; it is used in combination with the switched capacitor filter CXD1082M.

Features

- Provided with a Manchester code decoder with a small bit error rate.
- SAT detector circuit with negligible malfunction even in a very small electrical field.
- Low power consumption.

Functions

- Decoding of received DATA
- Detection of received SAT (Supervisory Audio Tone)
- Transmitting SAT having the same frequency and phase as those of received SAT
- Encoding of transmitting DATA and ST

Structure

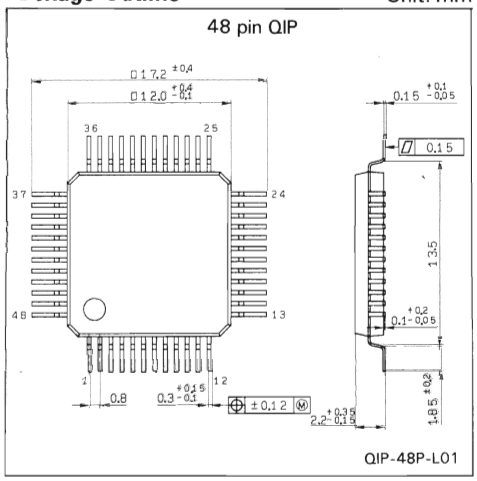
Silicon gate CMOS

Application

Cellular radio telephone

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	V_{SS}*1 −0.3*2 to 7.0	V
• Input voltage	V_I	V_{SS}*1 −0.3*2 to V_{DD} +0.3*2	V
• Output voltage	V_O	V_{SS}*1 −0.3*2 to V_{DD} +0.3*2	V
• Operating temperature	Topr	−34 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

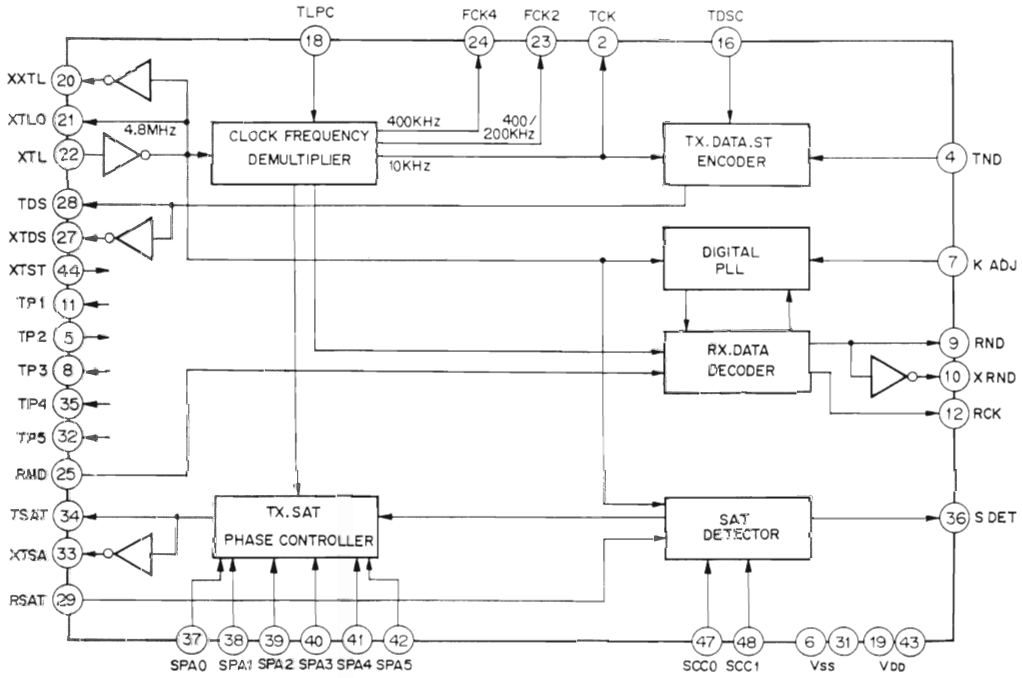
Note) *1 V_{SS} = 0V

*2 This value is a steady state voltage.
In transient state (20 to 30 ns), 0.5V is allowable.

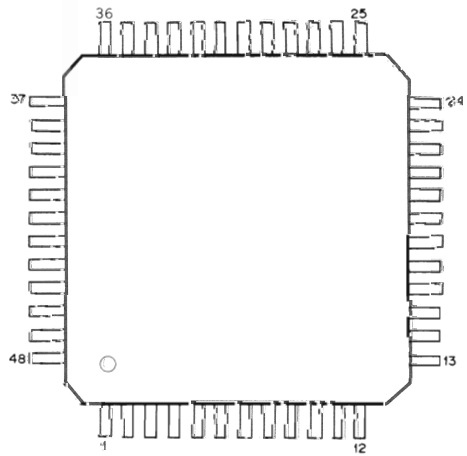
Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75 to 5.25 (5.00 Typ.)	V
• Operating temperature	Topr	−34 to +75	°C

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	N.C.	—	
2	TCK	O	Clock output (10kHz) for transmitting DATA, ST.
3	N.C.	—	
4	TND	I	Input of transmitting NRZ·DATA.
5	TP2	I	Input for test. Usually, fix "L".
6	Vss	—	GND
7	K ADJ	I	PLL lock range switching input for received Manchester DATA decoder (H: ±78Hz/L: ±19.5Hz).
8	TP3	O	Output for test.
9	RND	O	Output for received NRZ·DATA.
10	XRND	O	Inversion output of RND (Pin 9).
11	TP1	O	Output for test.
12	RCK	O	Clock output (10kHz), extracted from received DATA.
13	N.C.	—	
14	N.C.	—	
15	N.C.	—	
16	TDSC	I	ON/$\overline{\text{OFF}}$ control input for transmitting Manchester DATA.
17	N.C.	—	
18	TLPC	I	Frequency switching input of FCK2 (Pin 23) (H: 400kHz/L: 200kHz).
19	V_{DD}	—	+5V
20	XXTL	O	Inversion output of XTLO (Pin 21). 4.8MHz
21	XTLO	O	Crystal oscillator output. 4.8MHz
22	XTL	I	Crystal oscillator input, or external clock input. 4.8MHz
23	FCK2	O	Clock output for switched capacitor filter. 400kHz/200kHz
24	FCK4	O	Clock output for switched capacitor filter. 400kHz
25	RMD	I	Received Manchester DATA input
26	N.C.	—	
27	XTDS	O	Inversion output of TDS (Pin 28).
28	TDS	O	Output of transmitting Manchester DATA, ST.
29	RSAT	I	Received SAT input.

No.	Symbol	I/O	Description
30	N.C.	—	
31	Vss	—	GND
32	TP5	O	Output for test
33	XTSA	O	Inversion output of TSAT (Pin 34).
34	TSAT	O	Transmitting SAT output.
35	TP4	O	Output for test.
36	SDET	O	SAT detection output.
37	SPA0	I	Transmitting SAT phase correction input 0. (LSB)
38	SPA1	I	Transmitting SAT phase correction input 1.
39	SPA2	I	Transmitting SAT phase correction input 2.
40	SPA3	I	Transmitting SAT phase correction input 3.
41	SPA4	I	Transmitting SAT phase correction input 4.
42	SPA5	I	Transmitting SAT phase correction input 5. (MSB)
43	V_{DD}	—	+5V
44	XTST	I	Input for test. Usually, fix "H".
45	N.C.	—	
46	N.C.	—	
47	SCC0	I	SAT color code lower-bit input.
48	SCC1	I	SAT color code upper-bit input.

Electrical Characteristics

DC characteristics

V_{DD} = 5V±5%, V_{SS} = 0V
Topr = −34 to +75°C

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current		I_{DD}	Output without load		5		mA
		I_{DDS}	In steady state $V_{IH}=V_{DD}$ $V_{IL}=V_{SS}$	0		0.1	mA
Output voltage	H level	V_{OH}	I_{OH} = −0.4mA	4.0		V_{DD}	V
	L level	V_{OL}	I_{OL} = 2mA	V_{SS}		0.4	V
Input voltage	H level	V_{IH}		2.4			V
	L level	V_{IL}				0.8	V
Input leak current		I_{LI}		−10		10	μA

I/O capacitor

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			8	pF
Output pin	C_{OUT}			8	pF

Test conditions V_{DD} = V_I = 0V, fM = 1MHz

Functions

The CXD1083Q is a DATA and SAT LSI designed for the US cellular radio telephone system. It is used combined with the switched capacitor filter CXD1082M for following functions.

(1) Decoding of the received DATA.
(2) Detection of the received SAT.
(3) SAT transmission in the same frequency and phase as for received.
(4) Encoding of the transmitting DATA and ST.

The following is description of each function.

Decoding of the received DATA

With the cellular radio telephone system, DATA for selecting a channel is exchanged between land and mobile stations during cell movement after circuit connection. This DATA is called WIDE BAND DATA coded in the 20 k-baud Manchester code. The following diagram shows the logical values "1" and "0" of the Manchester code.

Fig. 1 Manchester code

To decode DATA input in this Manchester code, clock components are extracted by DPLL and the second half values of each bit are picked up using the clock. The decoded DATA is output as NRZ data from the output RND (Pin 9) and XRND (Pin 10) and its bit-clock is output from the output RCK (Pin 12). Timing of RCK with RND or XRND is shown in Fig. 2.

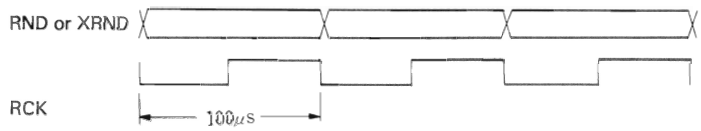


Fig. 2 Timing of RCK with RND or XRND

Detection of the received SAT

With the cellular radio telephone system, sinusoidal wave signals called SAT (Supervisory Audio Tone) are exchanged between land and mobile stations after radio link. SAT has three waves, 5.97 kHz, 6.00 kHz and 6.03 kHz; its frequency will be selected among them during cell movement, the one selected is notified in the SAT color code to the mobile station by the land station. During circuit connection, land and the mobile stations confirm each other through reception of the designated SAT frequency.

When the SAT signal with the frequency designated in the SAT color code is detected, SDET (Pin 36) becomes "H".

SAT transmission with the same frequency and phase as for received

The land station confirms a mobile station through receiving the SAT signal in the same frequency and phase as it has transmitted. The mobile station is required to transmit the SAT signal in the same frequency and phase as it has received. For this purpose, the mobile station transmits the signal by phase-correcting the DPLL output locked in the received SAT. Connecting the amount of phase depends on the transmitting circuit delay, etc.; this is correctly executed by varying 64 stages in 3.6° steps (0° to 226.8°) and then further shifting the phase by 180° by selecting the output TSAT pin (Pin 34) and XTSA (inversion output of TSAT, Pin 33), thereby resulting in the phase correction from 0° to 360° in 3.6° steps.

The following List 1 shows correction quantities of phase on the basis of TSAT output at the time of (SPA5, SPA4, SPA3, SPA2, SPA1, SPA0) = (0, 0, 0, 0, 0, 0).

SPA5	SPA4	SPA3	SPA2	SPA1	SPA0	Lag of phase	
						TSAT	XTSA
0	0	0	0	0	0	0°	180°
0	0	0	0	0	1	3.6°	183.6°
0	0	0	0	1	0	7.2°	187.2°
⋮						⋮	⋮
1	1	0	0	0	0	172.8°	352.8°
1	1	0	0	0	1	176.4°	356.4°

List 1: Lag of phase of the pins TSAT and XTSA on the basis of TSAT at the time of (SPA5, SPA4, SPA3, SPA2, SPA1, SPA0) = (0, 0, 0, 0, 0, 0)

Encoding of the transmitting DATA and ST

ST is a 10 kHz signal transmitted when conversation ends or when to ring the bell. It is output from TDS (Pin 28) and XTDS (Pin 27) with the DATA and ST (NRZ) input to TND (Pin 4), in synchronization with the clock output from TCK (Pin 2), and encoded in the Manchester code. However, it does not transmit the encoded data when the control input TDSC (Pin 16) is at "L" but fixes TDS to "H" and XTDS to "L".

Timing of TCK and TND is shown in Fig. 3.

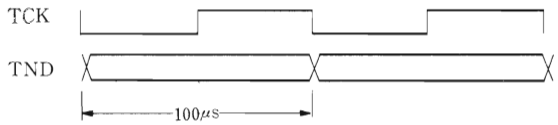


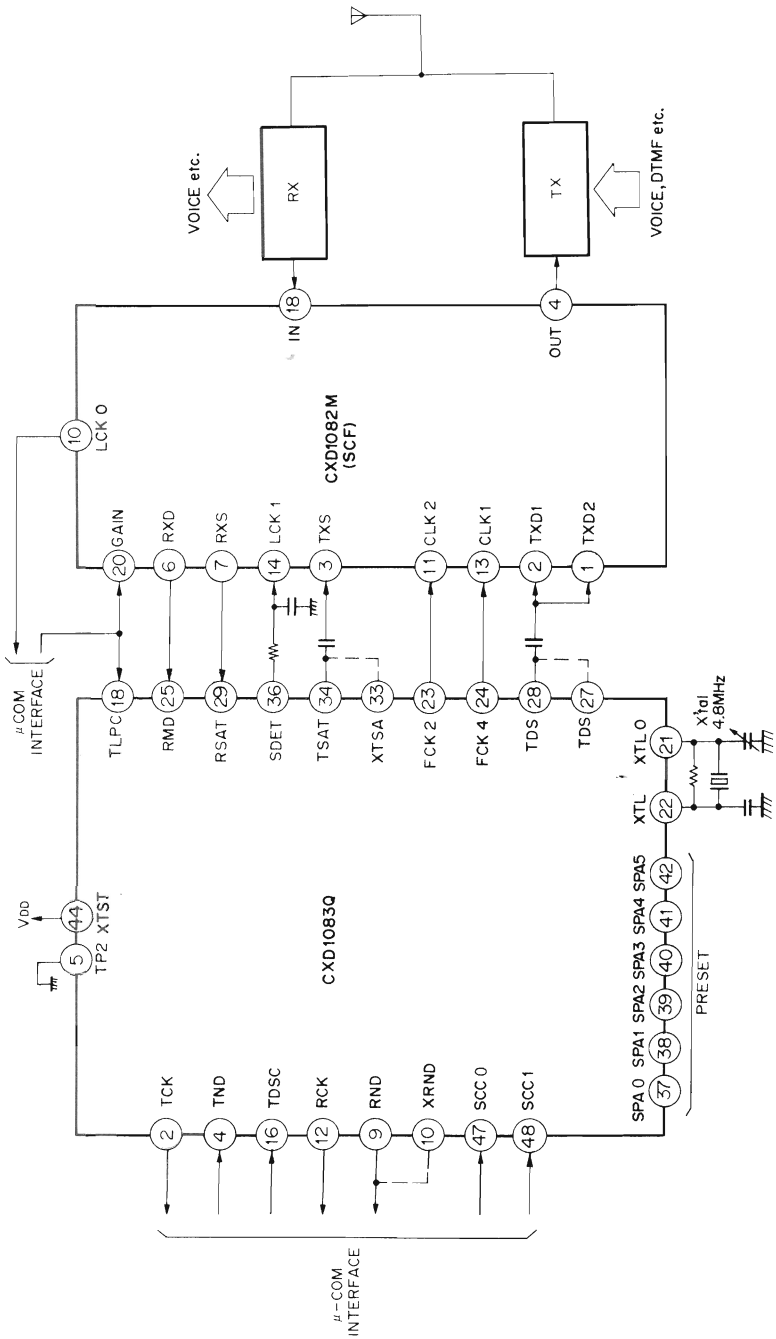
Fig. 3 Timing of TCK and TND

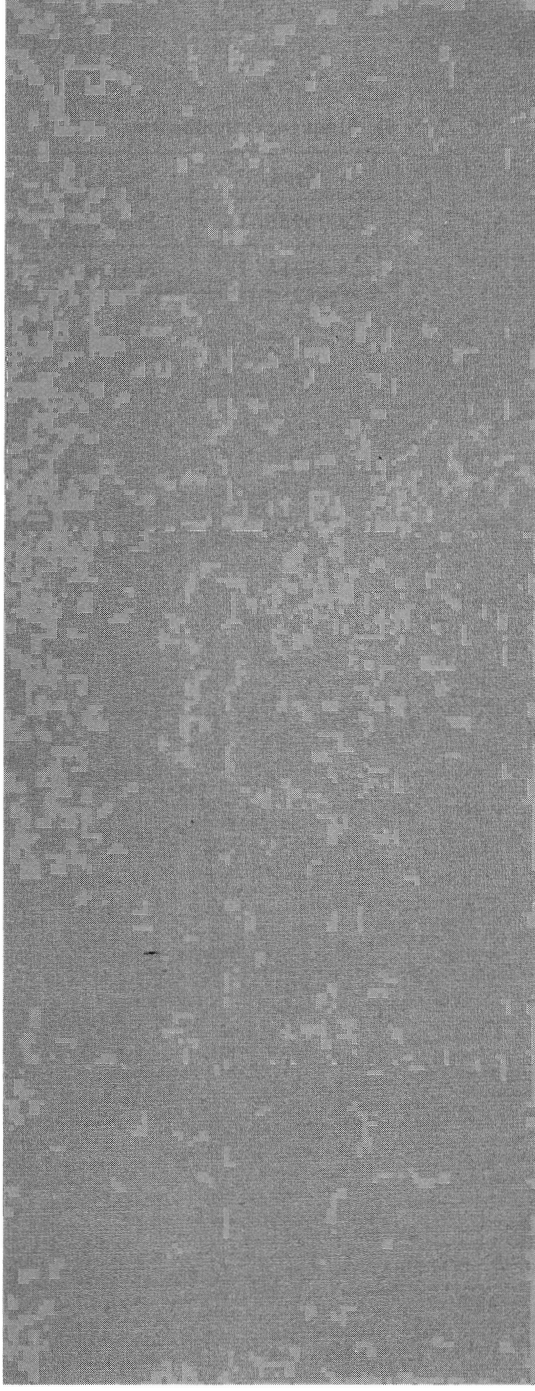
Also, at the time of sending of DATA and ST, frequency characteristics of filter connected to sending output TDS or XTDS differ. Therefore, change over frequency of clock (FCK2) to be given to the switch and capacitor filter in CXD1082M by TLPC (pin 18) as shown in List 2 below.

Sending	TLPC	FCK2	Cut-off frequency of filter
DATA	"H"	400 kHz	18.5 kHz
ST	"L"	200 kHz	9.25 kHz

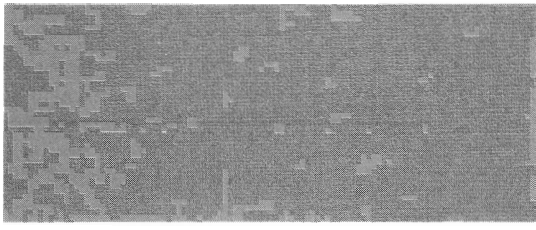
List 2: Changeover of TLPC at the time of sending of DATA and ST

Application Circuit





Frequency Synthesizer PLL



6) Frequency Synthesizer PLL

Type	Function	Page
CX-7925B/-1	Frequency Synthesizer PLL	425
CX-7961A/-1	Frequency Synthesizer PLL	436

SONY CX-7925B/7925B-1

Frequency Synthesizer PLL

Description

CX-7925B is a PLL IC for the digital selection of AM, FM and TV Broadcasting as well as other radio waves, developed using the high-speed N-channel silicon gate MOS technology.

Features

- The maximum operating frequency is warranted as follows
  CX-7925B Up to 300MHz
  CX-7925B-1 Up to 350MHz
  They can be used up to 1GHz when used combined with an ECL prescaler (general-purpose).
- Programmable divider makes it possible to divide a program frequency up to 1/262,151.
- Programmable reference divider realizes selection of a given reference frequency (e.g. 244Hz–2MHz can be selected when a 4MHz crystal oscillator is used).
- High C/N ratio with the high-speed phase comparator.
- Operation control using three terminals in serial mode.
- Independent 3 terminals (AM1, FM1 and TV1) are provided for a high frequency signal input depending on its frequency band.
- Multi-purpose output terminals are provided (AO, BO).
- Low power consumption (120mW Type)

Structure

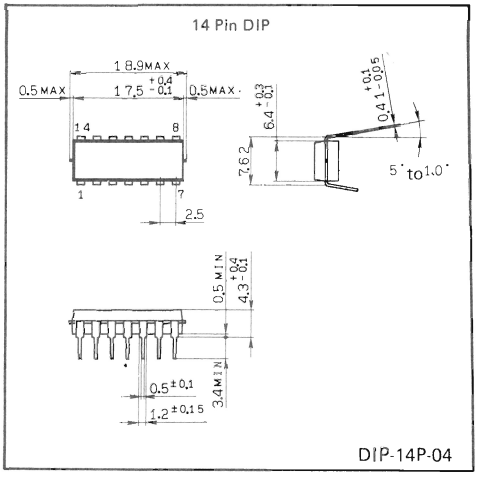
N-channel silicon gate MOS

Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

• Supply voltage	V_{DD}	−0.5 to +7	V
• Pin input voltage	V_{IN}	−1 to +7	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Package Outline

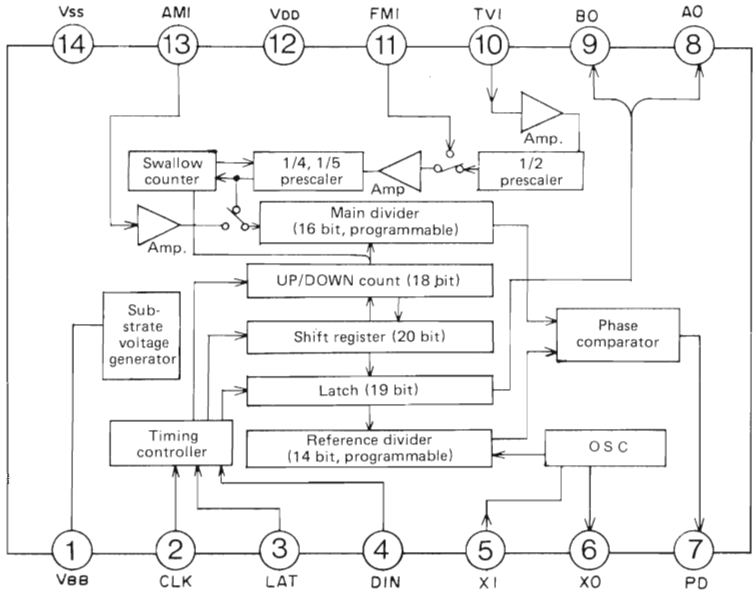
Unit: mm



Recommended Operating Conditions

Item	Pin, remark	Symbol	Operating range	Unit
Supply voltage		V_{DD}	4.5 – 5.5	V
High level input voltage	CLK, DIN	V_{IH}	+2.6 – V_{DD} +0.5	V
Low level input voltage	LAT	V_{IL}	−1.0 – 0.8	V
High frequency signal input amplitude	TVI	e_{IN}	0.3 – 4.0	Vp-p
High frequency signal input amplitude	VMI	e_{IN}	0.2 – 4.0	Vp-p
High frequency input amplitude	AMI	e_{IN}	0.2 – 2.5	Vp-p
High frequency input amplitude	XI	e_{IN}	0.6 – 4.0	Vp-p
Operating temperature		Topr	−20 +70	°C

Block Diagram and Pin Configuration



Pin Description

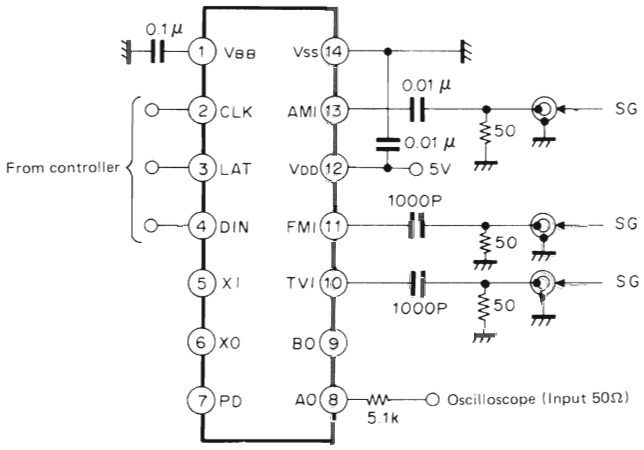
No.	Symbol	Description
1	V_{BB}	Substrate terminal (connect 0.01μF capacitor to the ground)
2	CLK	Clock input terminal for 20-bit serial data input (to be shifted with signal rise)
3	LAT	Latch signal input terminal for shift register input data (to be latched with signal rise) as well as the UP/DOWN clock input terminal (its state to be changed with signal rise)
4	DIN	Data input terminal as well as the UP/DOWN mode switching terminal (UP at "H" level, DOWN at "L" level)
5	XI	Crystal oscillator connection terminal for the reference signal generation (13MHz max., 4.0MHz standard)
6	XO	
7	PD	Phase comparator output terminal (3 states)
8	AO	External control signal output terminal/unlock output terminal (E/E MOS push-pull)
9	BO	External control signal output terminal/data check terminal (E/E MOS push-pull)
10	TVI	High frequency signal input terminal (300MHz or 350MHz max.) 1/2 prescaler is built-in.
11	FMI	High frequency signal input terminal (150MHz or 180MHz max.)
12	V_{DD}	Power supply (+5V)
13	AMI	High frequency signal input terminal (40MHz or 50MHz max.)
14	V_{SS}	Ground terminal

Electrical Characteristics (within the recommended operating condition range, unless otherwise specified) V_{SS} = 0V

Item	Pin, remark	Symbol	Condition	CX-7925B			CX-7925B-1			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating power supply current	V_{DD}	I_{DD}	Note 2		24	40		28	40	mA
Operating input frequency	TVI	fop	e_{IN} = 0.3–0.4Vp-p	20		300	20		350	MHz
	FMI	fop	e_{IN} = 0.2–4.0Vp-p	20		150	20		180	MHz
	AMI	fop	e_{IN} = 0.2–2.5Vp-p	0.05		40	0.05		50	MHz
Input leak current	Logic input	I_{IL}	$V_{IH} = 0–V_{DD}$ Note 1	–10		+10	–10		+10	μA
High level output current	Phase comparator (3-value output) PD	I_{OH}	V_{OUT} = 3V Note 2			–0.2			–0.2	mA
Low level output current		I_{OL}	V_{OUT} = 1V Note 2	0.2			0.2			mA
High impedance leak current		I_{HZ}	V_{OUT} = 2V Note 1	–50		+50	–50		+50	nA
High level output voltage	Push-pull by E/E MOS: Structure AO, BO	V_{OH}	I_{OH} = –20μA	2.8			2.8			V
Low level output voltage		V_{OL}	I_{OL} = 1mA			0.6			0.6	V

Note 1) Ta = 25°C Note 2) V_{DD} = 5V Ta = 25°C

Operating Input Frequency Measuring Circuit



Control input data to CX-7925B: T1-H, T2-H, A-L, B-H

SG: HP's 8640B (Input level is directly read with the built-in level meter)

Operating Description

(1) Signal input from the local oscillator

CX-7925B is provided with 3 independent input terminals corresponding to the signal frequency and applications.

- AMI terminal

  Reception terminal of AM broadcast with the warranted signal input up to 40MHz or 50MHz. The frequency division ratio using this terminal is 1/2 to 1/65537.

- FMI terminal

  Reception terminal of FM and TV broadcasts with the warranted signal input up to 150MHz or 180MHz. An external prescaler is not required in reception of FM channels. When TV is received, entire TV band width can be covered with combination of an external prescaler up to 1/8. The frequency division ratio ranges from 1/12 to 1/262.151. This terminal is open when it is not in use.

- TVI terminal

  This terminal is dedicated to reception of TV broadcasts. Signal input up to 300MHz or 350MHz are warranted with the built-in 1/2 prescaler. When combined with an external prescaler up to 1/4, entire TV bandwidth can be covered. The frequency division ranges from 1/24 to 1/524.302. When this terminal is not in use, it is grounded internally via a resistor of more than 100 kΩ.

(2) Phase comparator

The phase comparator output (PD terminal) has a 3-value level. When the input signal is advanced in phase than the reference signal, the terminal becomes HIGH level; LOW level when the phase is lagging behind and high impedance when they are in phase.

(3) Control signal and control system

CX-7925B is designed as a controller compatible with general 4- or 8-bit microcomputers. Three control input terminals, CLK, LAT and DIN, are available. Two control output terminals, AO and BO are also available. By combining these terminals properly, simplification of the system or multi-functional system can be realized.

(3-1) Control signal input modes

CX-7925B has three control signal input modes. DATA INPUT mode (normal mode), UP/DOWN mode and DATA CHECK mode with each of them differing in its signal input system.

(a) DATA INPUT mode (normal mode)

To set all initial values of CX-7925B it is required to input total 40-bit data in 20 bits each in this mode. When data is input to the DIN terminal with the LAT terminal in the LOW state, the data is input in one bit each to the shift register with the rise of clock input to the CLK terminal. After transmitting 20-bit data to the shift register, the data is latched when the LAT terminal is set to HIGH with the CLK in the HIGH state. (After latching of the data, the LAT terminal must be reset to LOW. Varying of the DIN and CLK terminals with the LAT terminal HIGH may affect the data internally.)
As will be described in detail later, input data is input either in the programmable divider or reference divider depending on a state of the last bit C. In practice, input the 20-bit data including the reference divider frequency division number, input terminal selection and AO/BO output terminal data from the controller first of all in the above manner. At this time, the last bit C of the data is set to LOW.
Then, input the 20-bit data including the programmable divider setting data in the same manner with the last bit C set to HIGH. In this manner, all internal states are set. After this setting, the latter 20-bit data only is varied when only the programmable divider value is varied. (At this time, C is set to HIGH without fail.)
When the programmable divider value is varied (selection of a broadcast channel, AFT), the following UP/DOWN mode can be used more effectively.

(b) UP/DOWN mode

After setting the CLK terminal to LOW, the UP/DOWN content can be increased or decreased by one depending on the level of HIGH or LOW of the DIN terminal when the LAT terminal (usually LOW level) is changed from HIGH to LOW. By repeating this process, the setting value of the programmable divider can be varied as required.

(c) DATA CHECK mode

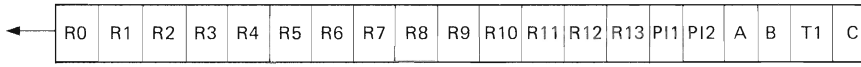
This mode is used to check if the data from the controller is correctly input to the shift register. The data left in the shift register immediately after the input data is latched is output in one bit each from the BO terminal when a clock is input to the CLK terminal after the LAT terminal is set to LOW with the CLK terminal held to HIGH. However, the shift register data is output from the BO terminal when the T1 or T2 bit of the data is respectively at HIGH or LOW only. T1 and T2 bits will be described in the following item.

(3-2) Control data assignment

The CX-7925B control data is assigned in 20 bits. The last 2 bits are the data recognition code and their recognition will tell the data content. Switching to the TEST mode is also performed using this code internally. As is described in the following, each of the frequency division number of the programmable divider and reference divider is given in the binary value with the leading digit of LSB.

(a) Control input data of the reference divider, etc. (C = LOW)

This data can be described as an initialization setting data and it is always input whenever the power supply is fed or a channel band is switched. The input data is assigned as follows.



- R0 – R13: Reference divider frequency division number (binary value with the LSB of R0). In practice, an offset component between the actual frequency division number and the input data. Their relationship is as follows.
  (Actual frequency division number) = (Input data) + 2
- P11, P12: Specification of the signal input terminal.

Input / PI1, PI2	AMI	FMI	TVI
PI1	–	L	H
PI2	L	H	H

- A, B, T1: Each of the AO and BO terminals have 2 functions which are switched depending on the T1 value. When T1 is at LOW, A and B values are output as they are to the AO and BO terminals. These signals can be used for switching an external prescaler's frequency division ratio, the filter constant and channel band, etc. When the prescaler M54465P (Mitsubishi) is used, the selection code of frequency division ratio will be as follows:

Frequency division ratio / A, B	1/2	1/4	1/8
A	H	L	L
B	L	H	L

When T1 is at HIGH, the AO output terminal outputs the LOCK/UNLOCK state of the phase comparator.

AO terminal H: UNLOCK
L: LOCK

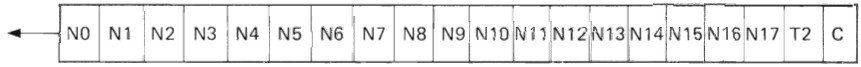
This can be used as a muting signal.
The BO terminal becomes, as described in (3-1) (C), the data output terminal of the shift register and the shift register content is continuously output by inputting the clock to the CLK terminal. It must be noted the AO and BO terminals can not be used for external control when T1 is at HIGH.

• C: This is a code to determine the latch direction of the input data. In this case, set to LOW.

Input data				AO output	BO output
T2	T1	A	B		
L	L			A	B
L	H			UNLOCK signal	Shift register output
H	H	L	L	Reference divider outputs	Main divider output
H	H	L	H	Main divider output	

(b) Programmable divider input data (C = HIGH)

This data determines the programmable divider's frequency division ratio.



• N0 – N17: Programmable divider frequency division number.
(Binary value with N0 as the LSB.) Actual frequency division number will be as follows depending on a terminal selected for the signal input.

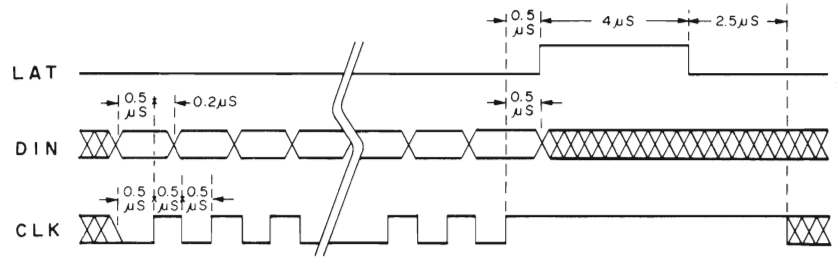
Control data		Input terminal	Range of the frequency division input data N	Relation between N and the true frequency division number ND	Range of the true frequency division number ND
PI1	PI2				
–	L	AMI	0 – 65,535	N + 2	2 – 65,537
L	H	AMI	4 – 262,143	N + 8	12 – 262,151
H	H	TVI	4 – 262,143	2 • (N + 8)	24 – 524,302

• T2: T2 is used for selection of the test mode. Set this data to LOW usually.
When the frequency division output and reference output are to be checked, set this T2 bit and T1 bit to HIGH and A and B bits to LOW. In this instance, the AO and BO output terminals output a reference output and a frequency division output respectively.

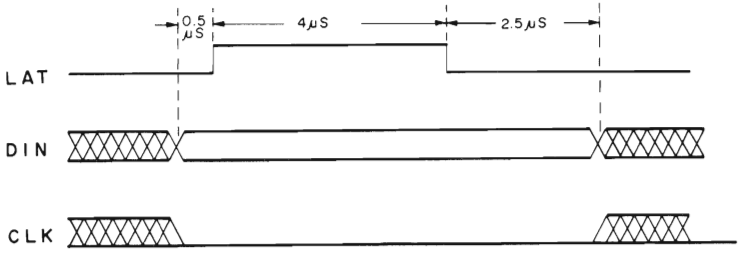
• C: As described before. Set to HIGH in this case.

(3-3) Data input and control signal times

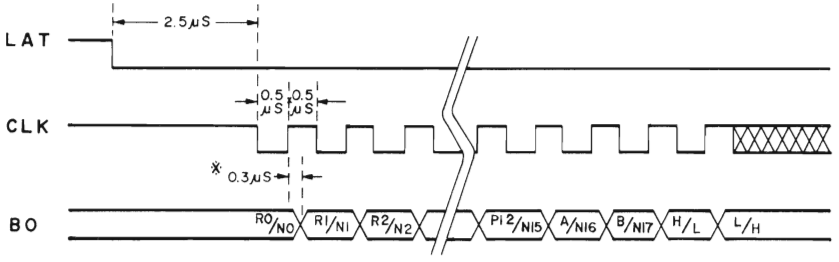
(a) Data input mode (normal mode) Each timing shows the minimum value unless otherwise described.



(b) UP/DOWN mode



(c) DATA CHECK mode (Data check of the shift register)



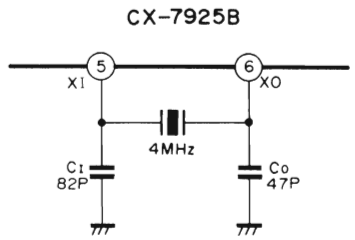
(* denotes data is output within this timing.)

(4) Reference signal (Input signal of the reference divider)

CX-7925B can generate a reference signal by connecting a crystal oscillator to XI and XO. It also allows an external clock to be used as a reference signal by inputting an external clock signal to the XI terminal.

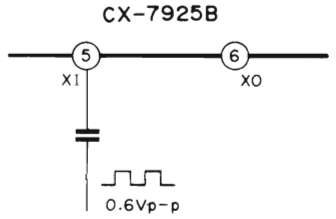
(4-1) Reference signal generator with the built-in oscillator

As shown below, connect a crystal oscillator to the XI and XO terminals. A crystal oscillator with the frequency of 1MHz – 13MHz can be used. The diagram below shows an example when a standard 4MHz oscillator is used. Be sure to make the capacitance ratio of C_I and C_O at 1 – 2 : 1 and theeir serial capacitance values be the specified load capacitance of the crystal oscillator.

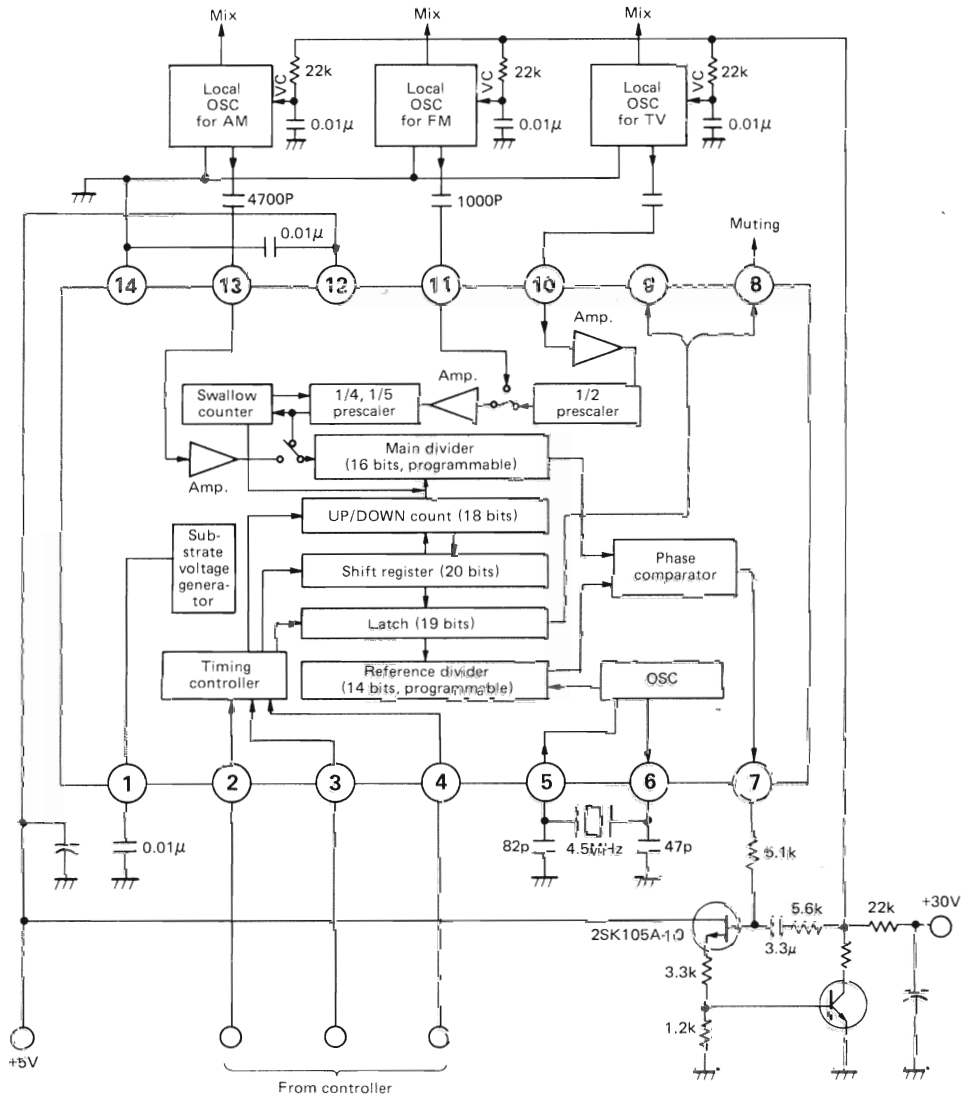


(4-2) Reference signal generator with an external clock

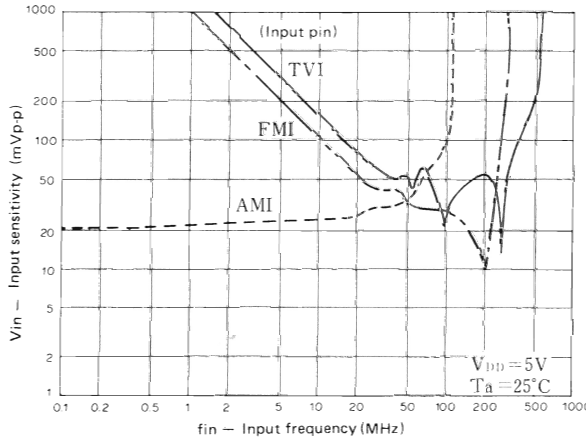
When an external clock signal, e.g. a clock signal obtained from the controller, is used as the reference clock, connect it to the XI terminal via a capacitor as shown below. The clock frequency is warranted up to 13MHz but use signal of proper rise and decay (more than 5V/μs) especially when the frequency is low. This will serve as a protection from mulfunction.



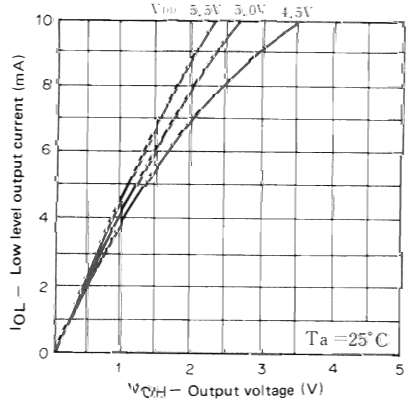
Application Circuit

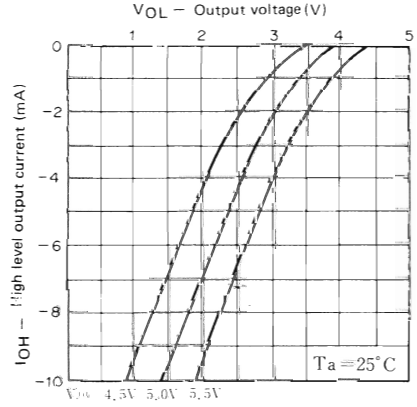


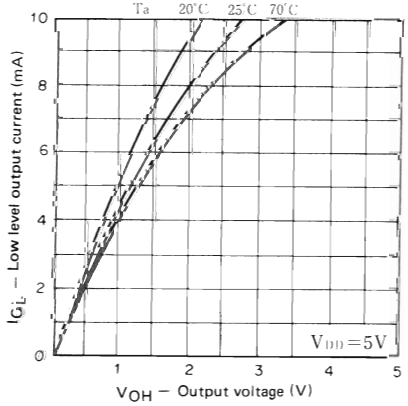
High Frequency Input Sensitivity Characteristics

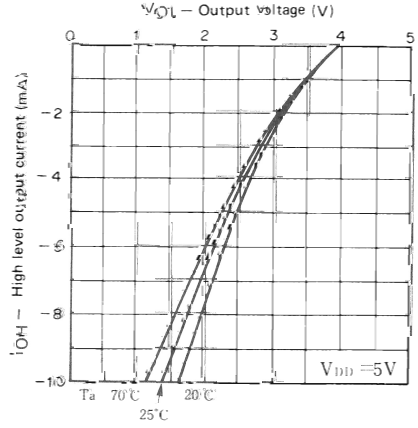


Output Current Characteristics of the AO and BO Terminals

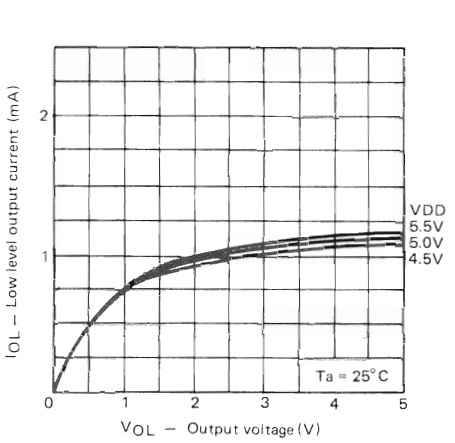


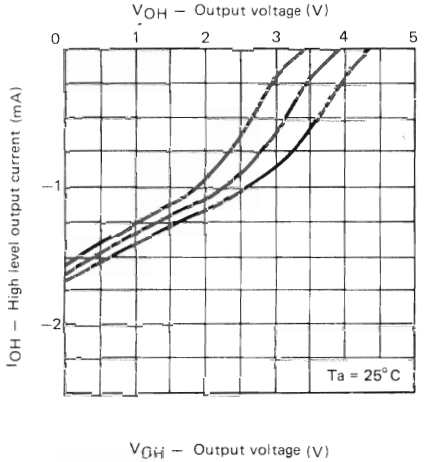


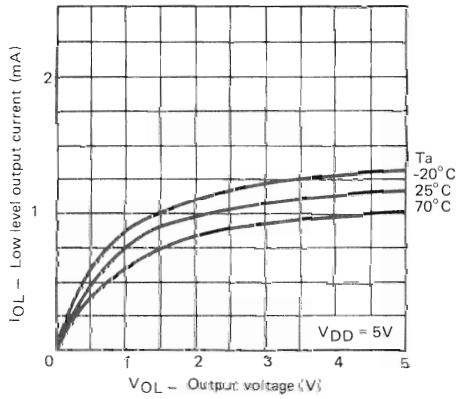


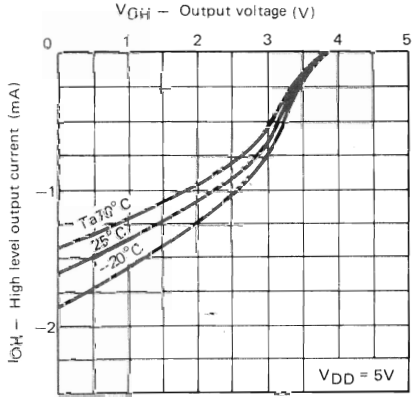


Output Current Characteristics of the PD (Phase Comparator)

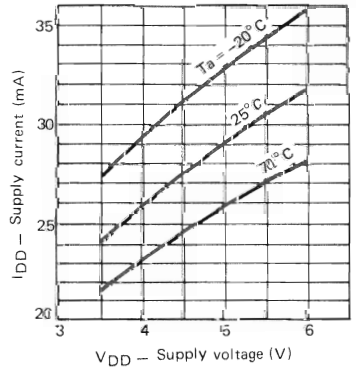








Power Supply Current I_{DD} and Voltage Characteristics



SONY CX-7961A/7961A-1

Frequency Synthesizer PLL

Description

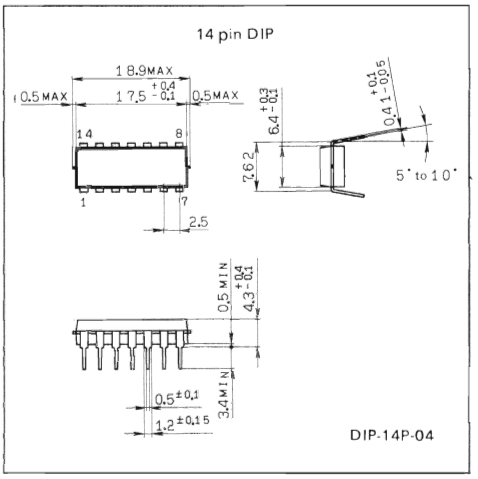
CX-7961A is a PLL IC for the digital selection of AM, FM and TV Broadcasting as well as other radio waves, developed using the high-speed N-channel silicon gate MOS technology.

Features

- The maximum operating frequency is warranted as follows:
  CX-7961A Up to 180MHz
  CX-7961A-1 Up to 240MHz
  They can be used up to 1GHz when used combined with an ECL prescaler (general-purpose).
- Programmable divider makes it possible to divide a program frequency up to 1/262,151.
- Programmable reference divider realizes selection of a given reference frequency (e.g. 244Hz – 2MHz can be selected when a 4MHz crystal oscillator is used).
- High C/N ratio with the high-speed phase comparator.
- Operation control using three terminals in serial mode.
- Independent 3 terminals (AM1, FM1 and TV1) are provided for a high frequency signal input depending on its frequency band.
- Multi-purpose output terminals are provided (AO, BO).
- Low power consumption (35 mW Typ)

Package Outline

Unit: mm



Structure

N-channel silicon gate MOS

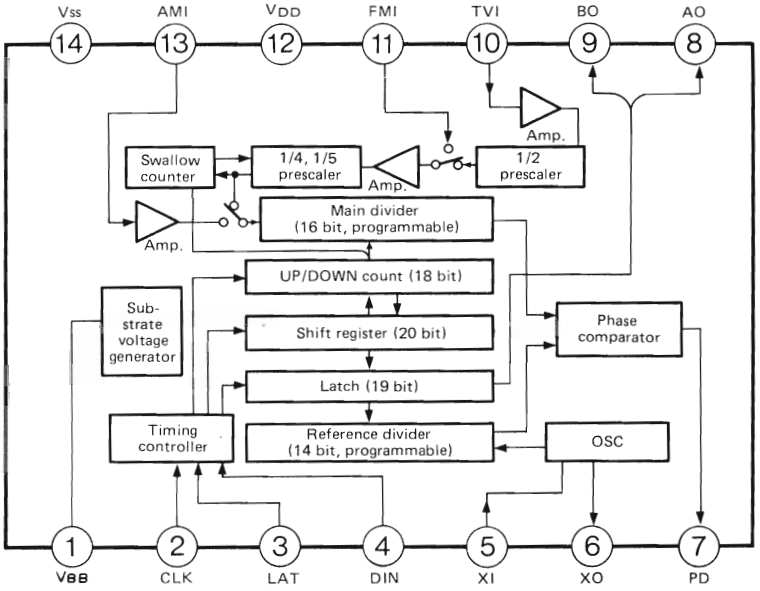
Absolute Maximum Ratings (T_a = 25°C, V_{SS} = 0V)

• Supply voltage	V_{DD}	−0.5 to +7	V
• Pin input voltage	V_{IN}	−1 to +7	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Recommended Operating Conditions

Item	Pin, remark	Symbol	Operating range	Unit
Power supply voltage		V_{DD}	2.7 – 3.3	V
High level input voltage	CLK, DIN LAT	V_{IH}	1.5 – V_{DD} +0.5	V
Low level input voltage		V_{IL}	−0.5 – +0.5	V
High frequency signal input amplitude	TVI	e_{IN}	0.2 – 2.5	Vp-p
High frequency signal input amplitude	VMI	e_{IN}	0.2 – 2.5	Vp-p
High frequency input amplitude	AMI	e_{IN}	0.2 – 1.5	Vp-p
High frequency input amplitude	XI	e_{IN}	0.6 – 2.5	Vp-p
Operating temperature		Topr	−20 – +70	°C

Block Diagram and Pin Configuration



Pin Description

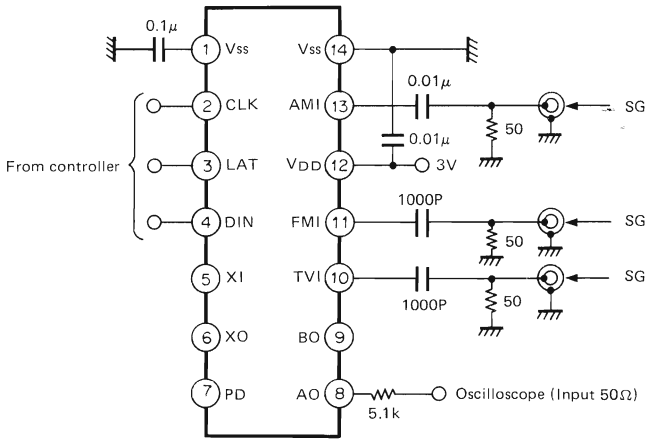
No.	Symbol	Description
1	V_{BB}	Substrate terminal (connect 0.01μF capacitor to the ground)
2	CLK	Clock input terminal for 20-bit serial data input (to be shifted with signal rise)
3	LAT	Latch signal input terminal for shift register input data (to be latched with signal rise) as well as the UP/DOWN clock input terminal (its state to be changed with signal rise)
4	DIN	Data input terminal as well as the UP/DOWN mode switching terminal (UP at "H" level, DOWN at "L" level)
5	XI	Crystal oscillator connection terminal for the reference signal generation (7.2MHz max., 4.0MHz standard)
6	XO	
7	PD	Phase comparator output terminal (three states)
8	AO	External control signal output terminal/unlock output terminal (E/E MOS push-pull)
9	BO	External control signal output terminal/data check terminal (E/E MOS push-pull)
10	TVI	High frequency signal input terminal (180MHz or 240MHz max.) 1/2 prescaler is built-in.
11	FMI	High frequency signal input terminal (90MHz or 125MHz max.)
12	V_{DD}	Power supply (+3V)
13	AMI	High frequency signal input terminal (20MHz or 25MHz max.)
14	V_{SS}	Ground terminal

Electrical Characteristics (within the recommended operating condition range, unless otherwise specified) V_{SS} = 0V

Item	Pin, remark	Symbol	Condition	CX-7961A			CX-7961A-1			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating power supply current	V_{DD}	I_{DD}	f_{IN} = 110MHz Note 2		10	18		13	18	mA
Operating input frequency	TVI	fop	e_{IN} = 0.2−2.5Vp-p	10		180	10		240	MHz
	FMI	fop	e_{IN} = 0.2−2.5Vp-p	10		90	10		125	MHz
	AMI	fop	e_{IN} = 0.2−1.5Vp-p	0.05		20	0.05		25	MHz
Input leak current	Logic input	I_{IL}	V_{IH} = 0−V_{DD} Note 1	−10		+10	−10		+10	μA
High level output current	Phase comparator (3-value output) PD	I_{OH}	V_{OUT} = 1.5V Note 2			−0.1			−0.1	mA
Low level output current		I_{OL}	V_{OUT} = 0.5V Note 2	+0.1			+0.1			mA
High impedance leak current		I_{HZ}	V_{OUT} = 1.0V Note 1	−50		+50	−50		+50	nA
High level output voltage	Push-pull by E/E MOS: Structure AO, BO	V_{OH}	I_{OH} = −20μA	1.5			1.5			V
Low level output voltage		V_{OL}	I_{OL} = 0.6mA			0.4			0.4	V

Note 1) Ta = 25°C Note 2) V_{DD} = 5V Ta = 25°C

Operating Input Frequency Measuring Circuit



Control input data to CX-7961A/7961A-1: T1-H, T2-H, A-L, B-H

SG: HP's 8640B (Input level is directly read with the built-in level meter)

Description of Operation

(1) Signal input from the local oscillator

CX-7961A is provided with 3 independent input terminals corresponding to the signal frequency and applications.

- AMI terminal

  Reception terminal of AM broadcast with the warranted signal input up to 20MHz or 25MHz. The frequency division ratio using this terminal is 1/2 to 1/65537.

- FMI terminal

  Reception terminal of FM and TV broadcasts with the warranted signal input up to 90MHz or 125MHz. An external prescaler is not required in reception of FM channels. When TV is received, entire TV band width can be covered with combination of an external prescaler up to 1/8. The frequency division ratio ranges from 1/12 to 1/262.151. This terminal is open when it is not in use.

- TVI terminal

  This terminal is dedicated to reception of TV broadcasts. Signal input up to 180MHz or 240MHz are warranted with the built-in 1/2 prescaler. When combined with an external prescaler up to 1/4, entire TV bandwidth can be covered. The frequency division ranges from 1/24 to 1/524.302. When this terminal is not in use, it is grounded internally via a resistor of more than 100 kΩ.

(2) Phase comparator

The phase comparator output (PD terminal) has a 3-value level. When the input signal is advanced in phase than the reference signal, the terminal becomes HIGH level; LOW level when the phase is lagging behind and high impedance when they are in phase.

(3) Control signal and control system

CX-7961A is designed as a controller compatible with general 4-bit or 8-bit microcomputers. Three control input terminals, CLK, LAT and DIN, are available. Two control output terminals, AO and BO are also available. By combining these terminals properly, simplification of the system or multi-functional system can be realized.

(3-1) Control signal input modes

CX-7961A has three control signal input modes. DATA INPUT mode (normal mode), UP/DOWN mode and DATA CHECK mode with each of them differing in its signal input system.

(a) DATA INPUT mode (normal mode)

To set all initial values of CX-7961A it is required to input total 40-bit data in 20 bits each in this mode. When data is input to the DIN terminal with the LAT terminal in the LOW state, the data is input in one bit each to the shift register with the rise of clock input to the CLK terminal. After transmitting 20-bit data to the shift register, the data is latched when the LAT terminal is set to HIGH with the CLK in the HIGH state. (After latching of the data, the LAT terminal must be reset to LOW. Varying of the DIN and CLK terminals with the LAT terminal HIGH may affect the data internally.)
As will be described in detail later, input data is input either in the programmable divider or reference divider depending on a state of the last bit C. In practice, input the 20-bit data including the reference divider frequency division number, input terminal selection and AO/BO output terminal data from the controller first of all in the above manner. At this time, the last bit C of the data is set to LOW.
Then, input the 20-bit data including the programmable divider setting data in the same manner with the last bit C set to HIGH. In this manner, all internal states are set. After this setting, the latter 20-bit data only is varied when only the programmable divider value is varied. (At this time, C is set to HIGH without fail.)
When the programmable divider value is varied (selection of a broadcast channel, AFT), the following UP/DOWN mode can be used more effectively.

(b) UP/DOWN mode

After setting the CLK terminal to LOW, the UP/DOWN content can be increased or decreased by one depending on the level of HIGH or LOW of the DIN terminal when the LAT terminal (usually LOW level) is changed from HIGH to LOW. By repeating this process, the setting value of the programmable divider can be varied as required.

(c) DATA CHECK mode

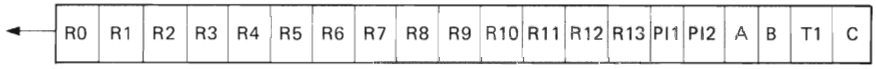
This mode is used to check if the data from the controller is correctly input to the shift register. The data left in the shift register immediately after the input data is latched is output in one bit each from the BO terminal when a clock is input to the CLK terminal after the LAT terminal is set to LOW with the CLK terminal held to HIGH. However, the shift register data is output from the BO terminal when the T1 or T2 bit of the data is respectively at HIGH or LOW only. T1 and T2 bits will be described in the following item.

(3-2) Control data assignment

The CX-7961A control data is assigned in 20 bits. The last 2 bits are the data recognition code and their recognition will tell the data content. Switching to the TEST mode is also performed using this code internally. As is described in the following, each of the frequency division number of the programmable divider and reference divider is given in the binary value with the leading digit of LSB.

(a) Control input data of the reference divider, etc. (C = LOW)

This data can be described as an initialization setting data and it is always input whenever the power supply is fed or a channel band is switched. The input data is assigned as follows.



- R0 – R13: Reference divider frequency division number (binary value with the LSB of R0). In practice, an offset component between the actual frequency division number and the input data. Their relationship is as follows.
  (Actual frequency division number) = (Input data) + 2
- PI1, PI2: Specification of the signal input terminal.

Input / PI1, PI2	AMI	FMI	TVI
PI1	–	L	H
PI2	L	H	H

- A, B, T1: Each of the AO and BO terminals have 2 functions which are switched depending on the T1 value. When T1 is at LOW, A and B values are output as they are to the AO and BO terminals. These signals can be used for switching an external prescaler's frequency division ratio, the filter constant and channel band, etc. When the prescaler M54465P (Mitsubishi) is used, the selection code of frequency division ratio will be as follows:

Frequency division ratio / A, B	1/2	1/4	1/8
A	H	L	L
B	L	H	L

When T1 is at HIGH, the AO output terminal outputs the LOCK/UNLOCK state of the phase comparator.

AO terminal H: UNLOCK
L: LOCK

This can be used as a muting signal.
The BO terminal becomes, as described in (3-1) (C), the data output terminal of the shift register and the shift register content is continuously output by inputting the clock to the CLK terminal. It must be noted the AO and BO terminals can not be used for external control when T1 is at HIGH.

• C: This is a code to determine the latch direction of the input data. In this case, set to LOW.

Input data				AO output	BO output
T2	T1	A	B		
L	L			A	B
L	H			UNLOCK signal	Shift register output
H	H	L	L	Reference divider output	Main divider output
H	H	L	H	Main divider output	

(b) Programmable divider input data (C = HIGH)

This data determines the programmable divider's frequency division ratio.

←	N0	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	T2	C

• N0 – N17: Programmable divider frequency division number.
(Binary value with N0 as the LSB.) Actual frequency division number will be as follows depending on a terminal selected for the signal input.

Control data		Input terminal	Range of the frequency division input data N	Relation between N and the true frequency division number ND	Range of the true frequency division number ND
PI1	PI2				
–	L	AMI	0 – 65,535	N + 2	2 – 65,537
L	H	AMI	4 – 262,143	N + 8	12 – 262,151
H	H	TVI	4 – 262,143	2 • (N + 8)	24 – 524,302

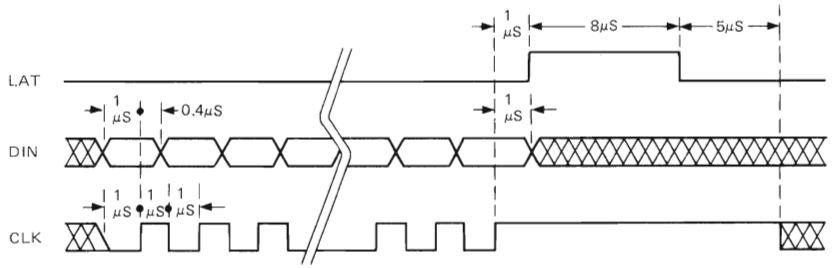
• T2: T2 is used for selection of the test mode. Set this data to LOW usually.
When the frequency division output and reference output are to be checked, set this T2 bit and T1 bit to HIGH and A and B bits to LOW. In this instance, the AO and BO output terminals output a reference output and a frequency division output respectively.

• C: As described before. Set to HIGH in this case.

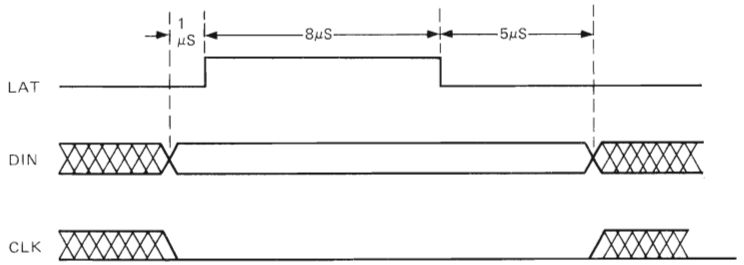
(3-3) Data input and control signal times

(a) Data input mode (normal mode)

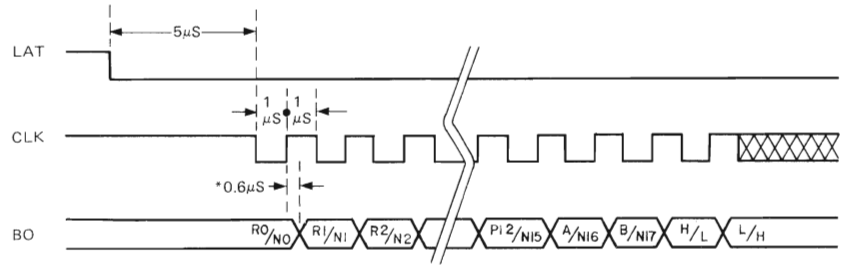
Each timing shows the minimum value unless otherwise described.



(b) UP/DOWN mode



(c) DATA CHECK mode (Data check of the shift register)



(* denotes data is output within this timing.)

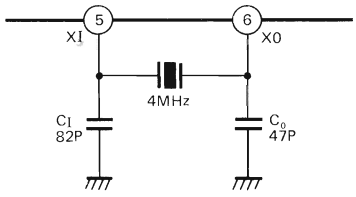
(4) Reference signal (Input signal of the reference divider)

CX-7961A can generate a reference signal by connecting a crystal oscillator to XI and X0. It also allows an external clock to be used as a reference signal by inputting an external clock signal to the XI terminal.

(4-1) Reference signal generator with the built-in oscillator

As shown below, connect a crystal oscillator to the XI and X0. A crystal oscillator with the frequency of 1MHz – 7.2MHz can be used. The diagram below shows an example when a standard 4MHz oscillator is used.
Be sure to make the capacitance ratio of C_I and C_0 at 1 – 1 : 1 and their serial capacitance values be the specified load capacitance of the crystal oscillator.

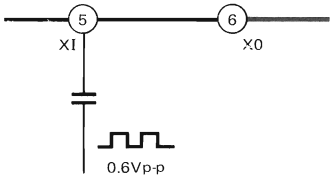
CX-7961A



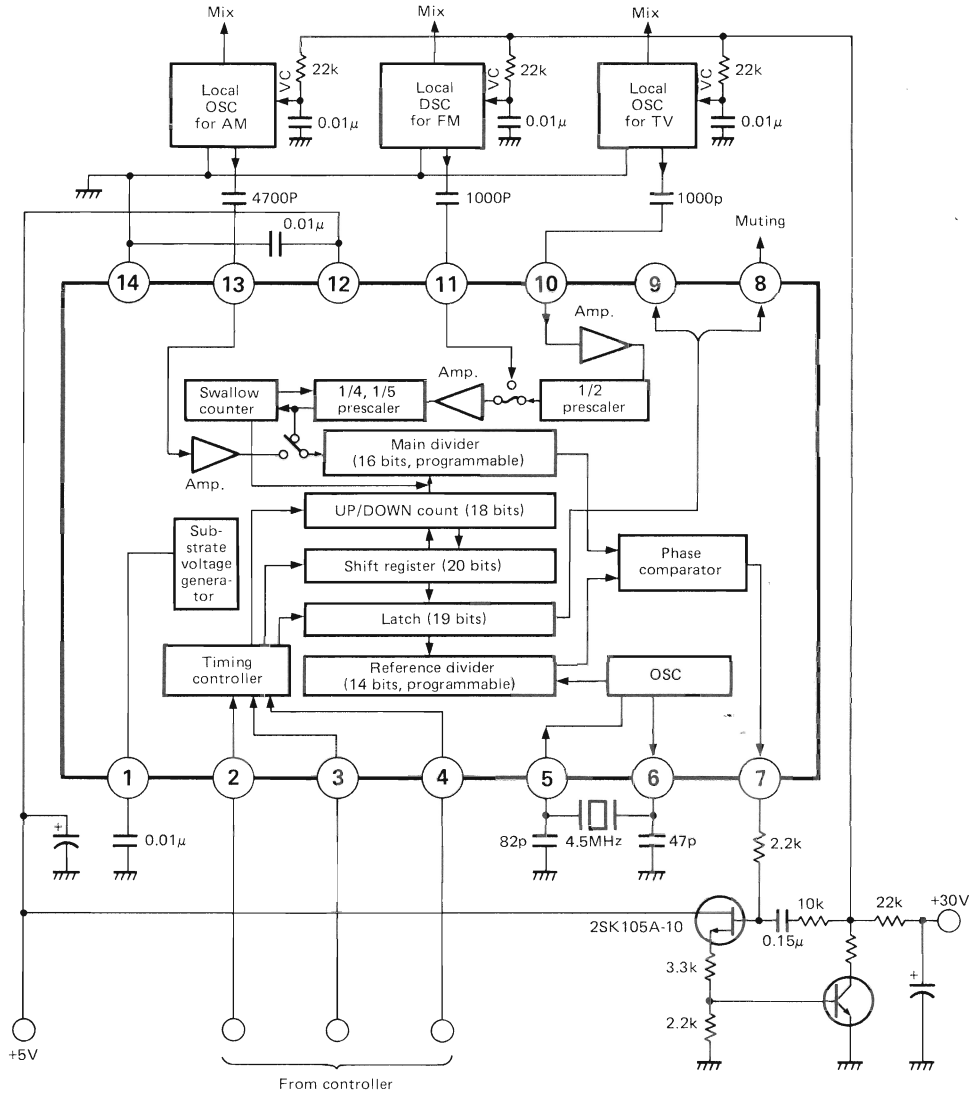
(4-2) Reference signal generator with an external clock

When an external clock signal, e.g. a clock signal obtained from the controller, is used as the reference clock, connect it to the XI terminal via a capacitor as shown below. The clock frequency is warranted up to 7.2MHz but use signal of proper rise and decay (more than 5V/μs) especially when the frequency is low. This will serve as a protection from mulfunction.

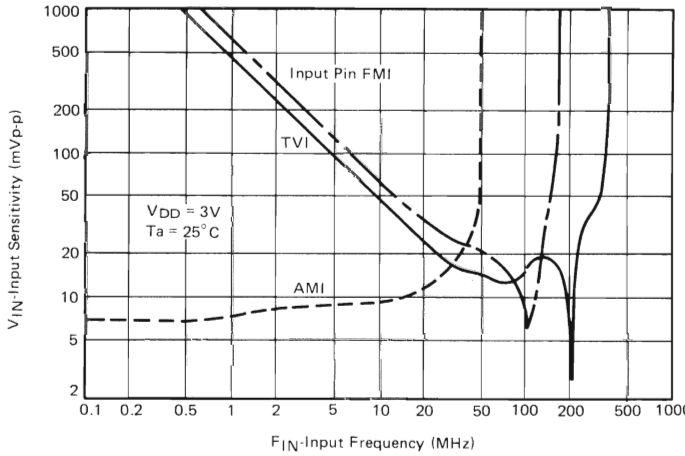
CX-7961A

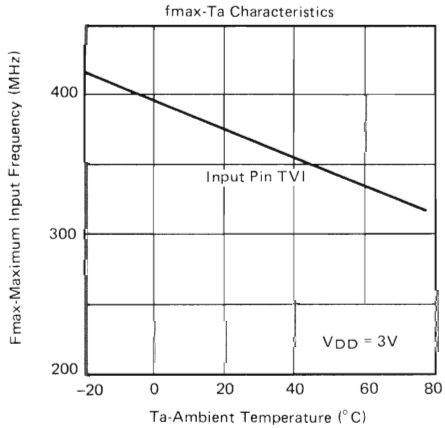


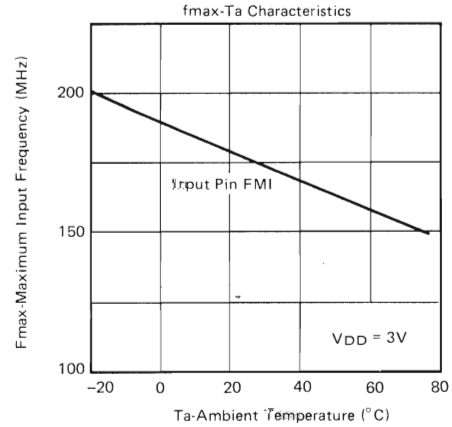
Application Circuit



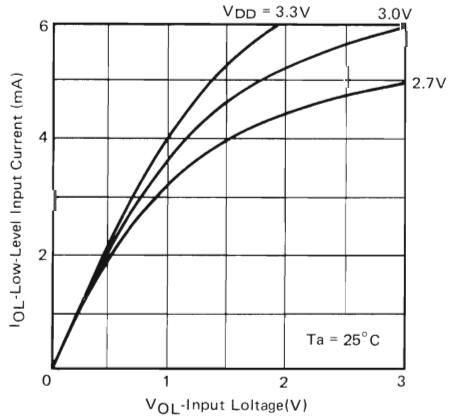
Characteristics of high-frequency input sensitivity

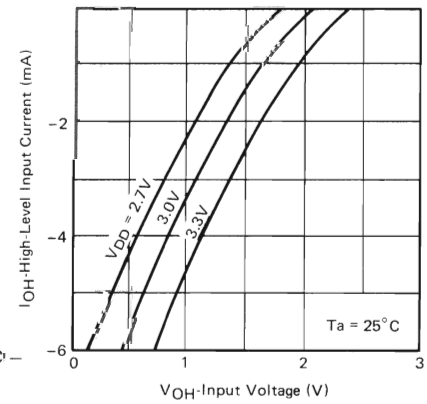




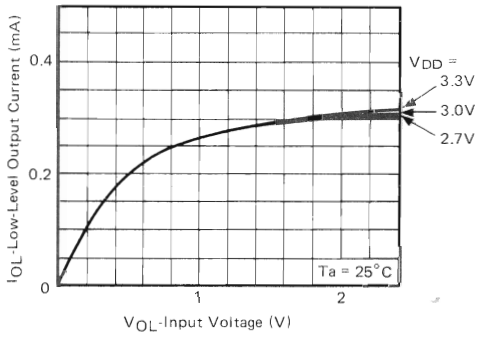


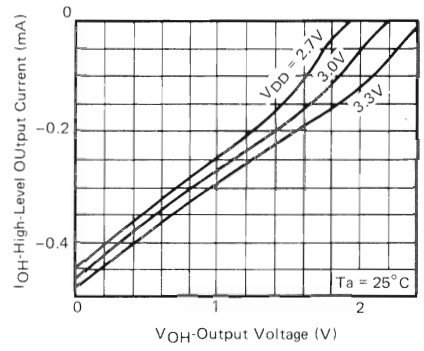
Output current characteristics of AO and BO terminals

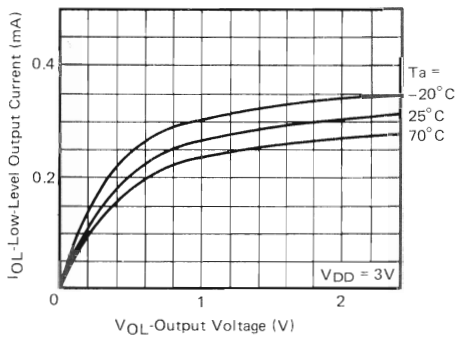


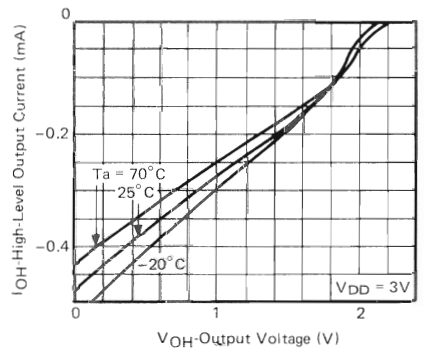


Output Current Characteristics of PD (Phase Discriminator) Terminal

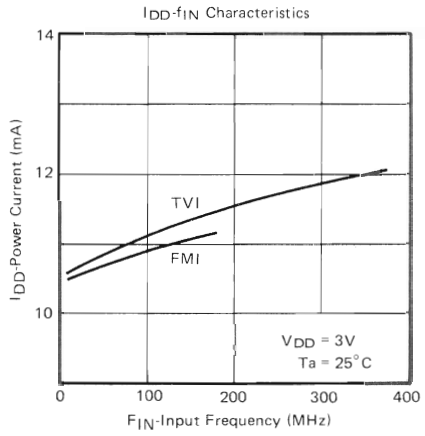


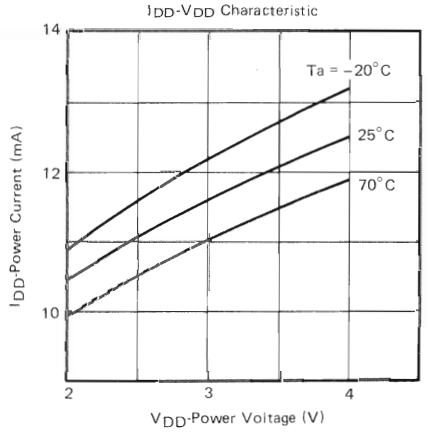






Power Current Characteristics





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